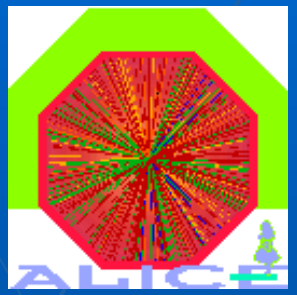

RD09

The ALICE Pixel Trigger System

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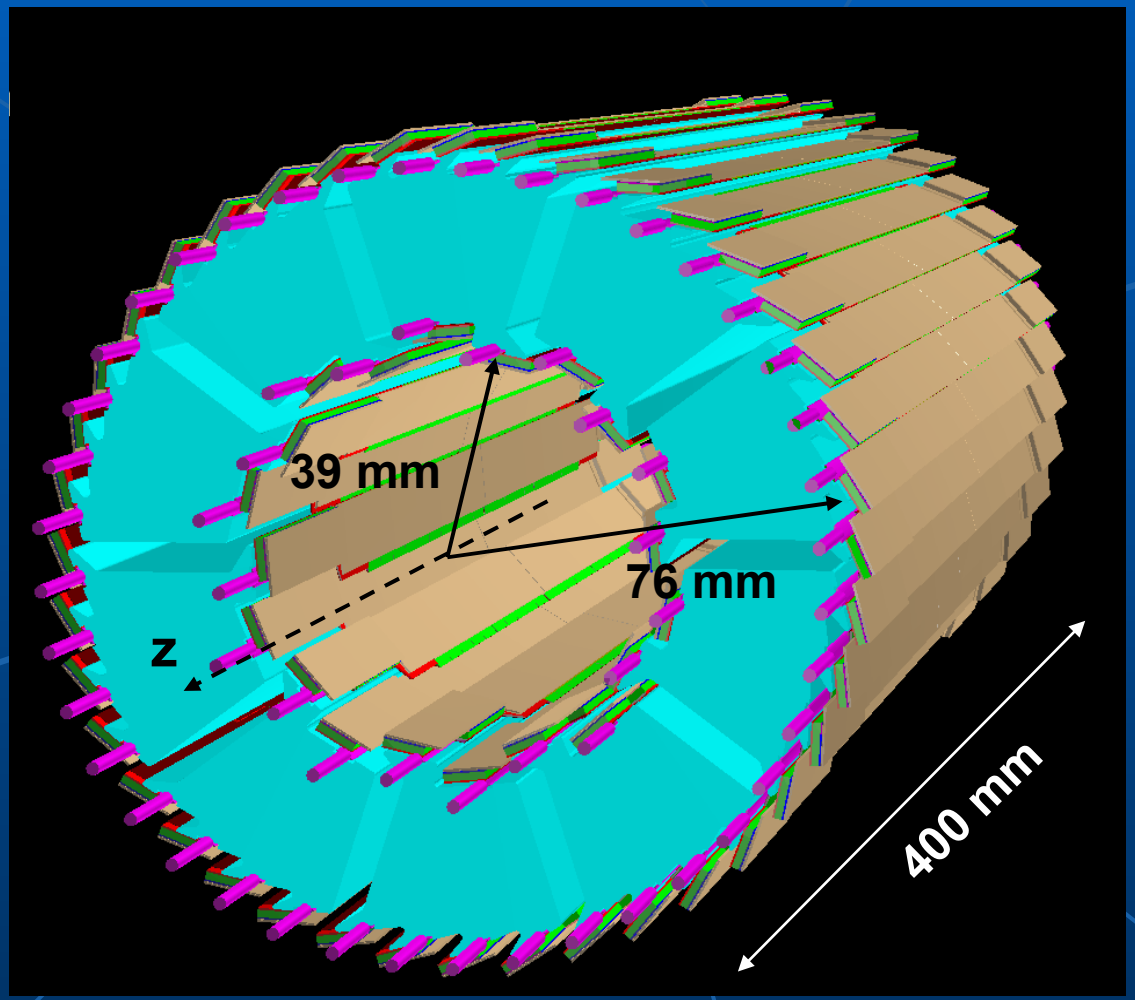
On behalf of the ALICE Silicon Pixel Detector Team

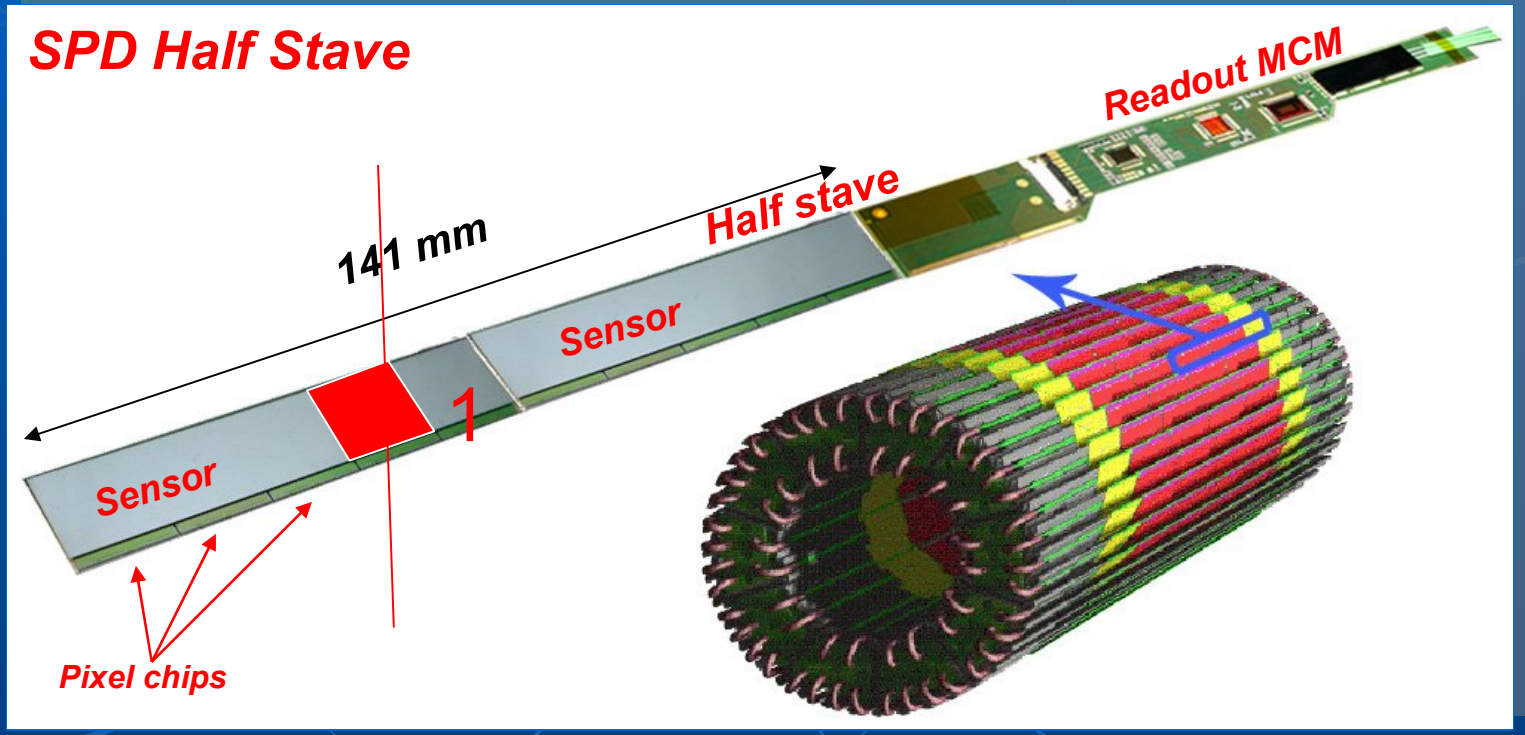
Outline

- ALICE Silicon Pixel Detector
  - FastOR circuit
- The Pixel Trigger System
  - Requirements
  - Implementation
- Commissioning and operating experience

ALICE Silicon Pixel Detector

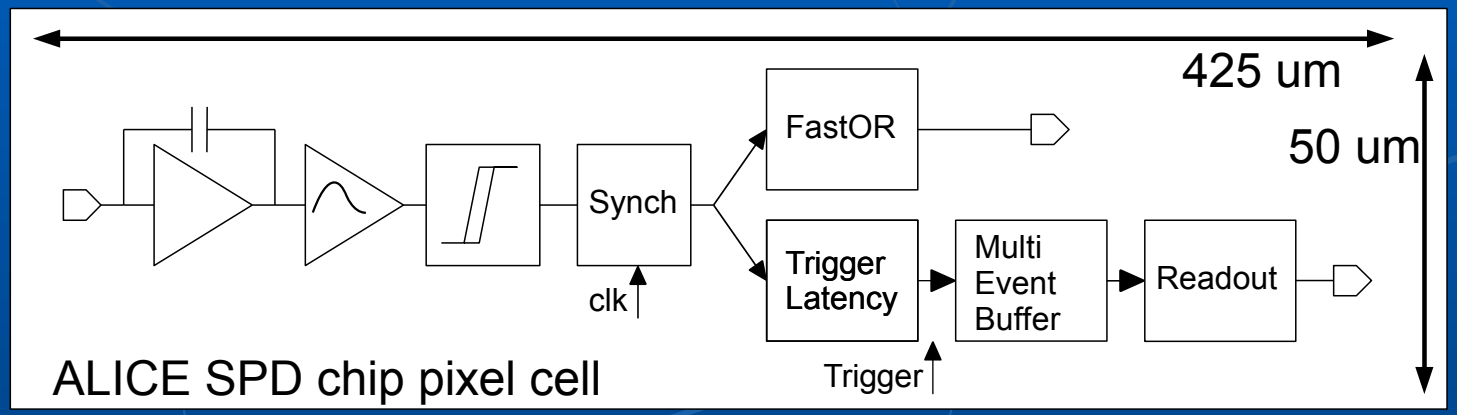


FastOR signals



- Front end chip provides prompt FastOR
  - Active if at least one pixel in the chip is hit
  - Transmitted every 100 ns
    - 10 FastOR bits transmitted on each readout fiber
    - 120 fibers * 10 * 10 MHz = 12 Gb/s

Front end pixel circuit

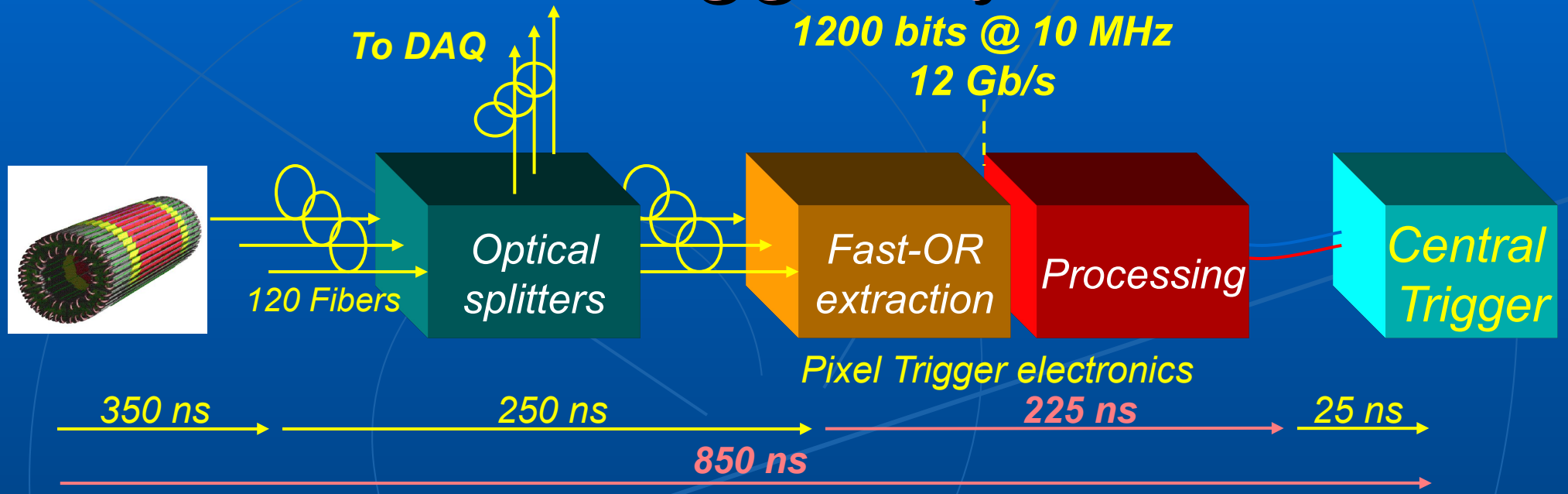


- Dedicated FastOR circuitry follows synchronizer
- Two data streams
  - High resolution pixel detector
  - Low latency PAD detector
    - 1200 pads of 13x14 mm^2

ALICE first level trigger with pixels

- Pre-process low latency Fast-OR and generate primitives for the Level 0 trigger decision
  - Proton-proton
    - Minimum bias
    - High multiplicity trigger
    - Topological trigger (jets)
  - Heavy ions
    - Selection of impact parameter
- Algorithms
  - Boolean functions of 1200 bits
    - Look up tables
  - Occupancy (multiplicity)

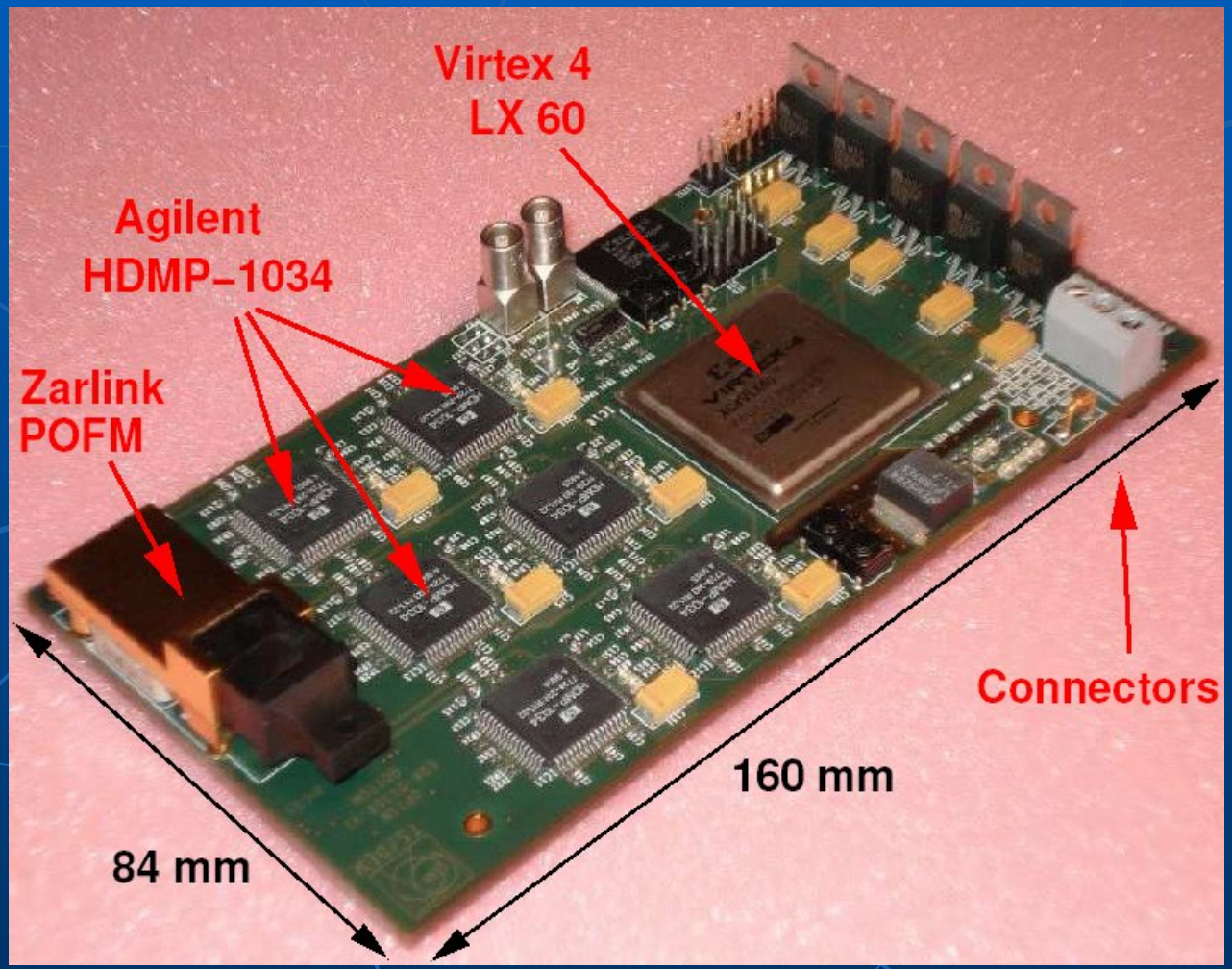
Pixel Trigger system



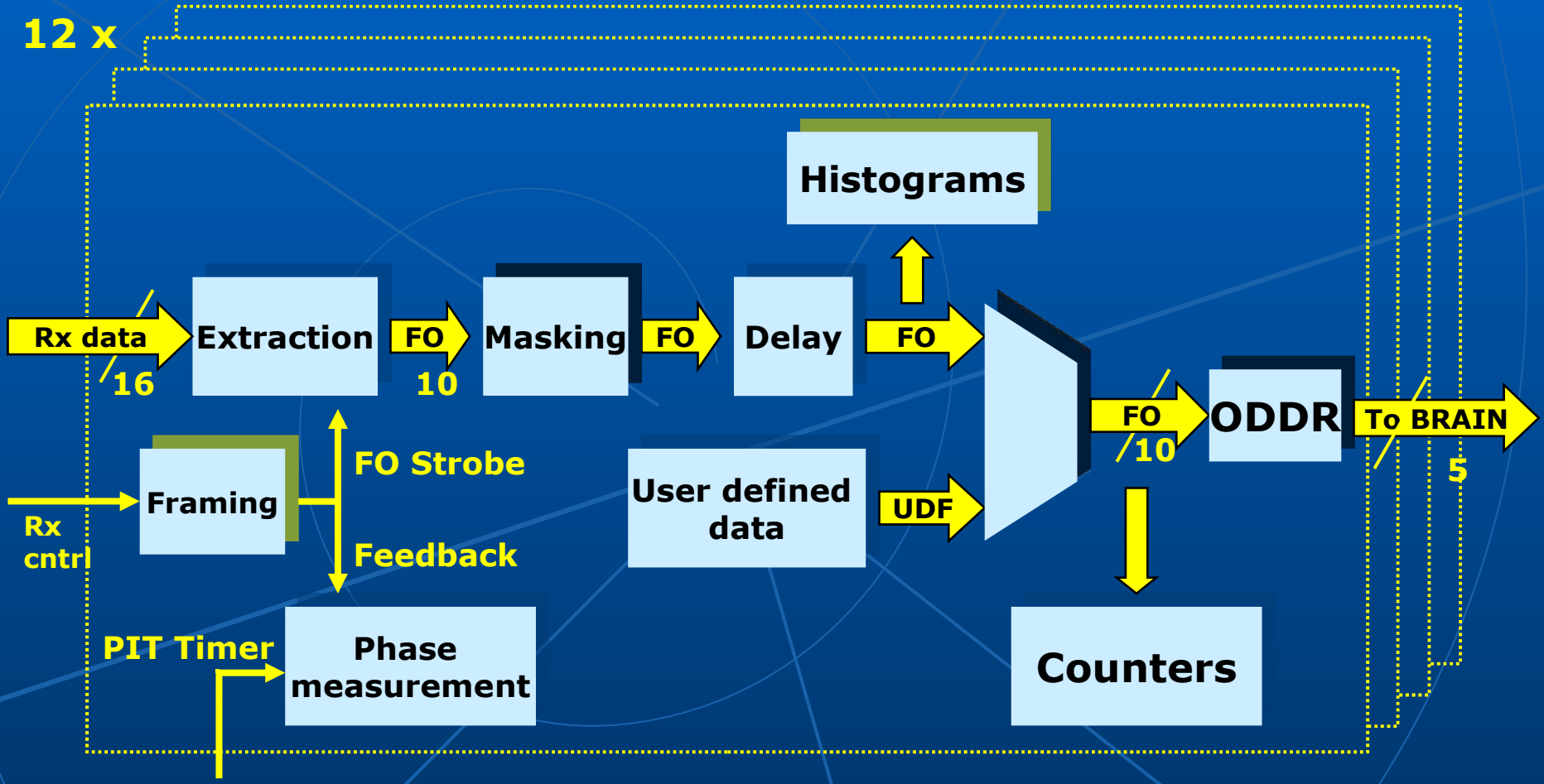
- Extract and synchronize 1200 FastOR bits every 100 ns
- Process algorithm
  - User defined and programmable
- Transmit result
  - Overall latency **850 ns**
  - Bottleneck is deserialization
- Independent from the data readout electronics
- Space constraint (one 9U crate)

Receiver board - OPTIN

- 12 Channels
  - Custom Parallel Optical Receiver Module
  - 12 G-Link deserializer ASICs closely packed
  - FPGA (60k logic cells)

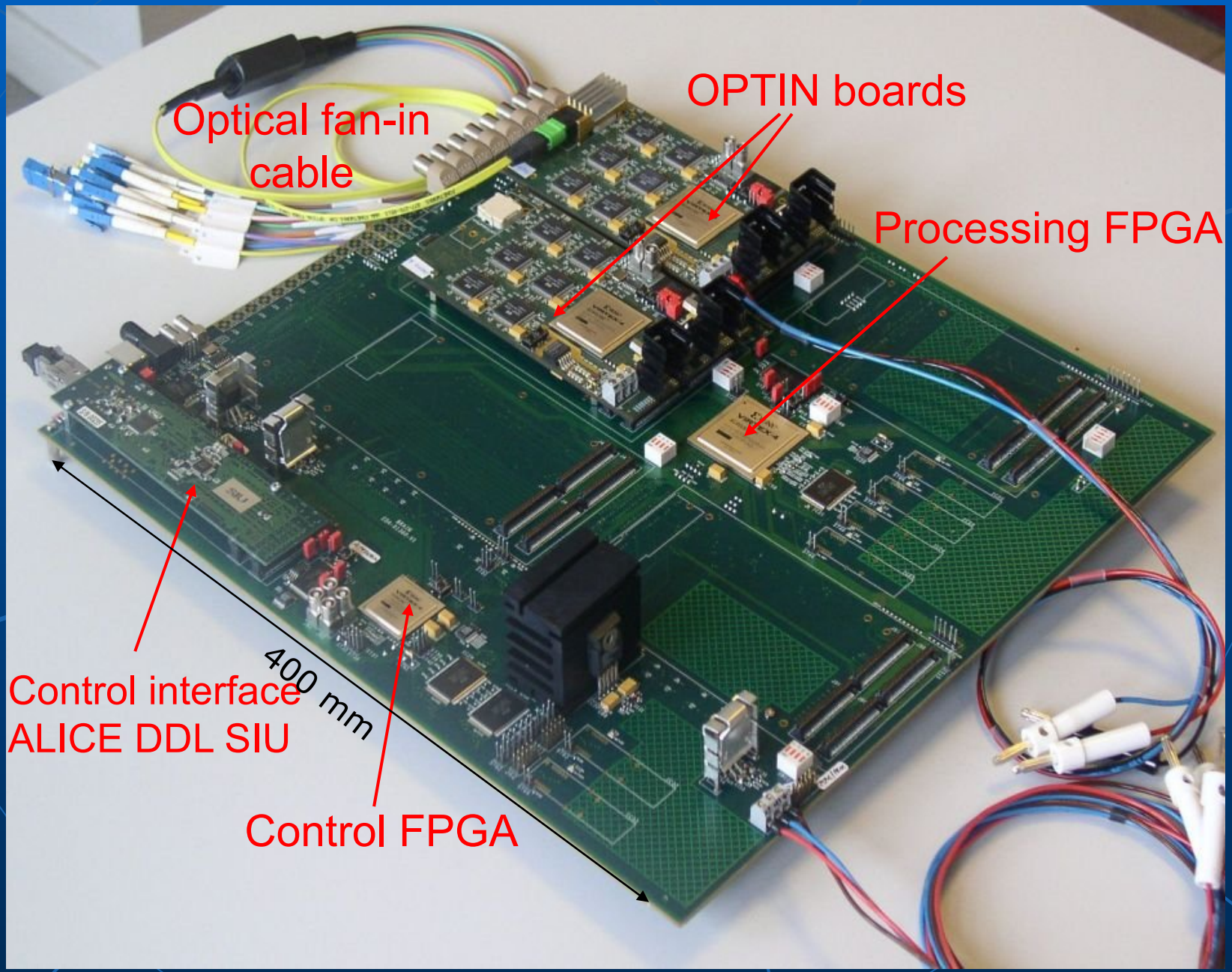


OPTIN board channels

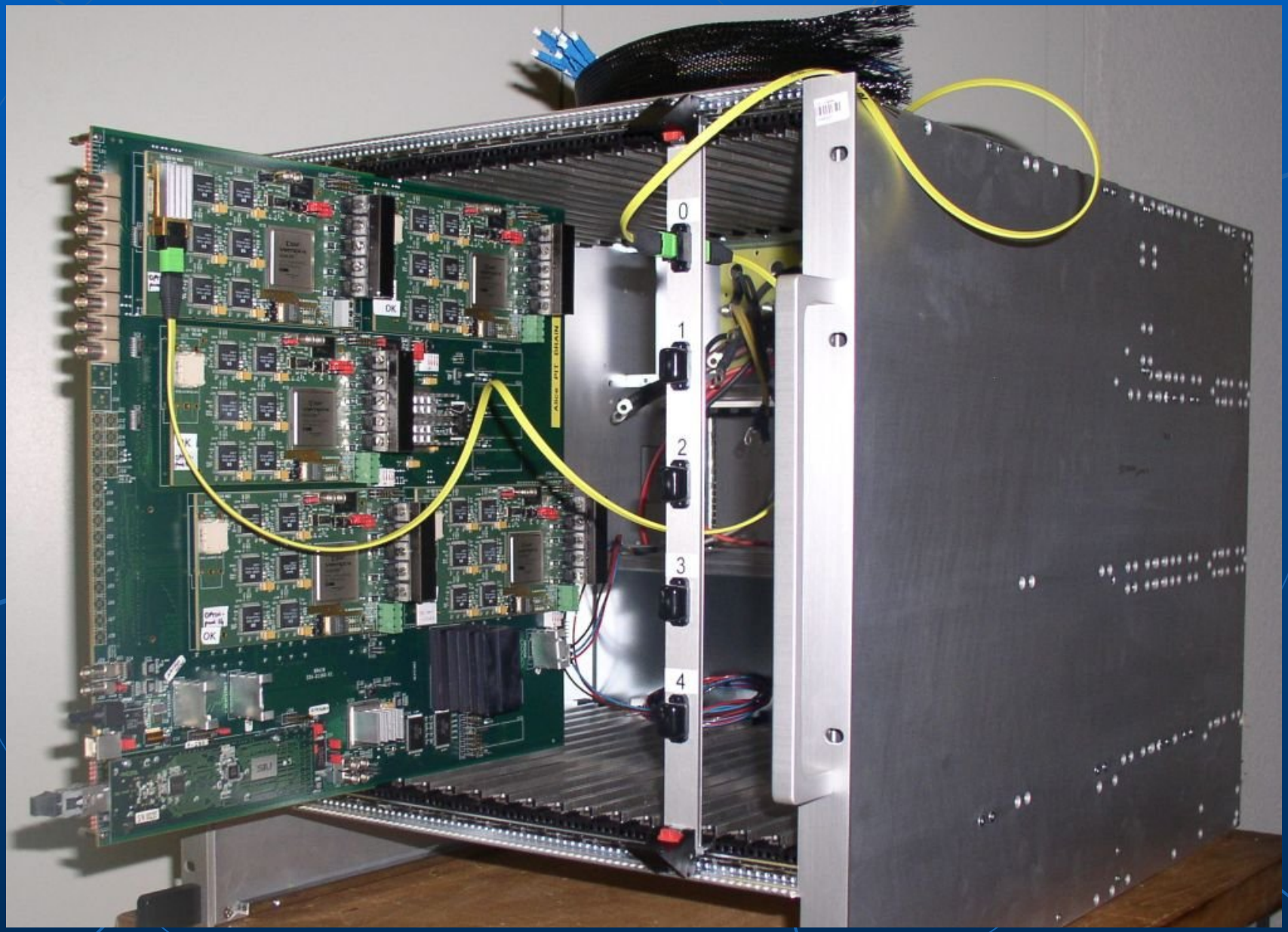


- FastOR extraction, masking, time alignment
- Data quality checks: counters and histograms

Processing board - BRAIN

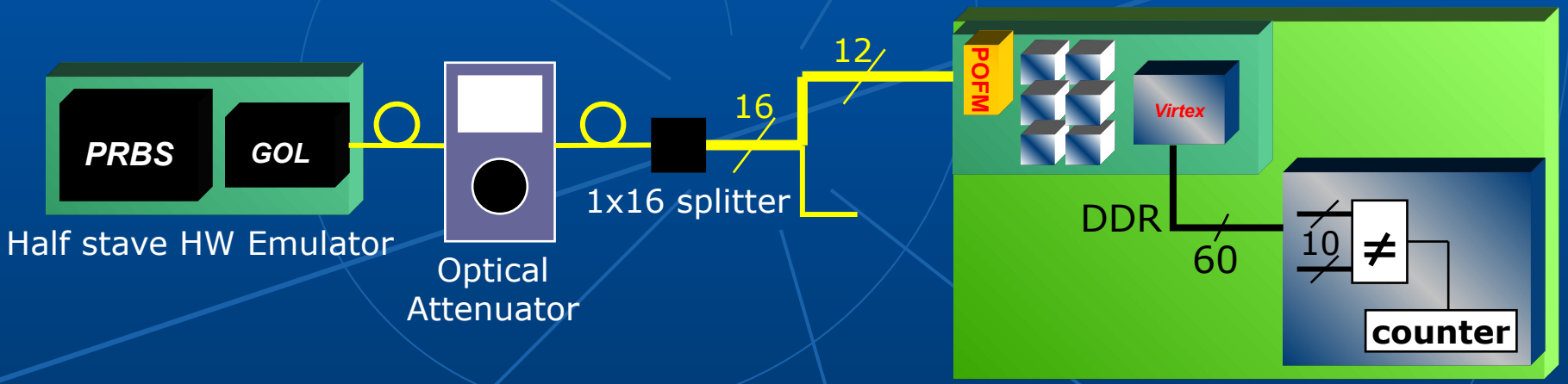


Pixel Trigger System crate



Data path Bit Error Rate Tests

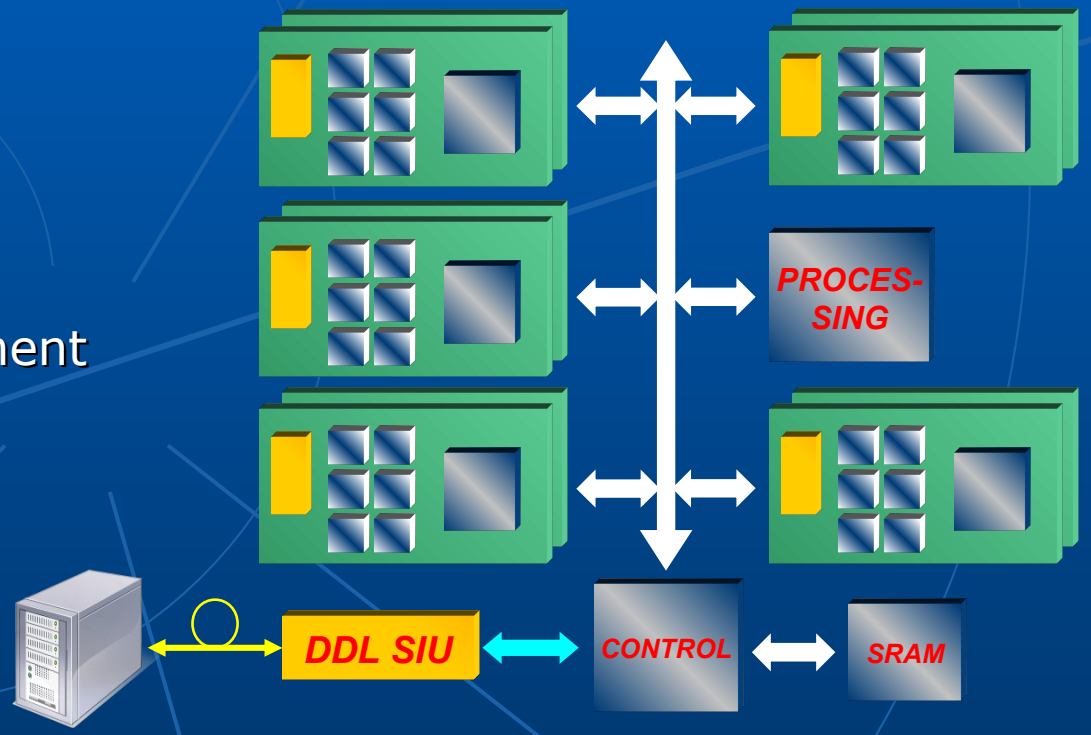
- Full Fast OR data path Bit Error Rate test
  - 12 channels in parallel, pseudo random data
  - Optical power: -18.5 dBm, 0.5 dBm margin



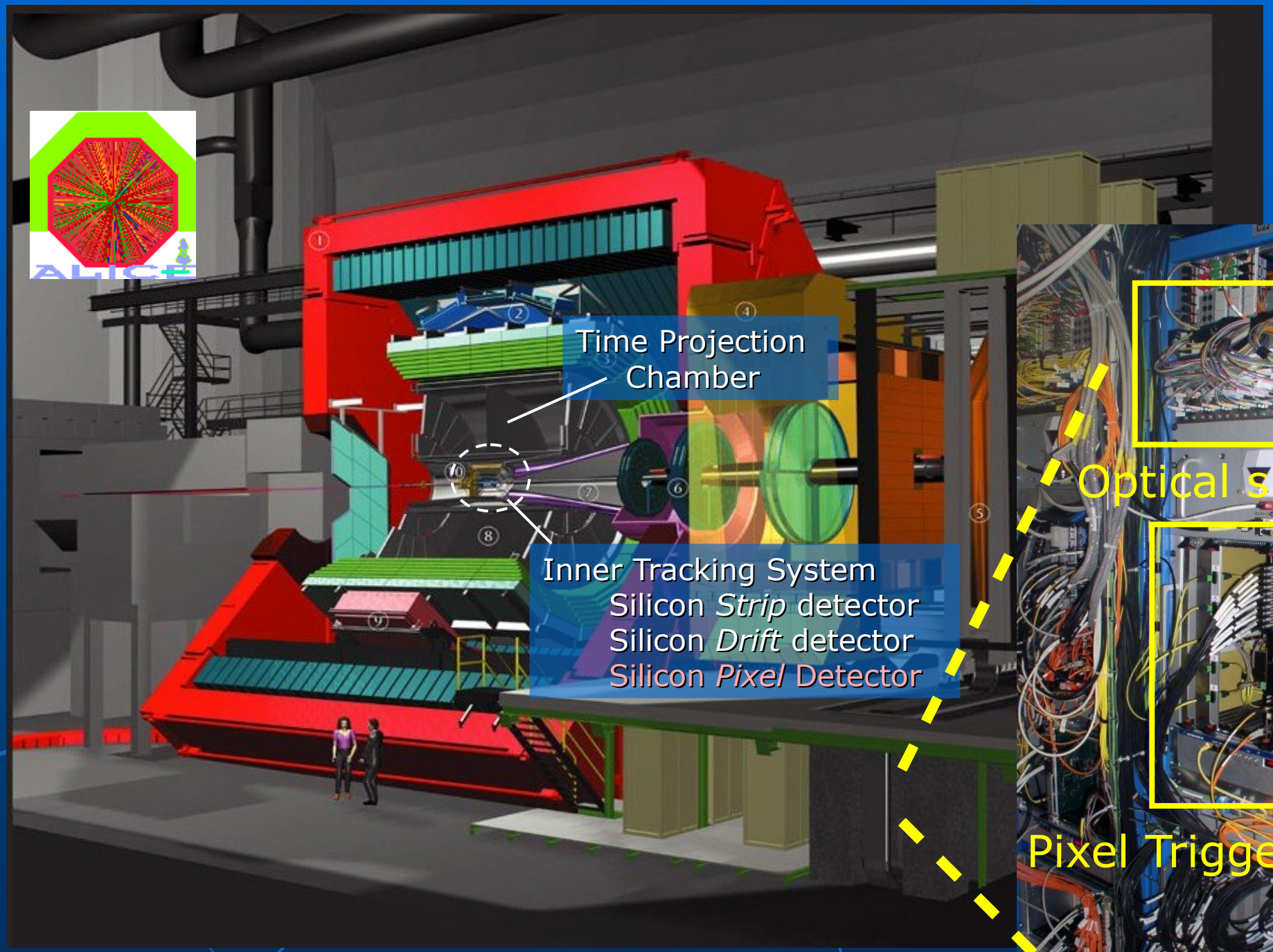
	Duration	N_{bits}	Errors	BER (99% c. l.)
Typical	1.5 hrs	$5.7 \cdot 10^{12}$	0	**$< 8.1 \cdot 10^{-13}$**
Max	17.8 hrs	$7.7 \cdot 10^{13}$	0	**$< 6 \cdot 10^{-14}$**

Pixel Trigger System control

- Custom control interface
  - ALICE Detector Data Link
  - Inter board parallel bus
- Reliability
  - Transaction acknowledgement
  - Parity checking

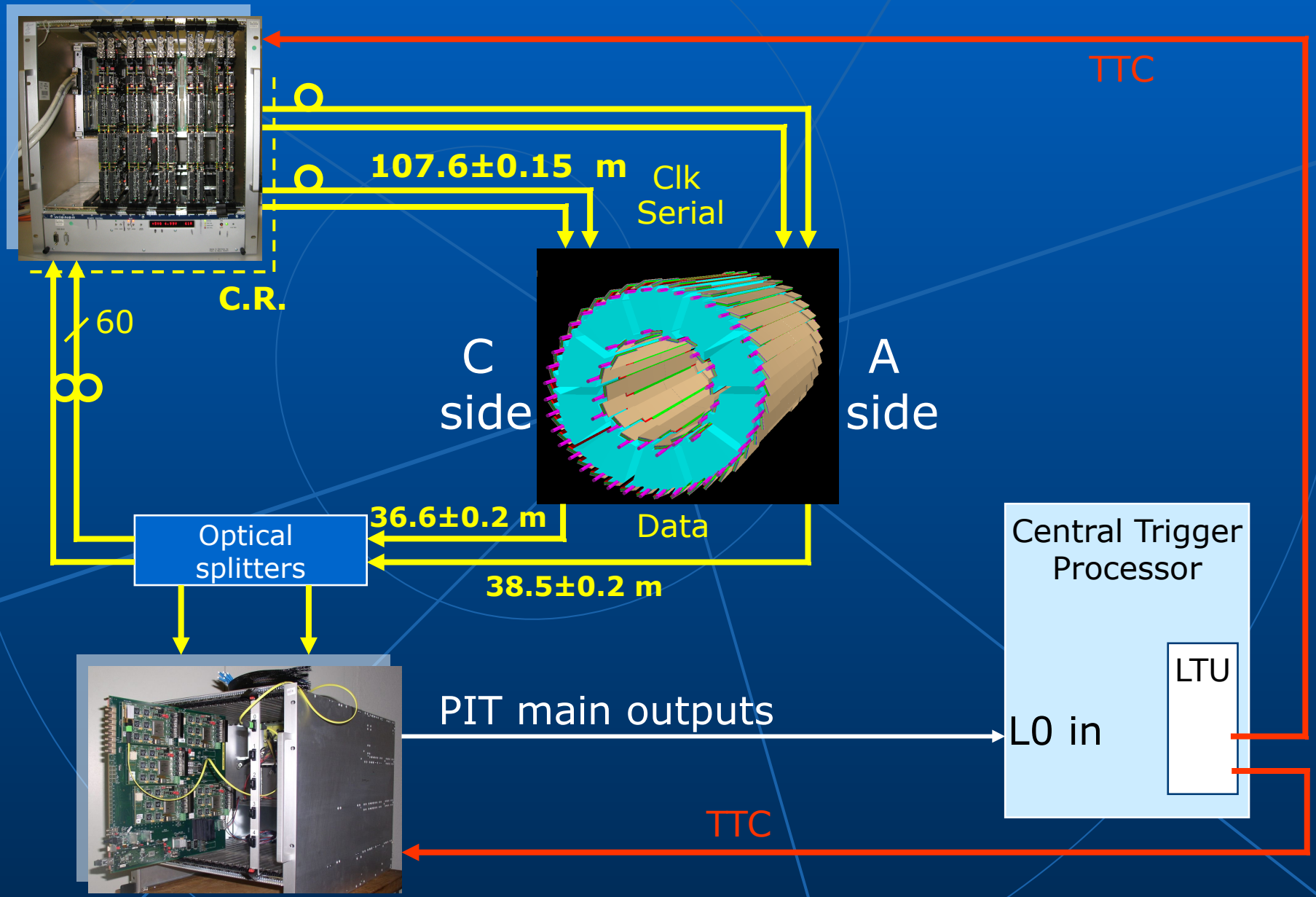


- Read/write test of pseudo random data blocks
  - Typical duration: 15 mins, ~$6*10^8$ bits exchanged, 0 errors
  - Longest: 12 hrs, ~$3*10^{10}$ bits, 0 errors


Time Projection Chamber
Inner Tracking System
Silicon *Strip* detector
Silicon *Drift* detector
Silicon *Pixel* Detector

Optical splitters
Pixel Trigger crate

Installation in ALICE experiment



Algorithms available (now)

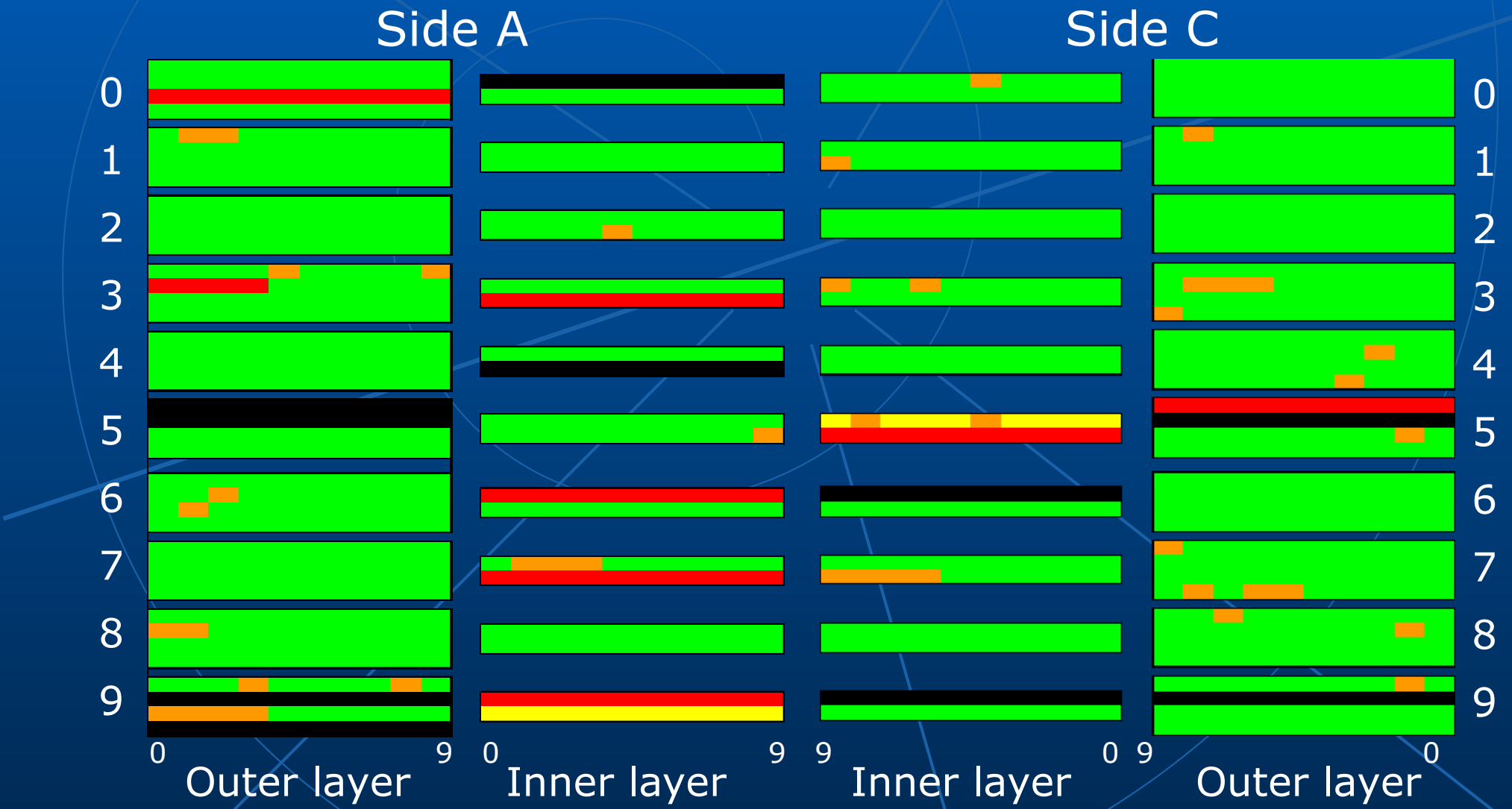
1	Minimum Bias	$(I+O)\geq th_{IO,mb}$ *and* $I\geq th_{I,mb}$ *and* $O\geq th_{O,mb}$
2	High Multiplicity 1	$I\geq th_{I,hm1}$ *and* $O\geq th_{O,hm1}$
3	High Multiplicity 2	$I\geq th_{I,hm2}$ *and* $O\geq th_{O,hm2}$
4	High Multiplicity 3	$I\geq th_{I,hm3}$ *and* $O\geq th_{O,hm3}$
5	High Multiplicity 4	$I\geq th_{I,hm4}$ *and* $O\geq th_{O,hm4}$
6	Past Future Prot	$(I+O)\geq th_{IO,pfp}$ *and* $I\geq th_{I,pfp}$ *and* $O\geq th_{O,pfp}$
7	Background(0)	$I \geq O+ offset_I$
8	Background(1)	$O \geq I+ offset_O$
9	Background(2)	$(I+O) \geq th_{(I+O),bnd}$
10	Cosmic	*Selectable coincidence*

FastOR circuit calibration

- FastOR circuit requires tuning of 5 DACs for correct operation (on each chip)
  - Maximize sensitivity
  - Minimize noise
- Developed experience
  - Large parameter space
- Automatic calibration procedure in place
  - Scans of DAC values
  - Measurement of signal rates
  - Coordinated operation of the SPD Readout, Control and Pixel Trigger systems

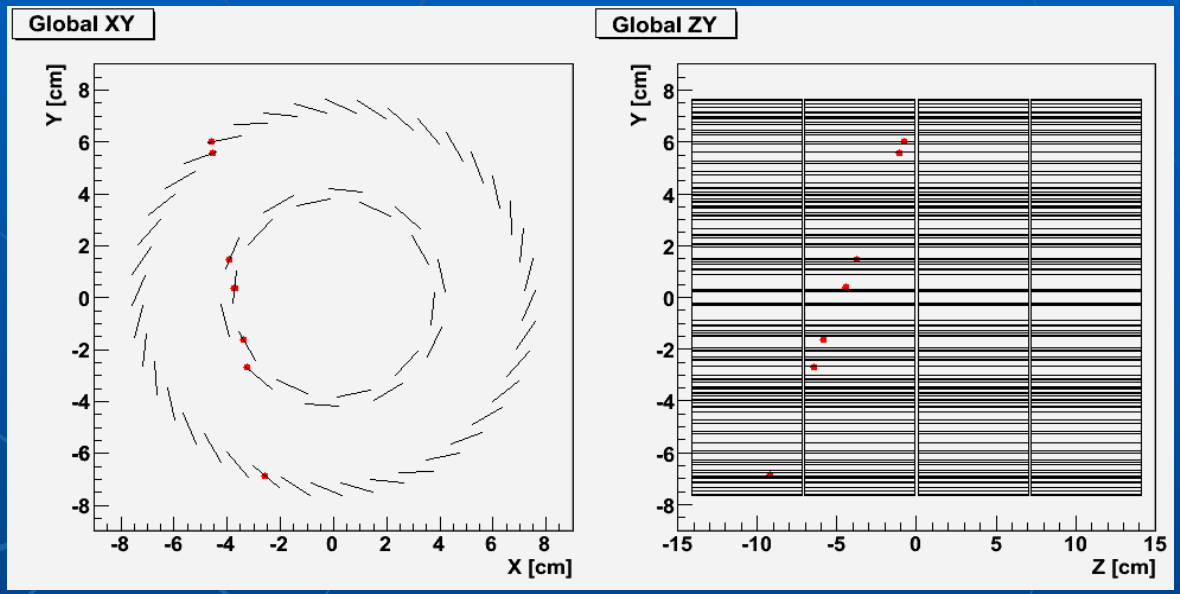
Calibration status summary

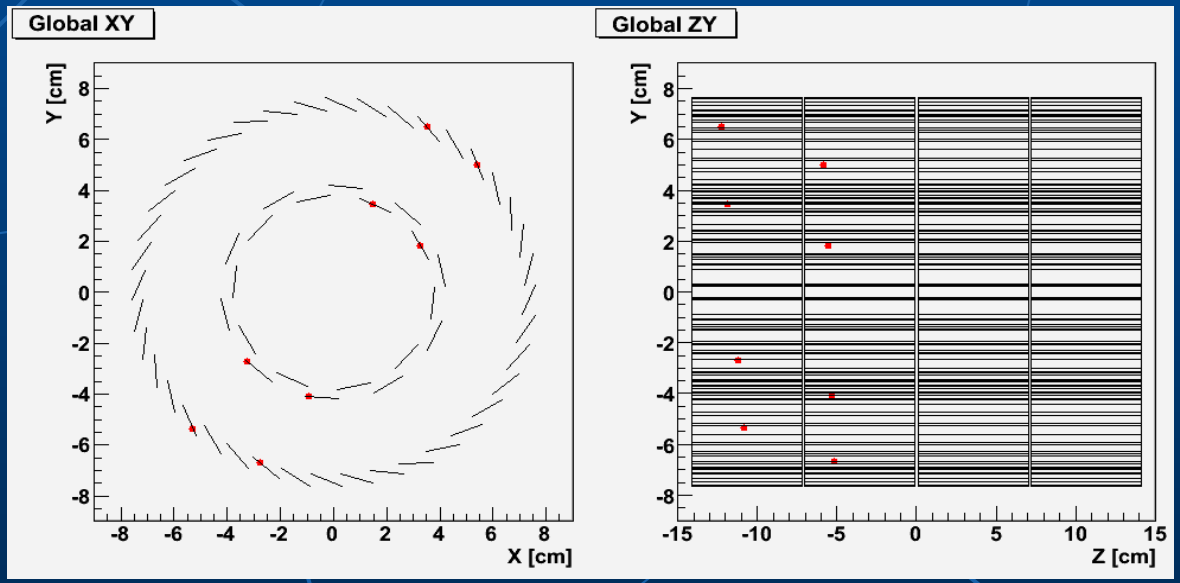
- Tuned Half Staves
  - 103/120 (86%)
- Tuned chips
  - 987/1030 (95.8%)



Cosmic radiation in the cavern

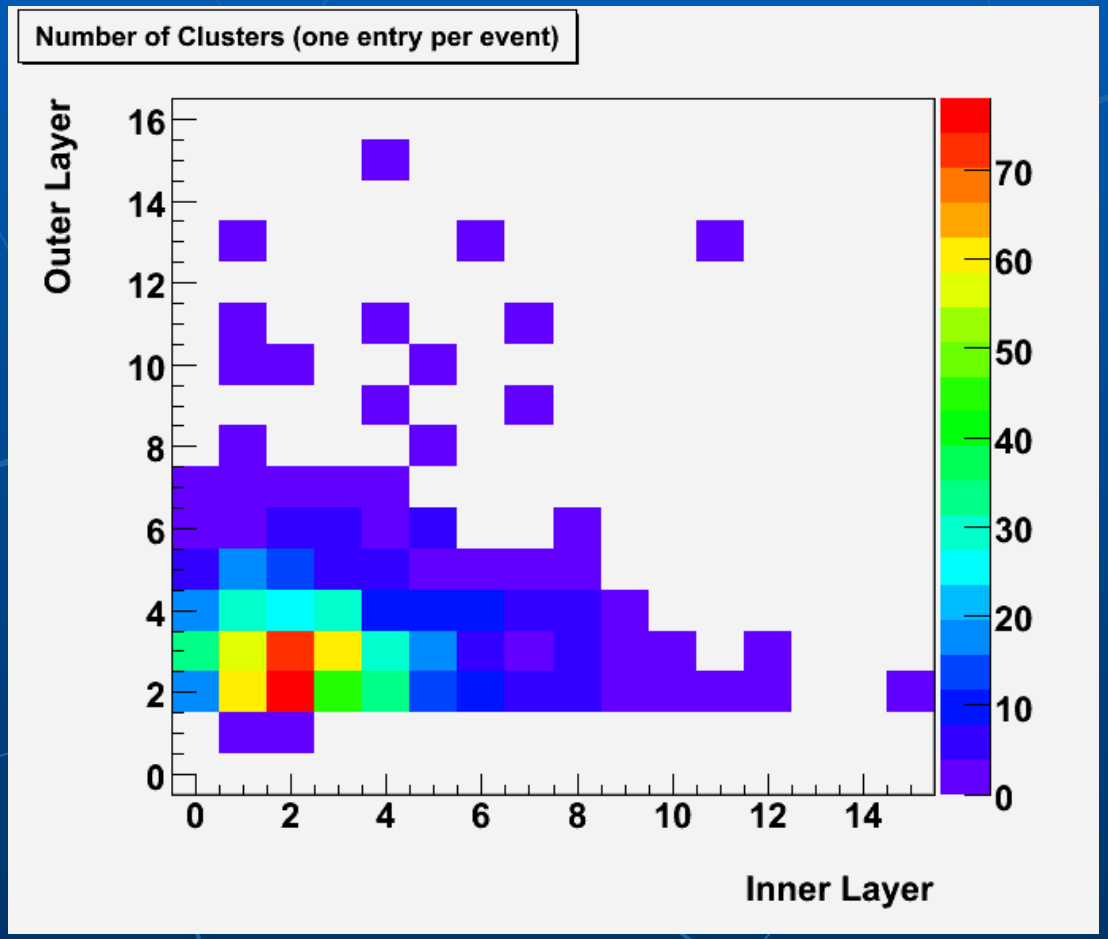
- Pixel Trigger extensively used during ALICE commissioning with cosmic data
  - SPD only
  - Inner Tracking (SPD+SSD+SDD)
  - ITS, TPC, TOF, ECAL
- Alignment data
  - 10^5 events > 3 SPD clusters
  - Showers





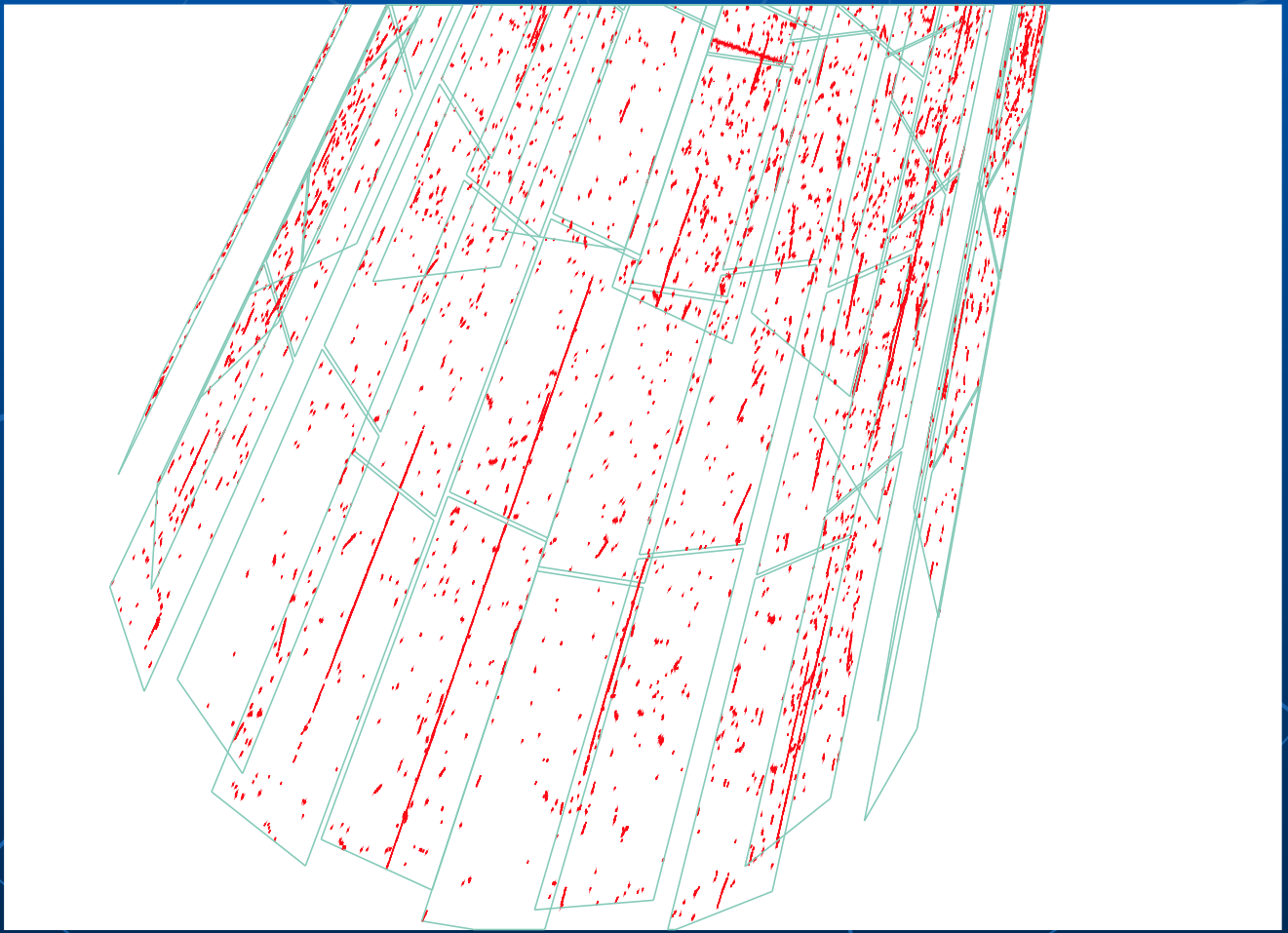
Cosmic data

- High efficiency
  - Rate 0.18 Hz
    - In agreement with the muon flux measured in the cavern and with Monte Carlo
- Very high purity
    - 99.5% of events with at least two clusters on the outer layer, as demanded by the coincidence

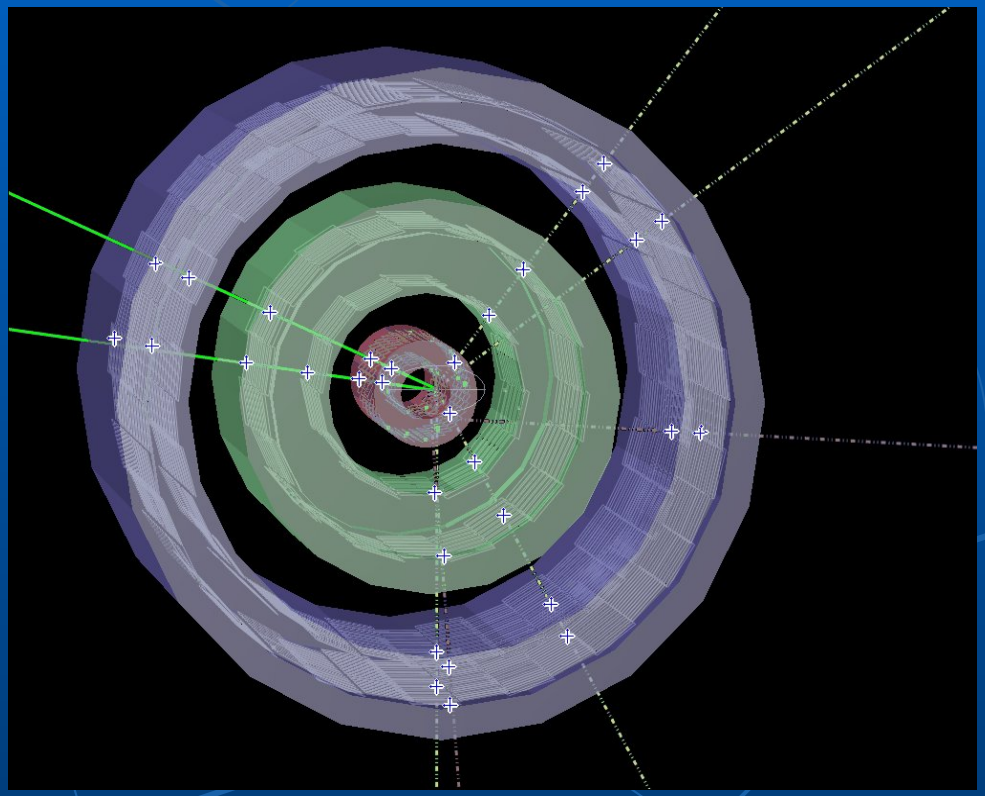


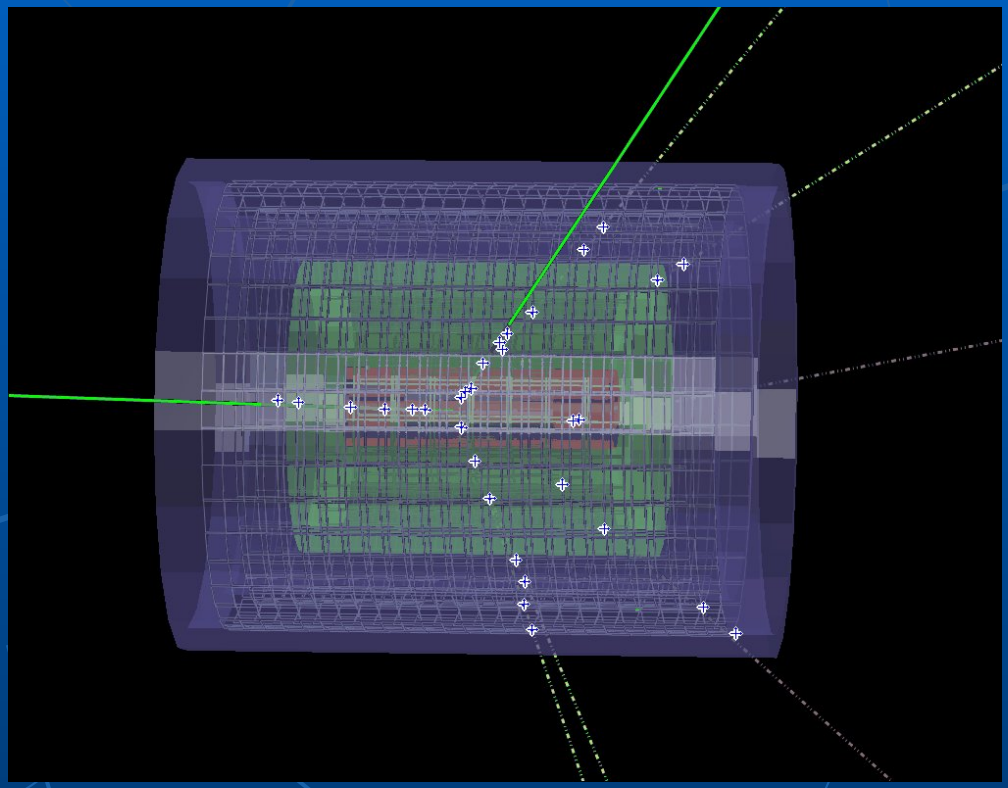
LHC beam injection tests

- August 2008: ALICE SPD was recording data self-triggering via the Pixel Trigger System
- The first “LHC related particles” were detected



Beam events





- Events from LHC circulating beam
  - 11th September 2009

Some lessons learned

- Self triggering functionality of Pixel FE chips proves extremely useful
  - Testing and commissioning
  - System
  - Experiment advanced trigger logic
- Different circuit solutions possible
  - Binary, digital, analog, charge threshold...
- Large bandwidth real time processing on FPGAs
  - Location of processing electronics
  - System implications: trigger latency

Summary

- The ALICE Pixel Trigger system allows to include the prompt FastOR outputs of the Silicon Pixel Detector in the Level 0 trigger decision
  - ALICE is the only LHC experiment including the vertex detector in the first trigger decision from startup
- The Pixel Trigger system
  - Installed and operational
  - Board level and system level challenging requirements
  - Highly compact solution including original developments
  - Commissioning and operation experience

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- J. Conrad et al., "Minimum Bias Triggers in Proton-Proton collisions with the VZERO and Silicon Pixel Detectors", ALICE Internal note, ALICE-INT-2005-025, 19/10/2005