Time resolved studies of Single Event Upset in optical data receiver for the ATLAS pixel detector

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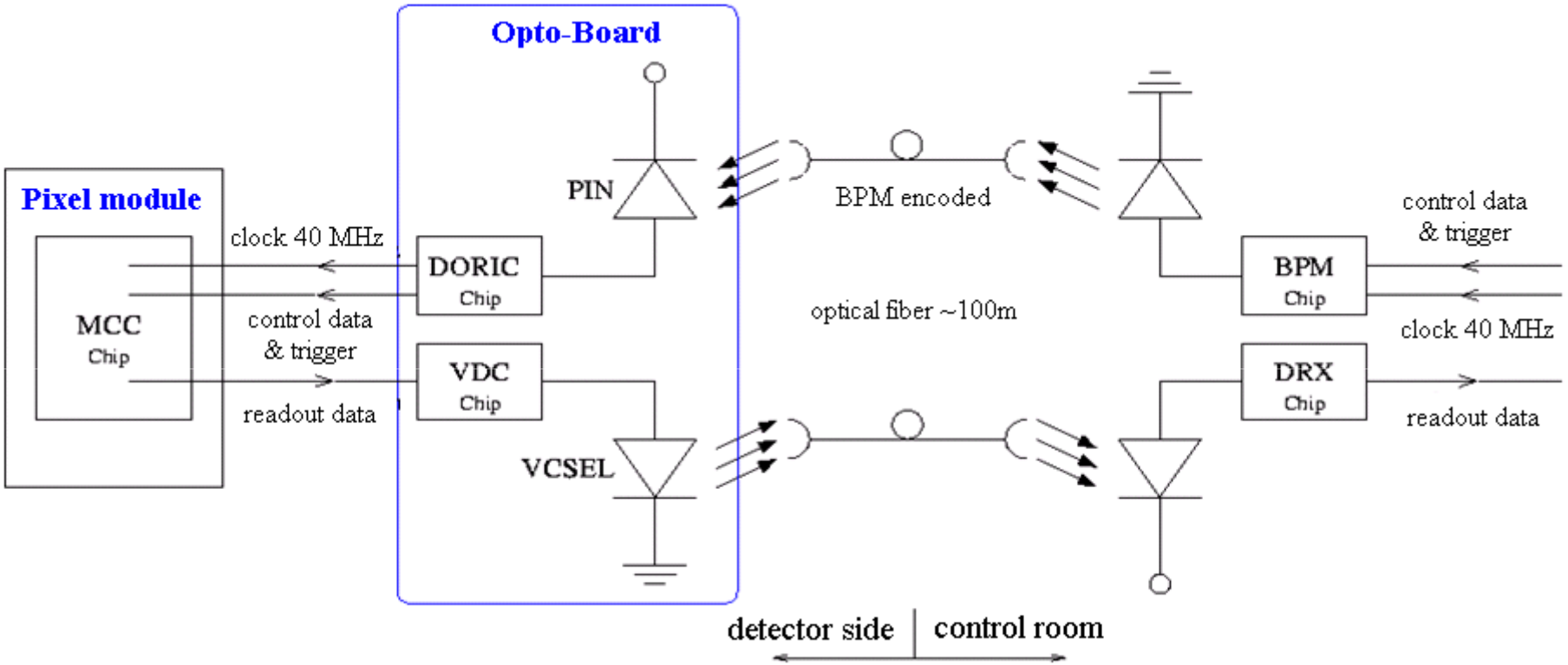
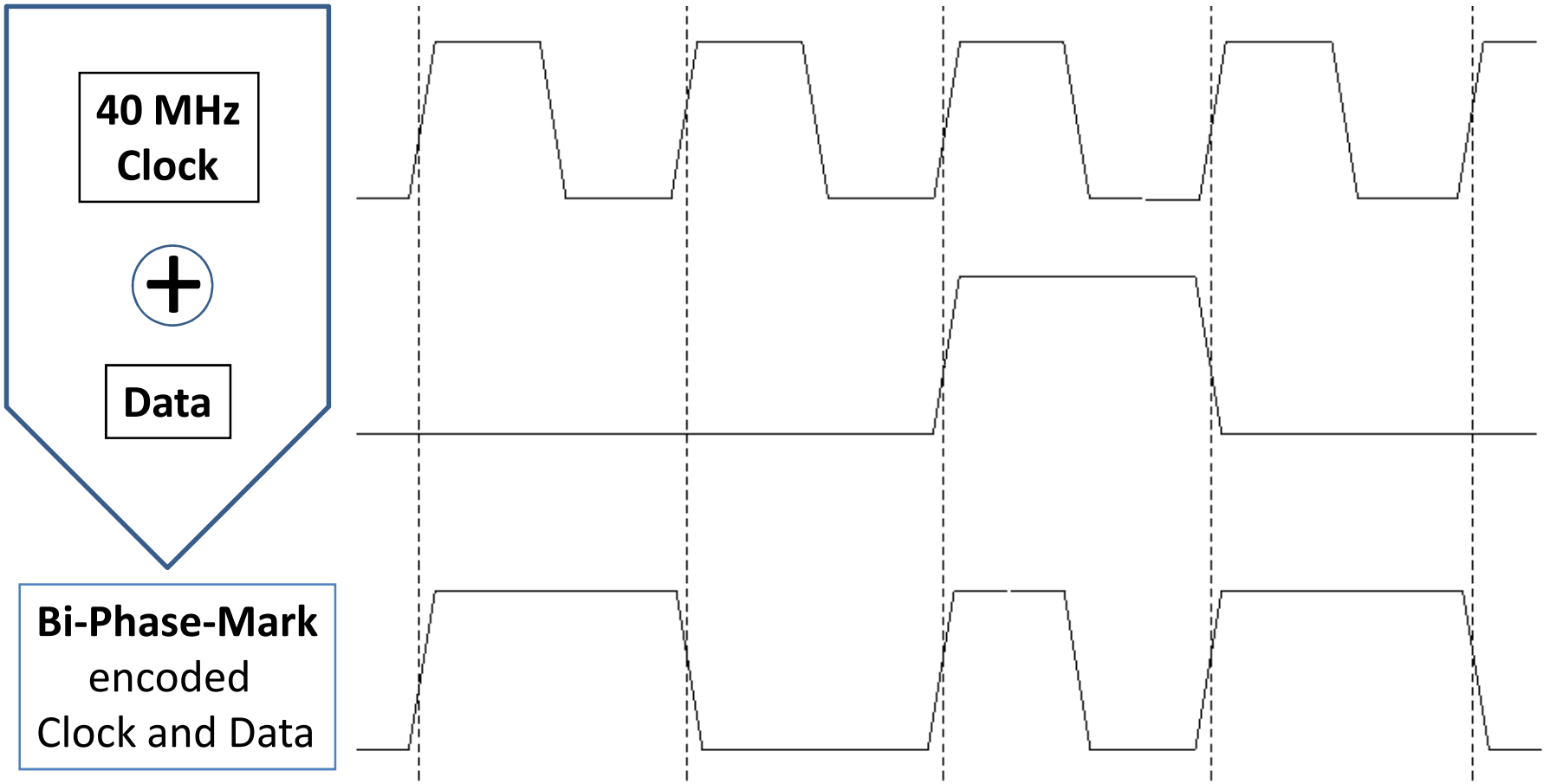
Architecture of Optical Links for ATLAS Pixel Detector



- Light-Receiver:
  PIN: PiN-diode followed by
  DORIC-ASIC (Digital Opto-Receiver Integrated Circuit)
- Light-Emitter:
  VCSEL (Vertical Cavity Surface Emitting Laser)
  driven by VDC-ASIC (VCSEL-Driver-Chip)

Bi-Phase-Mark encoding scheme

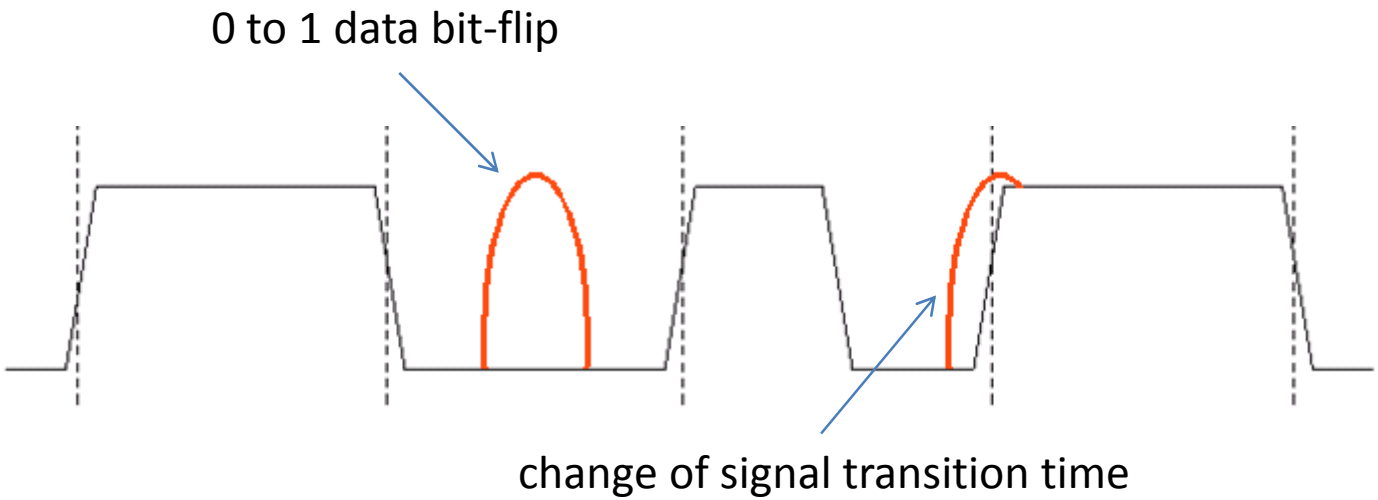


Single Event Upset

The **Single Event Upset (SEU)** is an effect of radiation induced errors in microelectronic circuits when charged particles loose energy by ionizing the medium through which they pass, leaving behind electron-hole pairs.

However, the minimal ionizing particles can not cause a SEU directly. They produce, through collisions with atoms, strong ionizing ions, which in turn produce enough amount of electron-hole pairs to induce an error.

The most sensitive part of the opto-link to the SEU is the **PIN** light detector. The SEU induced charge can cause a data bit-flip transition or change the timing of the signal edges.



Single Event Upset

What is known:

- The SEU Bit Error Rate (BER) as a function of the PIN current (optical power). This dependence was measured in the past on many occasions.
- The expected particle flux at the opto-board location: 2×10^{6} cm^{-2} s^{-1}.

$\Rightarrow$The estimated expected BER induced by SEU at nominal PIN current of 100 µA:

~3 x 10^{-10}

corresponding to **1 bit error in 80 seconds**

- Since the BER for the DORIC ASIC is by factor 30 less (< **10^{-11}**), the opto-link BER is limited by the SEU .

What we want to know:

- Insight into the bit error event structure , by means of recording data bit sequences of SEU occurrence in time and further off-line analyses.

$\Rightarrow$ Conclusions useful for future development of optical receivers.

SEU measurement in August 2009

In August 2009 an irradiation of PIN and VCSEL arrays for pixel IBL project was carried out by OSU group at CERN T7 irradiation facility with 24 GeV/c protons.

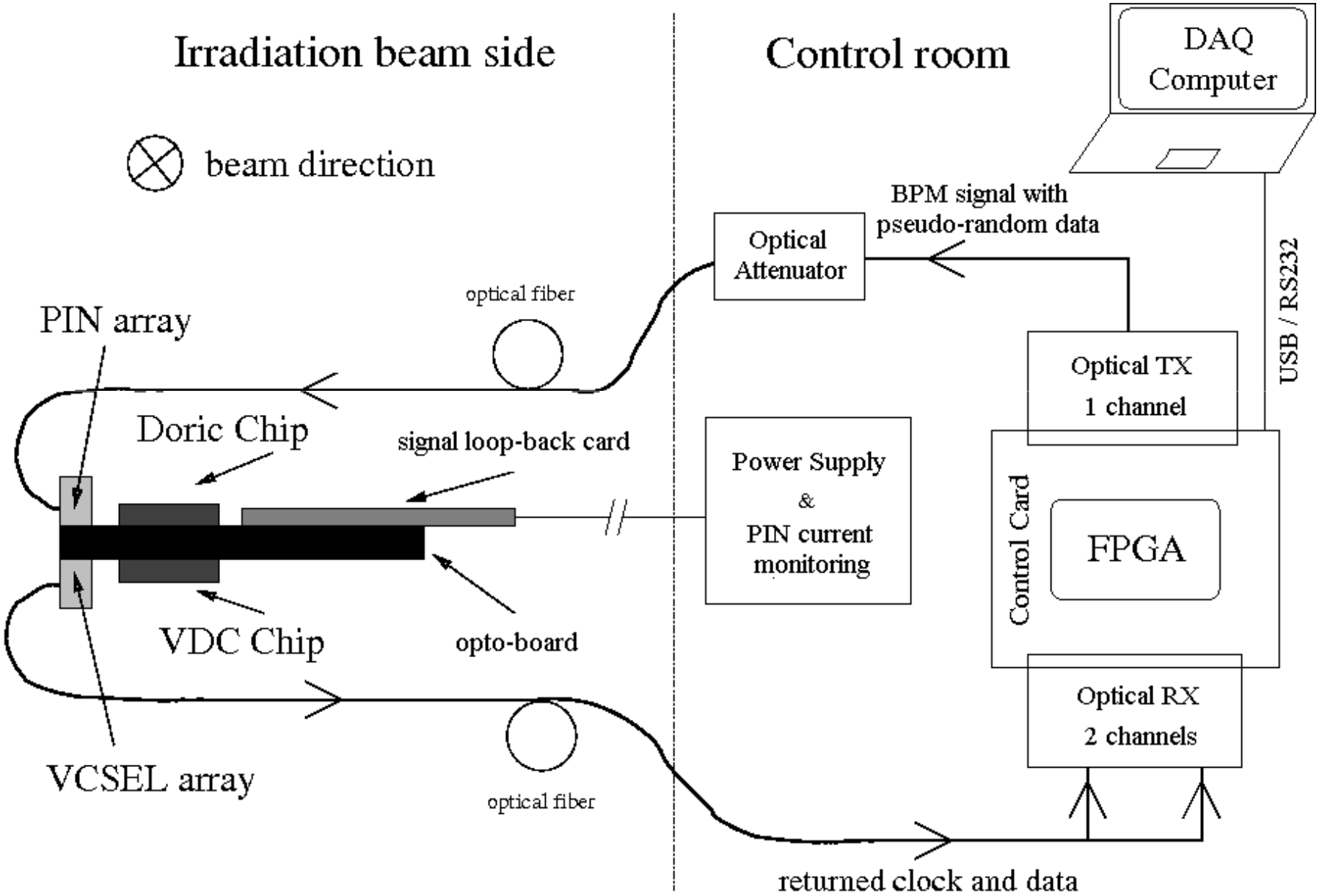
The idea to perform a time resolved SEU measurement in addition was born just few weeks before the irradiation started.

During roughly two weeks time, OSU and Siegen transformed the idea into a real test system by building dedicated opto-boards and developing a compact DAQ system for time resolved SEU measurement.

Nowadays, such prompt acting is possible, thanks to FPGA hardware and flexible VHDL designing tools.

For performing the SEU measurement two hours of beam time were allocated. The effective time spent on it was longer, mainly due to set up and operation related activities.

Experimental setup for SEU measurement



Functionality implemented in FPGA for time resolved SEU measurement

- Pseudo-random data bit generation, 40 Mb/s,
- Bi-Phase-Mark encoding of data with 40 MHz clock,
- SEU event detection by bit comparison for sent and returned data,
- In parallel, checking of returned 40 MHz clock by 80 MSPS sampling,
- Pre storing of data bit sequences for both sent and returned data (64 bit long),
- Pre storing of sampled returned clock (64 cycles long),
- Time stamp generation for each SEU event,
- SEU data formatting,
- Transfer of pre-stored SEU data from FPGA to PC (readout function).

Single Event Upset measurement

We have performed two sets of consecutive measurements on two PIN+Doric channels.

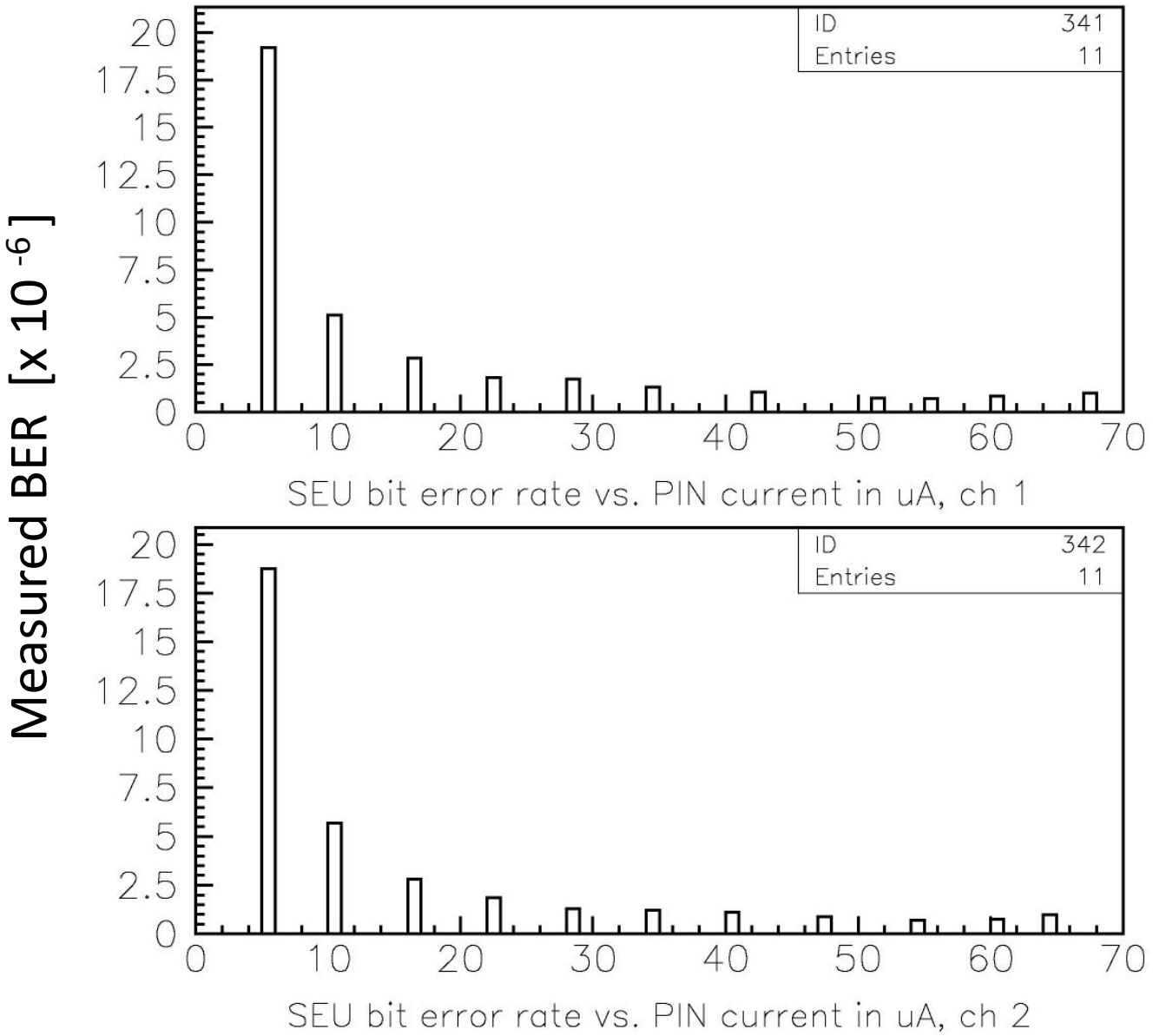
For each channel the SEU data was taken at 11 optical power setting , ranging from ~20 to 250 µW (twice to 25 times above the Doric threshold).

At each optical power setting , the data was recorded for 10 proton bursts , each 400ms long. This corresponds to 100 million pseudo-random data bits sent to opto-board for each optical power setting.

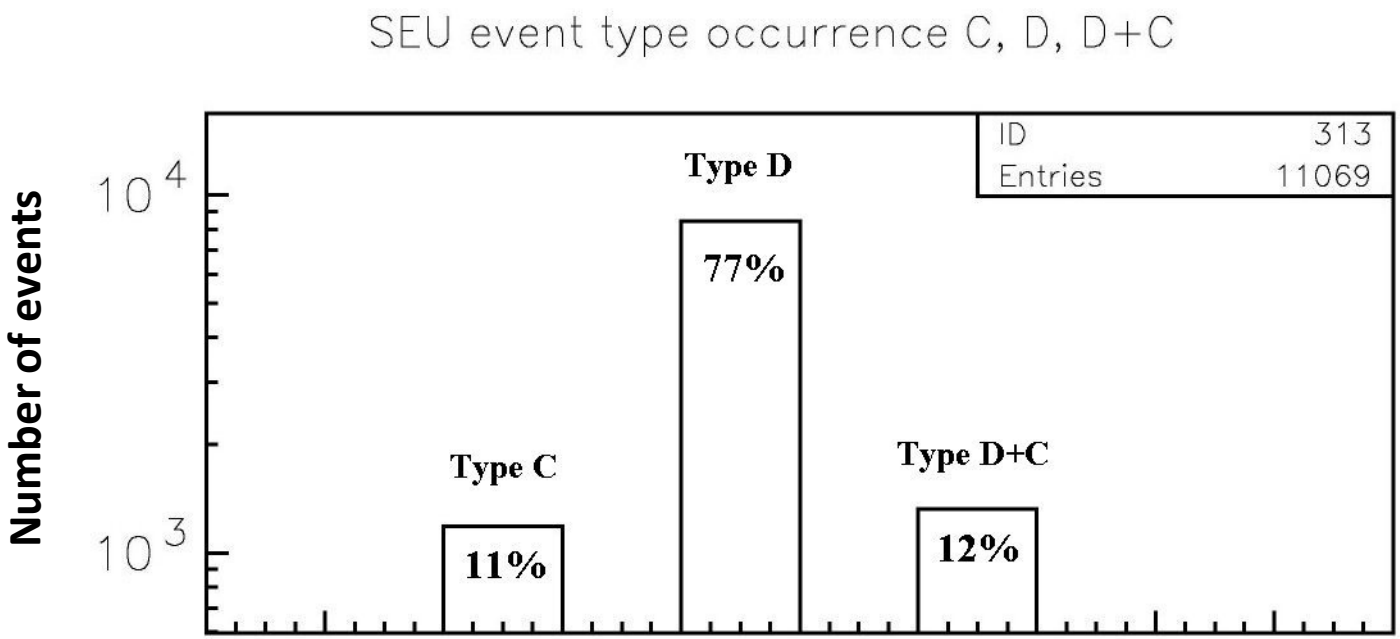
Both the PIN array and the Doric ASIC were exposed to the proton beam of ~1.5 x 1.5 cm^2 size ; the beam was centered at the PIN array itself.

The proton beam flux was ~10^{10} p cm^{-2} sec^{-1} .

Single Event Upset rate measured for two PIN channels



Identified SEU event types



Type C :

with **only clock** disturbed

Type D :

with **only data** bit errors

Type D+C :

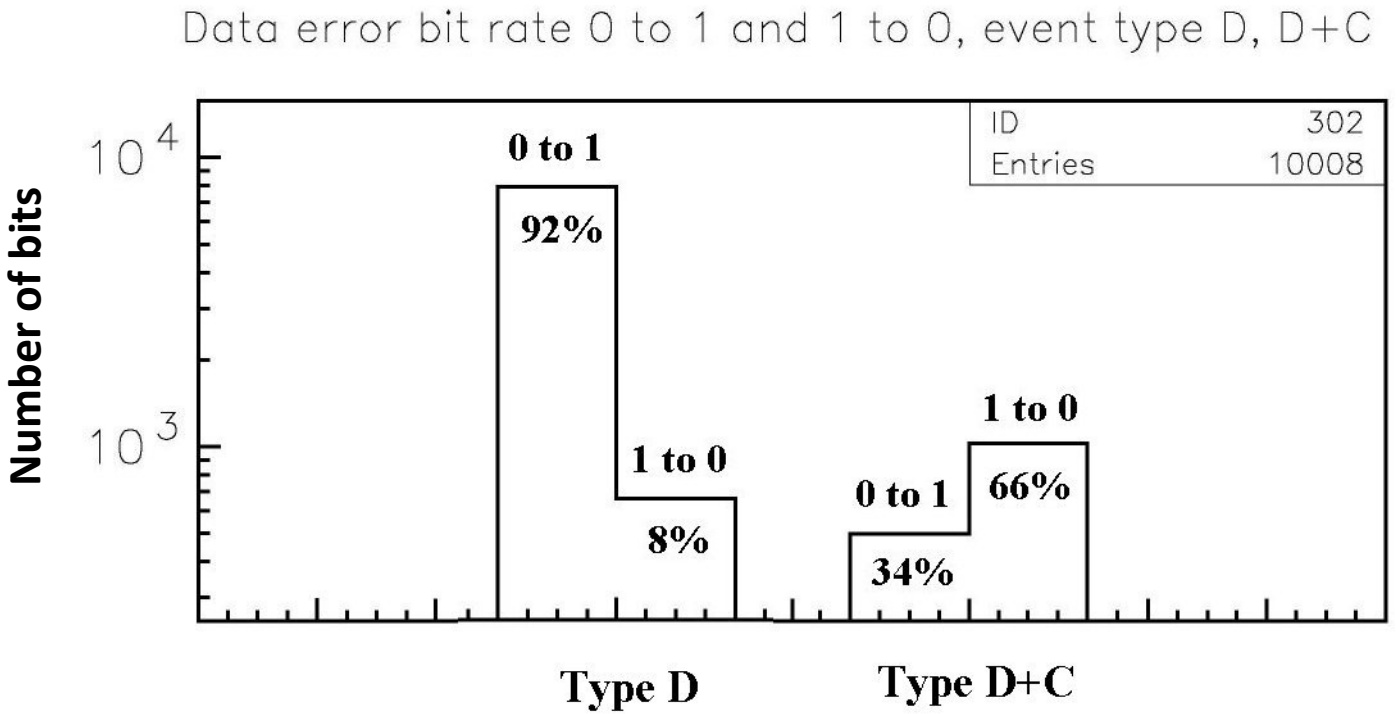
with both **data** bit errors and disturbed **clock**

Data error transitions for SEU type D and D+C

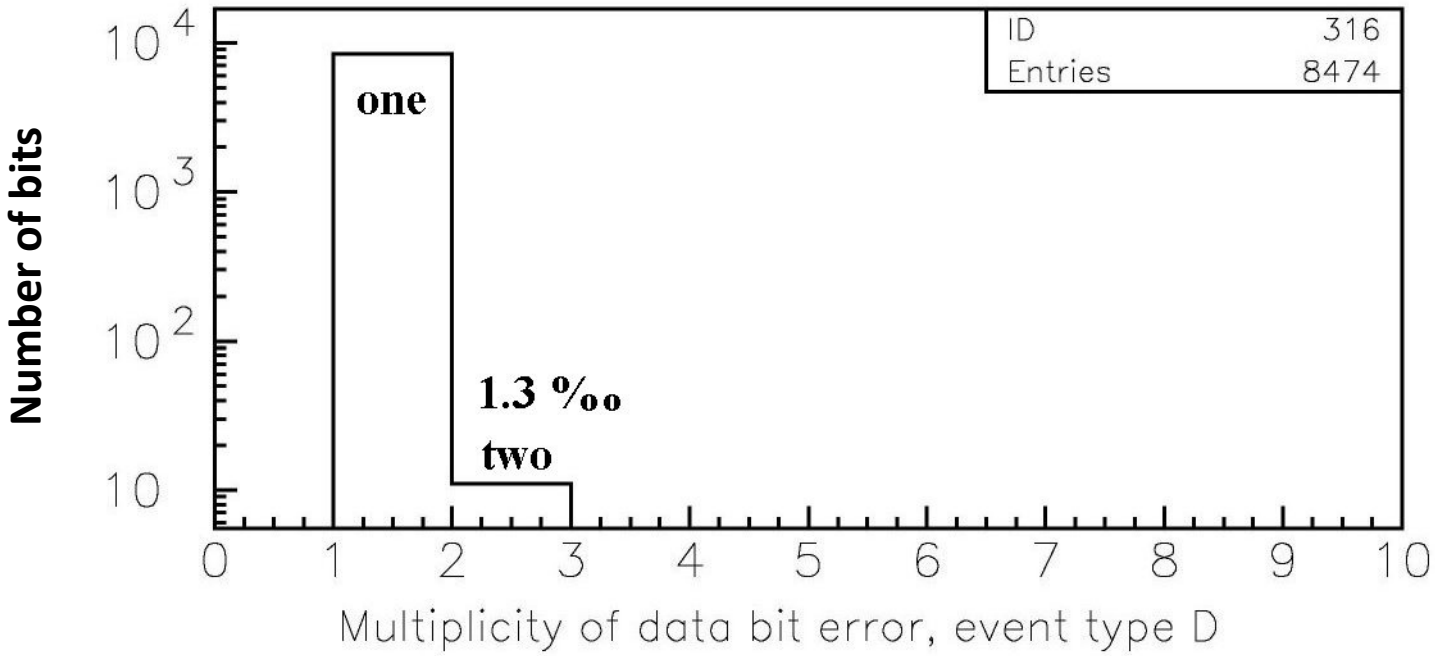
Data bit-flip transition

from **0 to 1** and from **1 to 0**

both possible due to charge deposition in the PIN diode.



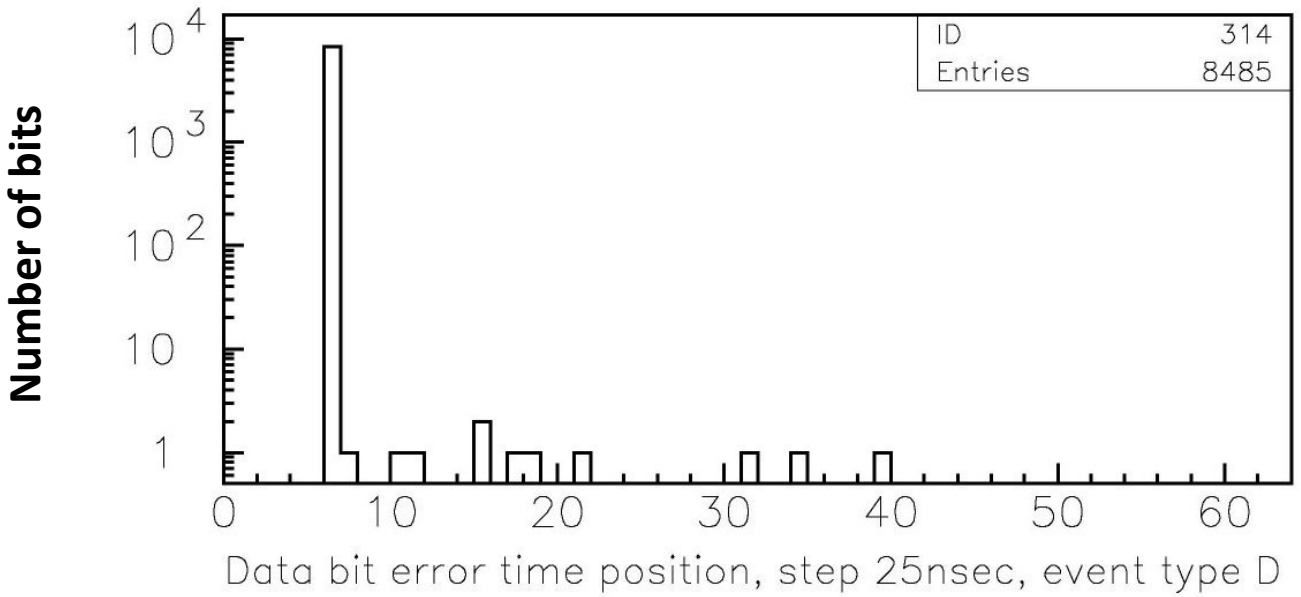
Event type D: data error bit multiplicity



Events of type D almost are exclusively with only one data bit error .

Very rare event occurrence (1.3‰) with two data bit errors (11 events detected).

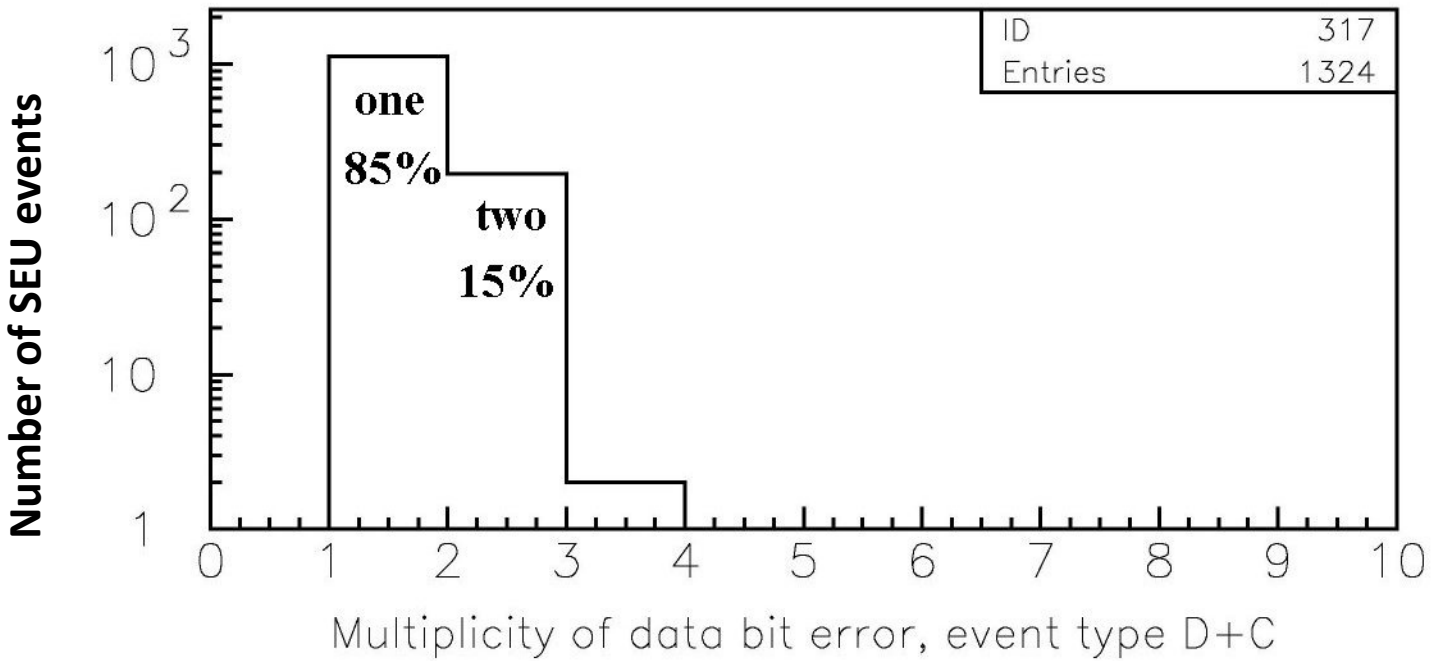
Event type D: data error bit time position



Two-bit data error events are very rare:

they may be induced by a following radioactive decay.

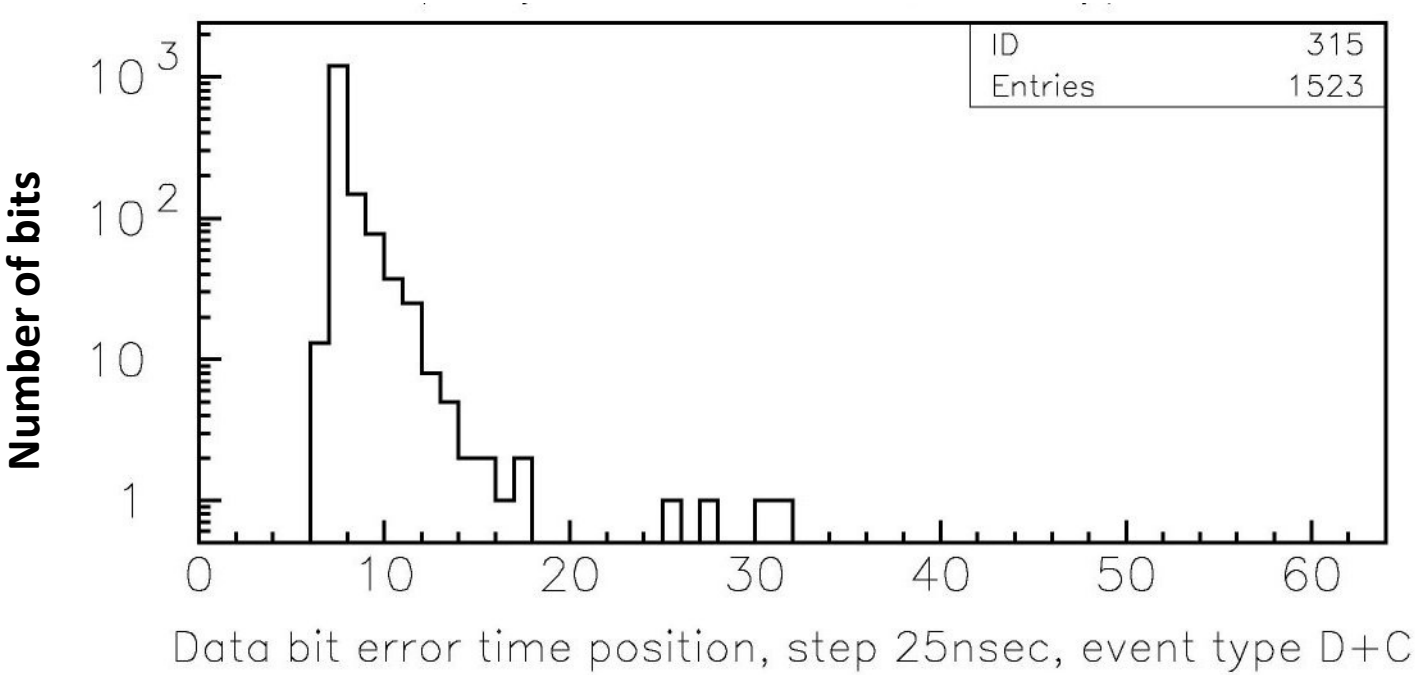
Event type D+C: data bit error multiplicity



In addition to data bit error, a disturbed clock was detected for each event.

A significant occurrence of events with two data bit errors, compared to type D.

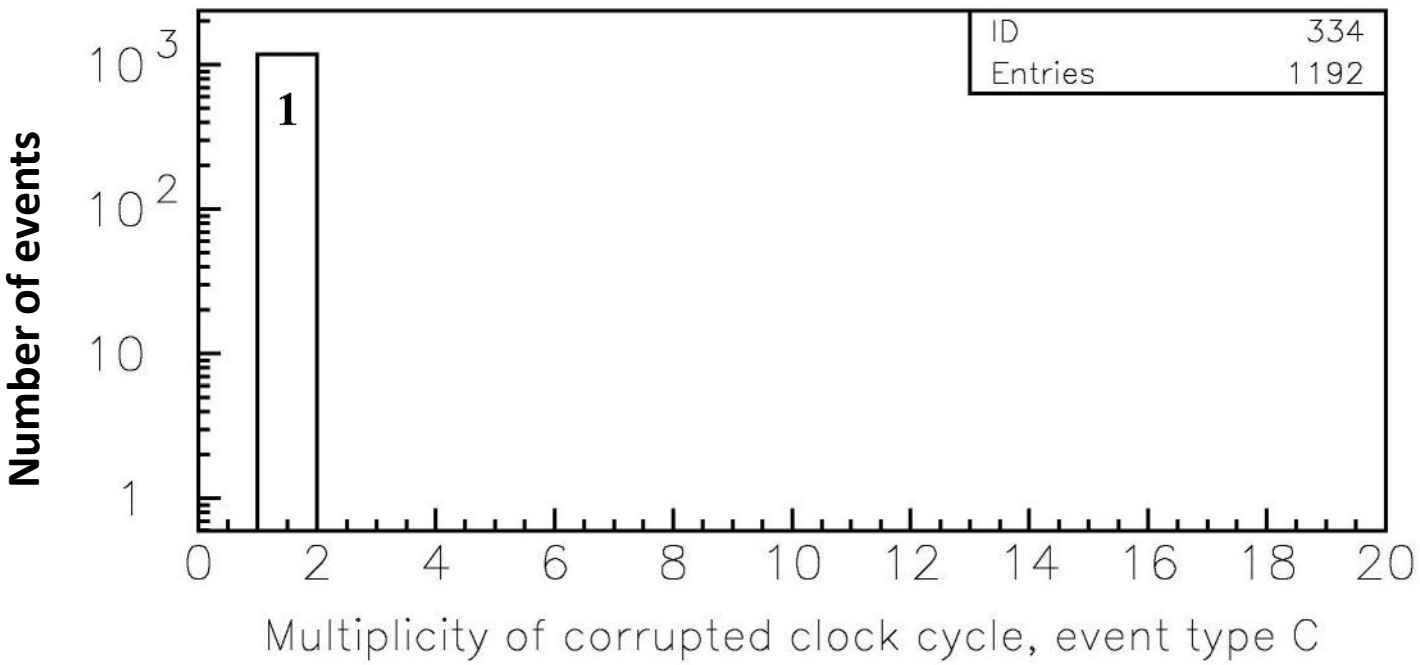
Event type D+C: data error bit time position



Most probable are events with data bit errors delayed by one clock cycle in respect to disturbed clock cycle (internal clock delay in Doric circuit) .

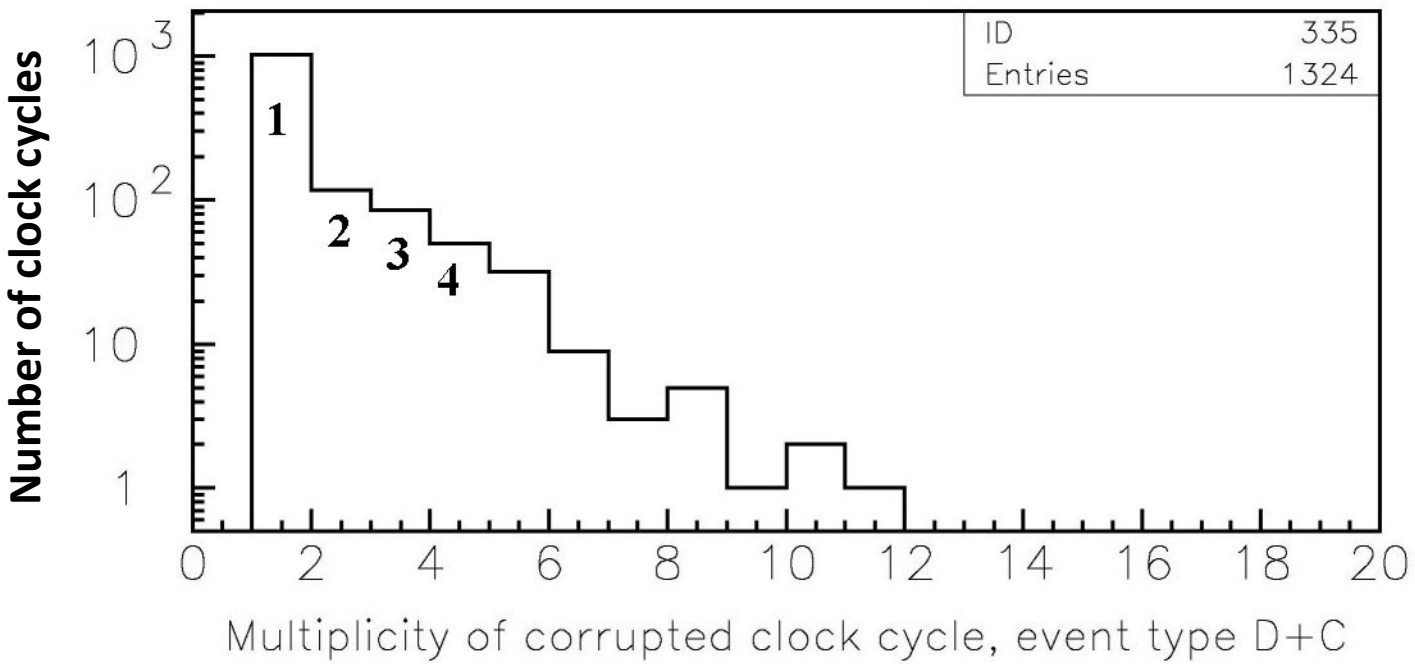
The second bit error is not always adjacent in time to the first one.

Event type C: multiplicity of disturbed clock cycle



Event type C: exclusively only one clock cycle is disturbed.

Event type D+C: multiplicity of disturbed clock cycle



Most likely only one clock cycle is disturbed for event type D+C .
For a significant number of events, the clock is disturbed longer than only one cycle. This may indicate a SEU induced disturbance of the Delay Locked Loop circuitry in the Doric chip. The clock duty cycle is then out of balance for some time, causing data bit errors during decoding.

Conclusions and outlook

- During August 2009 test run we have measured the following SEU occurrences:

77% cases with only one data bit-flip, among them
92% with 0 to 1 bit-flip transition and
8% with 1 to 0 bit-flip transition ,

11% cases with only one clock cycle disturbed and no data errors,

12% cases with both data errors and disturbed clock cycles,
with a duration of one and more clock cycles.

- Identified were SEU events with a likely impact on DLL decoding circuitry.
  The DLL circuit may take advantage of it and be improved accordingly in the future.

- More data evaluation and considerations are still in progress.

- In the future, we plan to update the test system with higher sampling rate for
  the returned clock, which will allow more accurate analyses of the recovered clock.