CHIR2 CMOS HW R&D

Sensor information and HW Development status

Stato CMOS – Rome, 07 September 2017

INFN Sezione di Roma & Sapienza

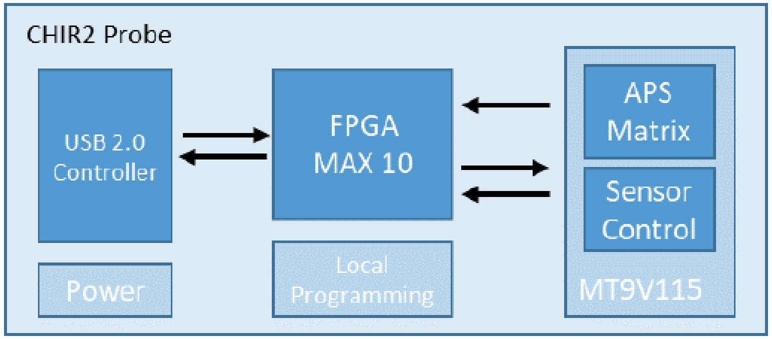


Fig. 1: CHIR2 Probe Read-out and Control System Overview

- The first system model had FPGA an on board (3x3/5x5mm package)
- The main motivation of this choice was the requirements of a ***limited number of cables*** (<u>NO I2C-Bus, single SERDES ch.</u>)
- Choosing the USB for data exchange requires either glue logic to interface with sensor or a DSP for payload reduction

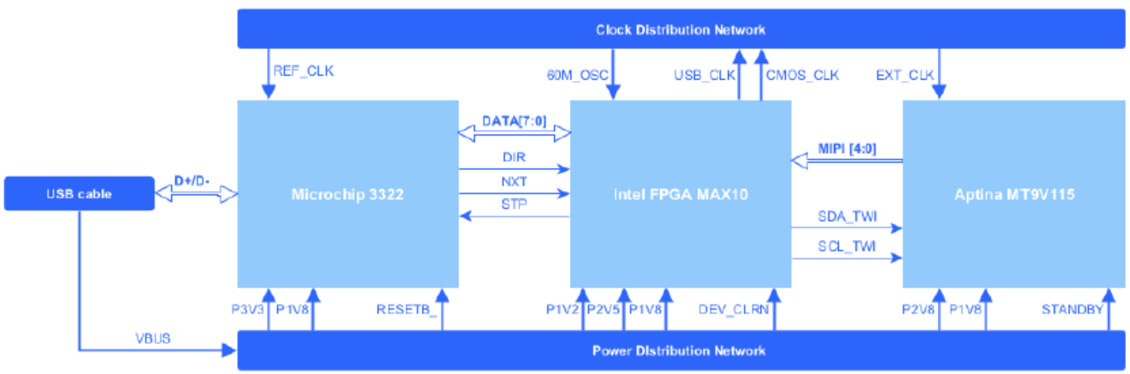


Fig. 2: CHIR2 Probe, Top-Level Architecture Block scheme

In order to reduce as much as possible the dimension we decided to use the small package (3x3mm, less fabric) and try to implement glue logic

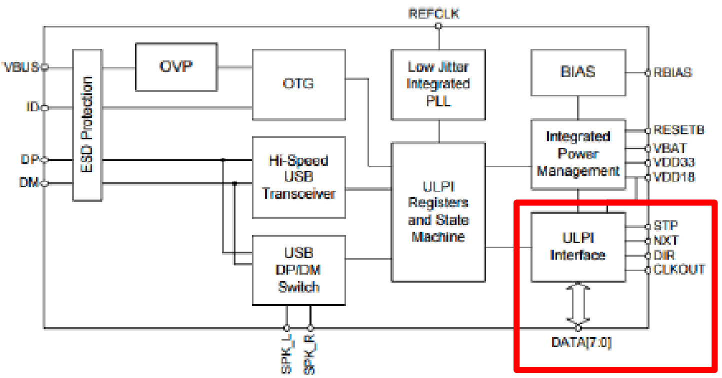


Fig. 3: Microchip USB 2.0 Transceiver 3322 Internal Architecture (Datasheet Rev 1.1 - 2012)

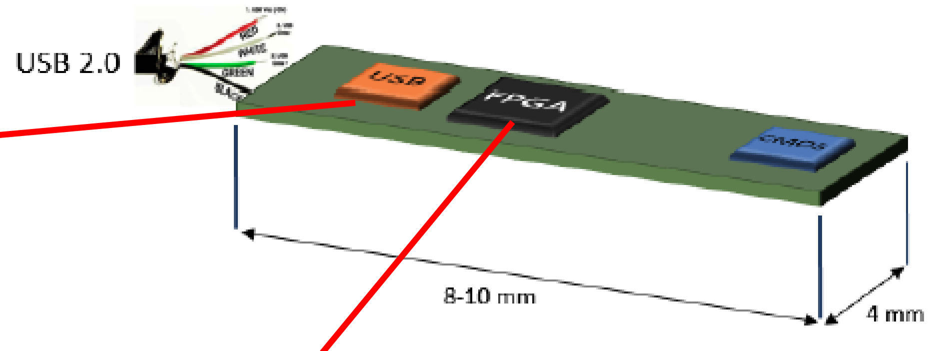


Fig. 13: CHIR2 Probe intended outline

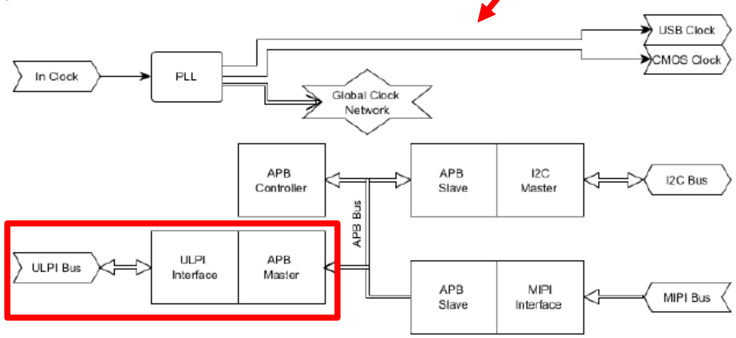


Fig. 4: FPGA MAX 10 Internal Architecture

- Main advantages of such implementation:

1. support up to 3 CMOS
2. small size

- Main disadvantages of such implementation:

1. **a lot of effort required** to adapt and test the ULPI interface (core from opencores.org)
2. **small form factor of the CMOS sensor,** small active area, slow response (NEW!!)

A greater sensor package relaxes the size requirements

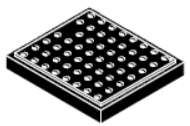
Relaxing as well the cable requirements (NO USB) make the development easier...

CMOS Sensor Candidates

We assume to use a sensor from ON Semiconductor (ex Aptina, ex Micron) probably from series MT9M/V_xyz in ODCSPxy package

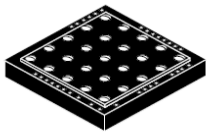
ON Semiconductor®

www.onsemi.com



ODCSP55 4.7x3.9
CASE 570BP

MT9M114



ODCSP−25
CASE 570BK

MT9V115

This package should have a small protective film (we talked with ON Semi. Italia application engineer) in fact both the -114 and the -115 have the same thickness :

Table 32. PACKAGE DIMENSIONS

Parameter	Symbol	Nominal	Min	Max	Nominal	Min	Max
		Millimeters			Inches		
Cavity height (Glass to Pixel Distance)	C4	0.041	0.037	0.045	0.002	0.001	0.002
Glass Thickness	C3	0.400	0.390	0.410	0.016	0.015	0.016

Table 1. KEY PERFORMANCE PARAMETERS

Parameter	Typical Value
Optical Format	1/6-inch
Active Pixels	1296 (H) × 976 (V) = 1.26 Mp
Pixel Size	1.9 μm × 1.9 μm
Color Filter Array	RGB Bayer
Shutter	Electronic Rolling Shutter (ERS)
Input Clock Range	6–54 MHz
Output MIPI Data Rate Maximum	768 Mb/s
Max. Frame Rate	30 fps Full Res 36.7 fps 720p 75 fps VGA 120 fps QVGA (Note 2)
Responsivity	2.24 V/Lux−sec (550 nm)
SNR_{MAX}	37 dB
Dynamic Range	70.8 dB
Supply Voltage Digital Analog I/O PLL PHY	 1.7−1.95 V 2.5−3.1 V 1.7−1.95 V or 2.5−3.1 V 2.5−3.1 V 1.7−1.95 V
Power Consumption	135 mW (Note 1)
Operating Temperature Range (Ambient) − T_A	–30°C to 70°C
Chief Ray Angle	27.7°
Active Imager Size	2.46 mm (H) × 1.85 mm (V), 3.08 mm Diagonal
Package Options	Bare Die, CSP

Table 1. KEY PARAMETERS

Parameter		Value
Optical Format		1/13-inch
Active Pixels		648 x 488 = 0.3 Mp (VGA)
Pixel Size		1.75 μm
Color Filter Array		RGB Bayer
Shutter Type		Electronic Rolling Shutter (ERS)
Input Clock Range		4–44 MHz
Output Clock Maximum	Parallel	22 MHz
	MIPI	176 Mbps
Output	Parallel	8 bit
	MIPI	8 bit, 10 bit
Frame Rate, Full Resolution		30 fps
Responsivity		1.88 V/lux*sec
SNR_{MAX} (Temporal)		34.1 dB
Dynamic Range		64 dB

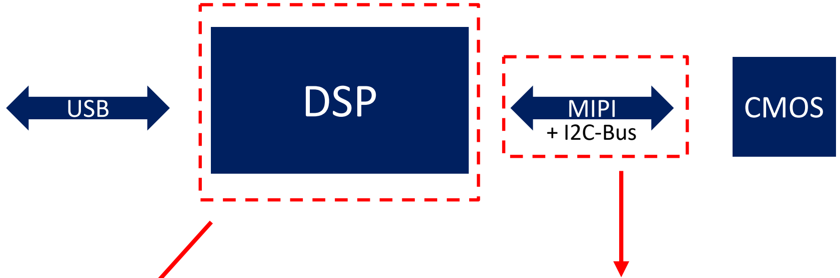
At the moment the candidate is the MT9M114 it has a greater optical format (1/6-inch) and the same pixel size of the -115 (same pix-to-pix cross talking expected)

It has 1.26Mp resolution (higher data bandwidth on MIPI)

ON Semi. app. ing. suggest to **migrate to a new series**, the AR0261 but we are stuck with NDA documents…

System Architecture Overview

Running back-end SW (and the GUI)



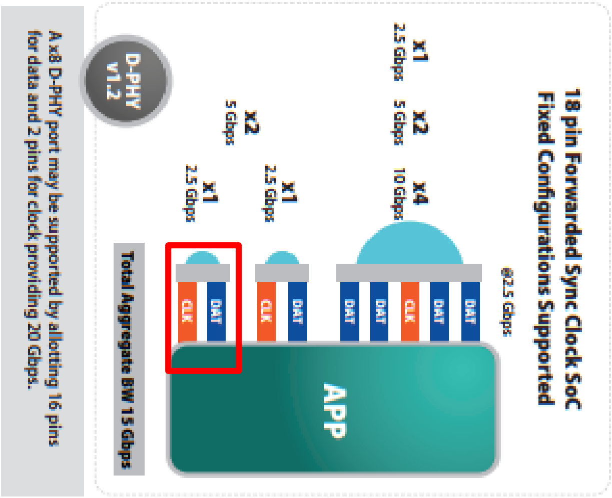
- It can be based either on uC or SoC (uC+FPGA)
- it is meant to execute the algorithm of "hit" detection as fast as possible
- **it must also interface the MIPI with USB**
- it must also configure the CMOS sensor via I2C-Bus

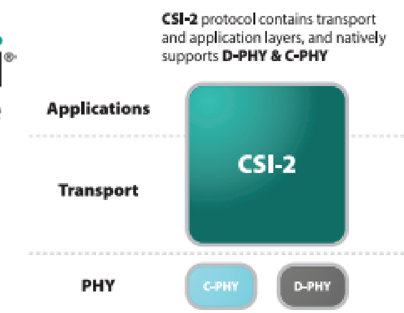
The MIPI of the MT9 is the CSI-2 version:

- **proprietary protocol**
- D-PHY based on Sub-LVDS

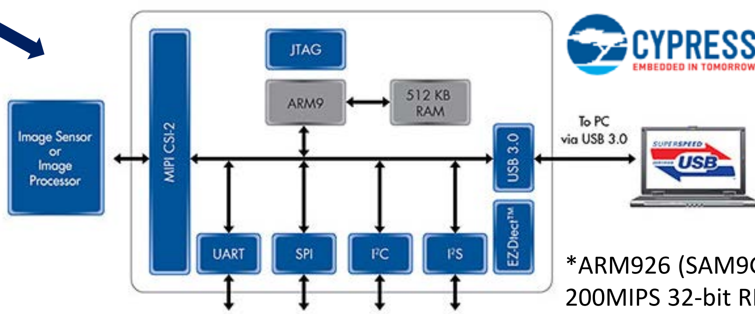
The CX3 has also the I2C-Bus to control the sensor.

WE NEED A MEDIA SUPPORT…





EZ-USB® CX3 Programmable MIPI CSI-2 to USB 3.0 Camera Controller

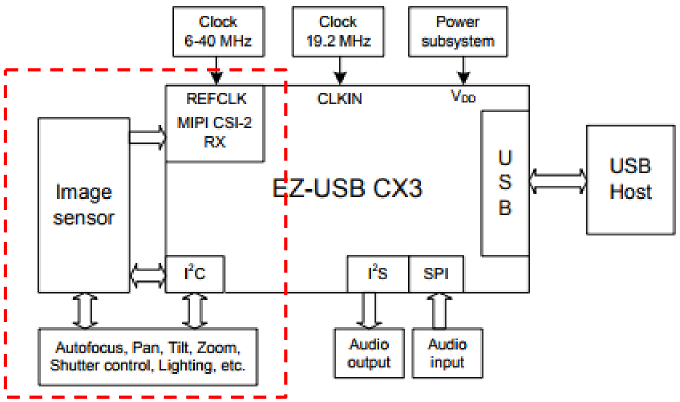


*ARM926 (SAM9G) inside
200MIPS 32-bit RISC

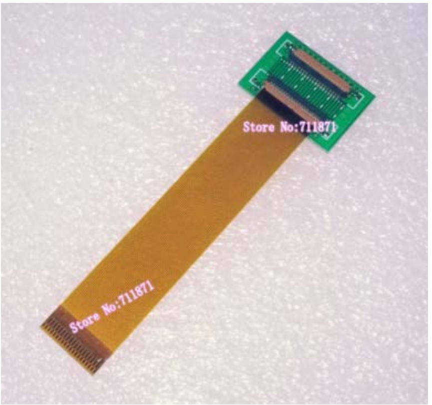
MIPI Media Support (HDMI fusion)

The MIPI interface is meant to be a means for controlling a sensor **placed on the same board** (the media is made of PCB traces and eventually connectors):

Figure 1. EZ-USB CX3 Example Application



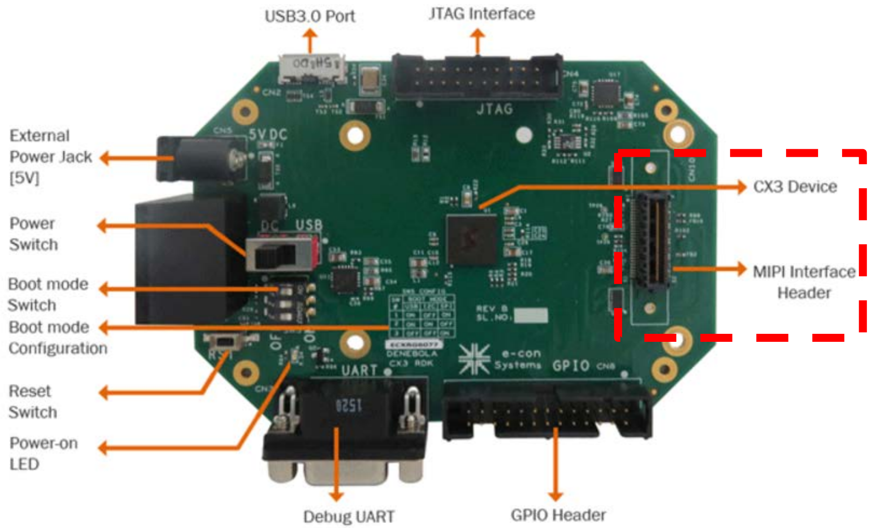
There are some specific flat cables used with MIPI channels, but **they do not fit our application** (they are meant to be used for test):



I did not find any better solution than adapting a commercial standard media support to our purpose:

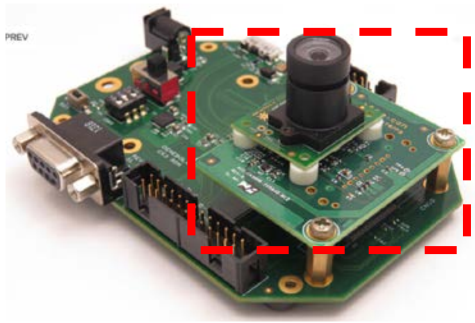
- dedicated I2C-Bus wires and control pin (3 + sens reset)
- up to 3 diff. data lanes and 1 diff. clock (> 1Gbps per ch.)
- dedicated power pin (+5V, max 50mA but carries more...)
- micro connector size (Type-D)

Cypress® offers an EVB designed by Denbola® which host the CX3:



Denebola - Cypress EZ-USB® CX3 Development Kit

But it is meant to be connected with a sensor board using a MIPI connector (not standard, it use a SAMTEC QFS) :



PRO:

- commercially available DSP (~250$)
- a lot of code examples
- ARM A9 fully available
- maybe it’s fast enough for our algorithm
- CX3 is in a 9x9mm package...

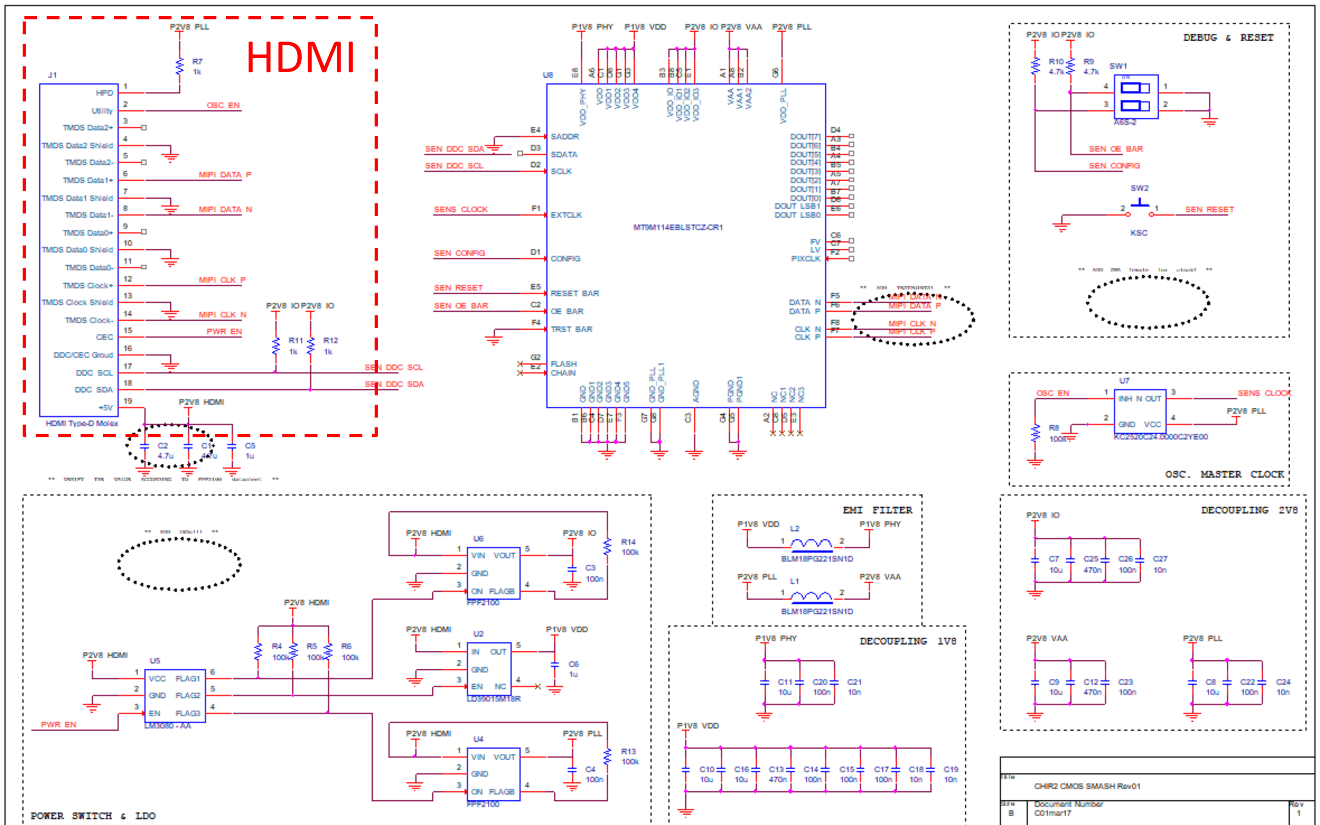
The idea is to develop:

1. a sensor holder and a small dummy adapter between HDMI and the SAMTEC QFS (**HW**)
2. the backend SW and the ARM A9 firmware (**SW**)

SMASH Rev01

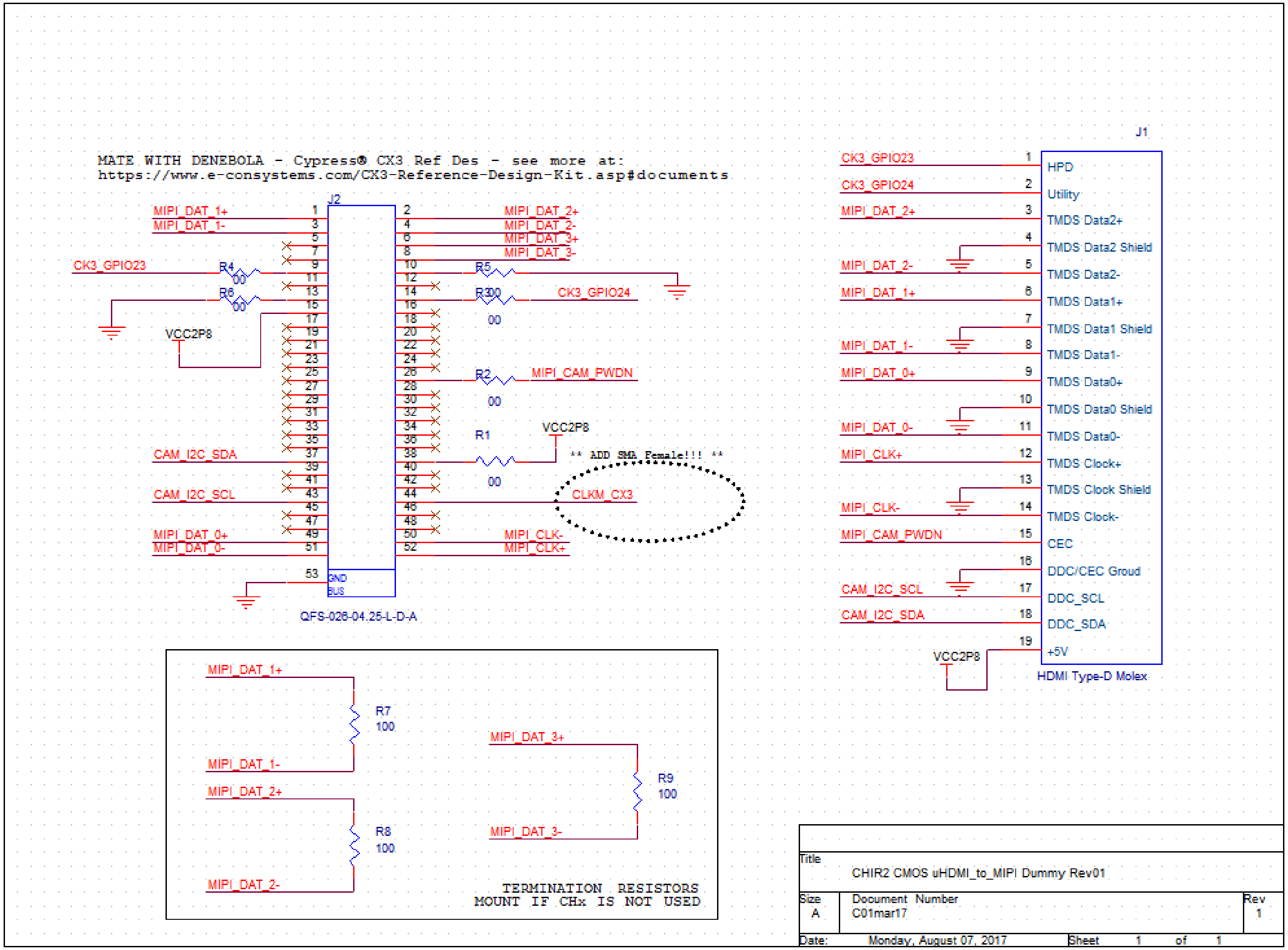
Small MT9- Adaptable Stand-alone Holder (SMASH):

- with small changes can host any of the MT9-Serie sensors (probably also the AR-Serie)
- provide power and clock to the sensor
- it has a HDMI Type-D connector (micro HDMI, removed in REV02)



- The schematics of REV01 are ready
- They provide also debug facilities (removed in REV02)
- We are waiting for the documentation from ON Semi. (NDA stuck) to complete the brd

uHDMI-to-MIPI REV01:



- just changing J2 you can use another DSP (*)
- The schematics of REV01 are ready
- We are waiting for the LabE (INFN) to develop the HDMI type-D lib

To be defined ASAP...

USB

DSP

MIPI
+ I2C-Bus

CMOS

SMASH
+ HDMI to MIPI

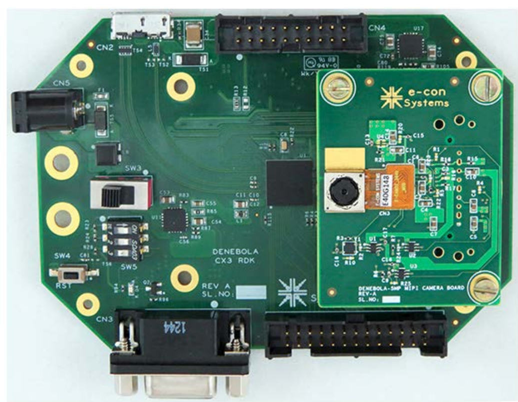
Running back-end SW
(and the GUI)

To be developed...

To be finalized ASAP by Roma1...

it might be good to start the RDA process
(purchase submission deadline 30 Sept.)

We also need to do test on the custom hw when delivered (< Dec 2017)



(*) Another solution might uses the ON Semi. Demo 3X board...

To be purchased ASAP...

<u>it requires fw (Perugia?)</u>