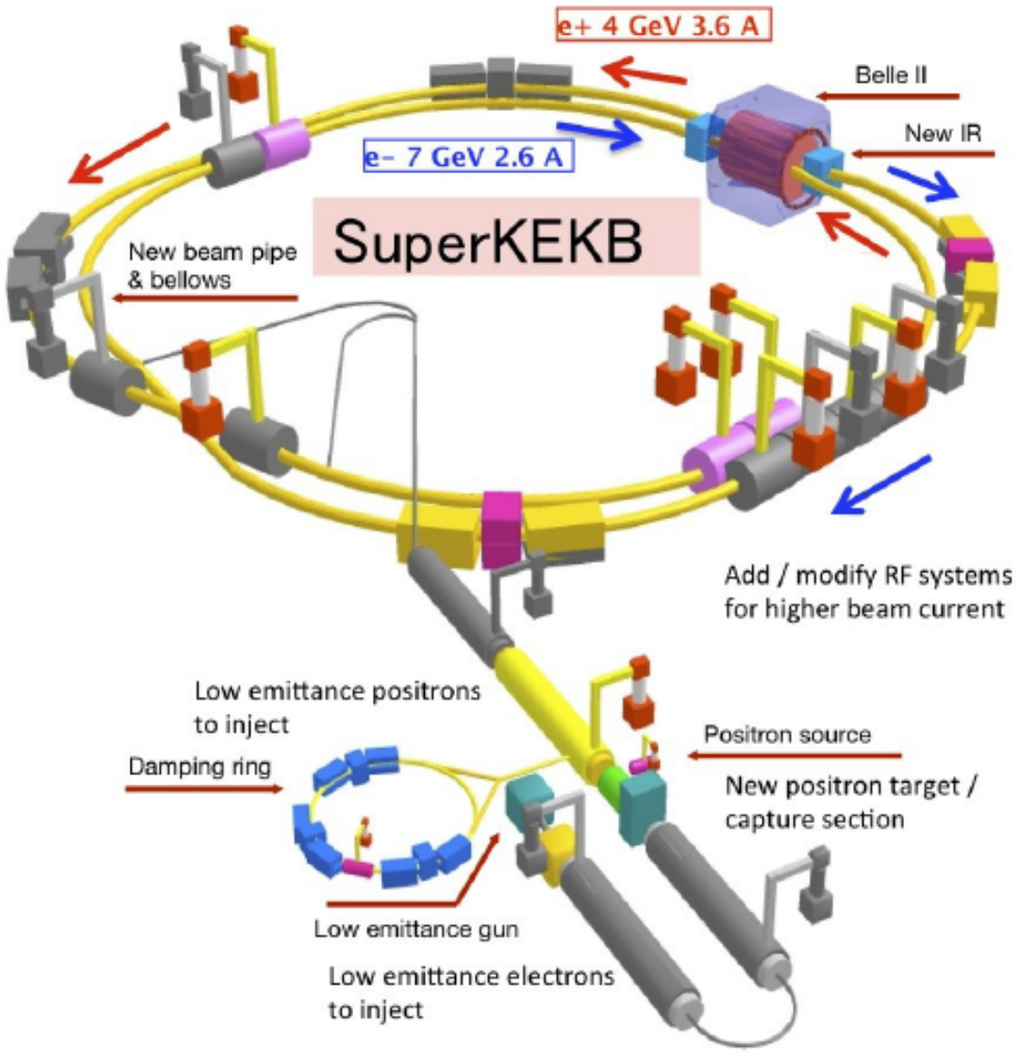
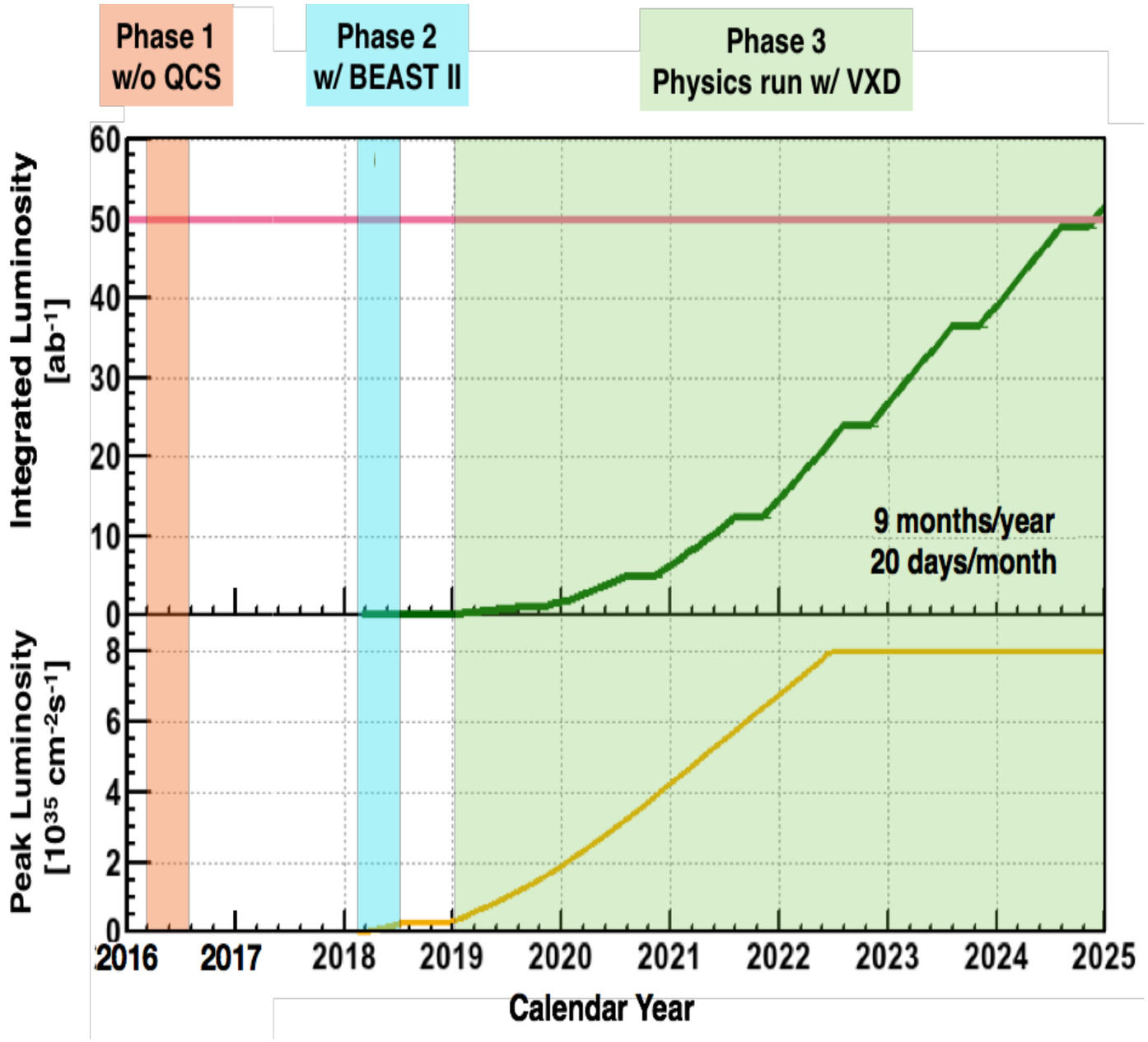
Status of PXD and SVD

C. Schwanda / C.Niebuhr
on behalf of the VXD Groups

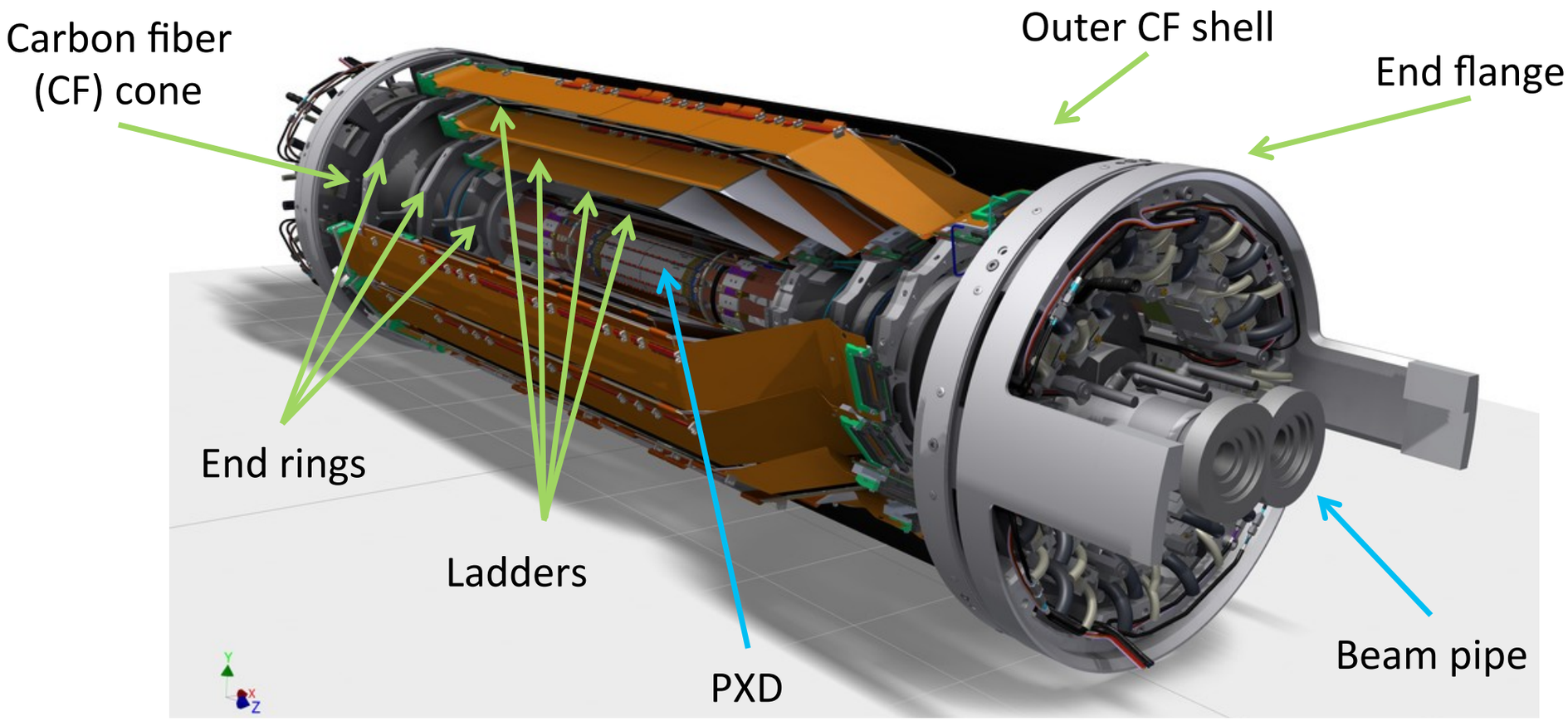
SuperKEKB



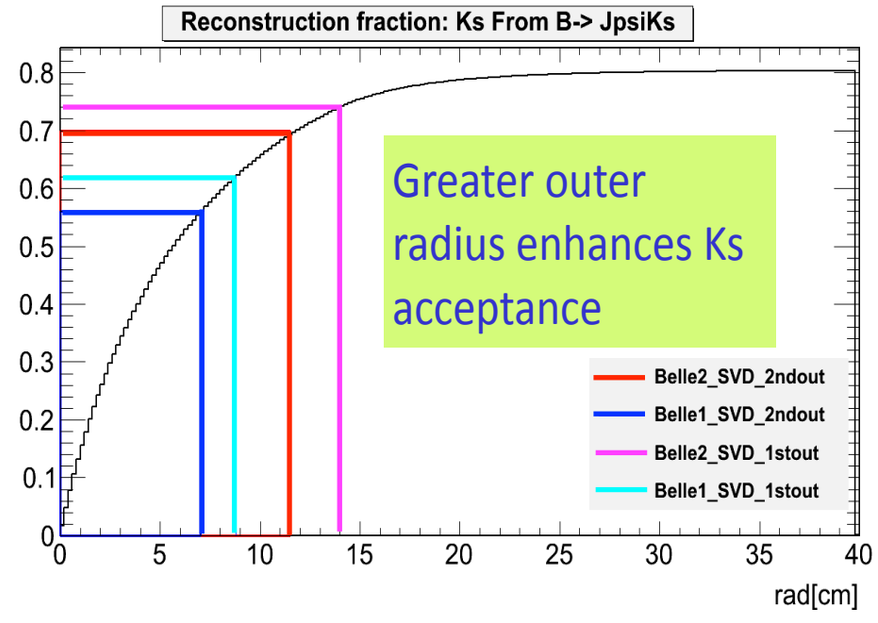


- SuperKEKB: Asymmetric e^+e^- collider @ E_{CM} = 10.58 GeV = m(Υ(4S))
- Peak luminosity L = 8×10^{35} $cm^{-2}s^{-1}$, i.e. 40 times higher than KEKB machine
- Nano beam scheme: reduce beam size (x1/20) and increase currents (x2)

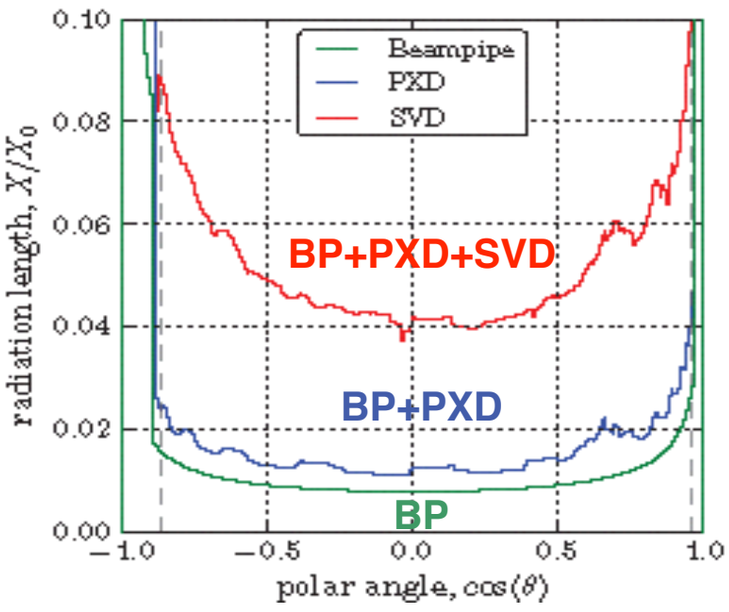
Belle II Vertex Detector VXD



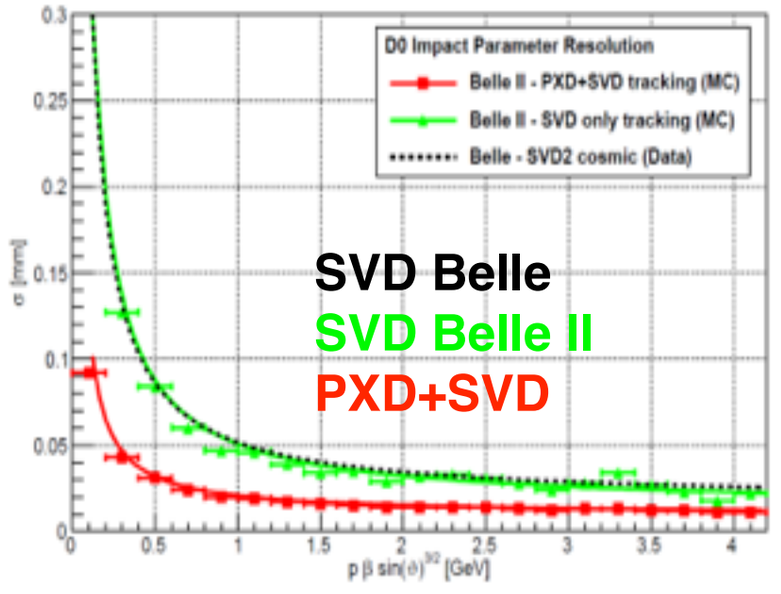
Acceptance



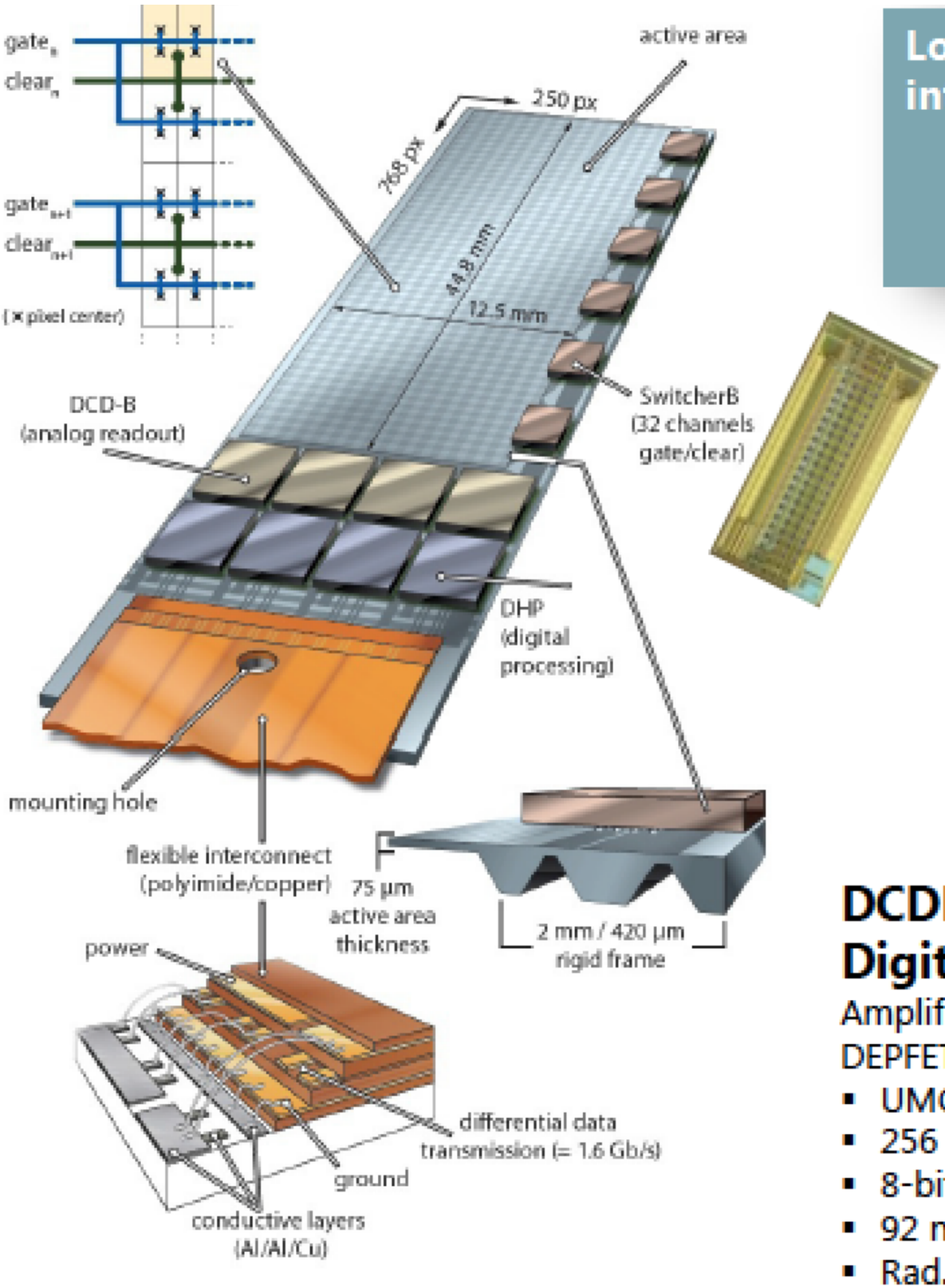
Material budget



Resolution



PXD Components

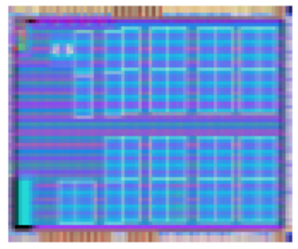


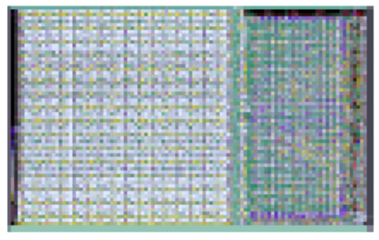
Low mass vertex detectors with highest possible integration!

- Thin sensor area **75µm**
- EOS for r/o ASICs
- Thin (perforated) frame with steering ASICS

SwitcherB - Row Control

- AMS/IBM HVCMOS 180 nm
- Size 3.6 x 1.5 mm^2
- Gate and Clear signal
- Fast HV ramp for Clear
- Rad. hard proved (36 Mrad)





DCDB - Drain Current Digitizer

Amplification and digitization of DEPFET signals.

- UMC 180 nm
- 256 input channels
- 8-bit ADC per channel
- 92 ns sampling time
- Rad. hard proved (10 Mrad)

DHP - Data Handling Processor

- TSMC 65 nm
- Size 4.0 x 3.2 mm^2
- Stores raw data and pedestals
- Common mode and pedestal correction
- Data reduction (zero suppression)
- Timing and trigger control
- Rad. Hard proved (100 Mrad)

PXD System with Off-Module Data Flow

Total of 0.2% of X_0

2 layers: @1.4(2.2) cm

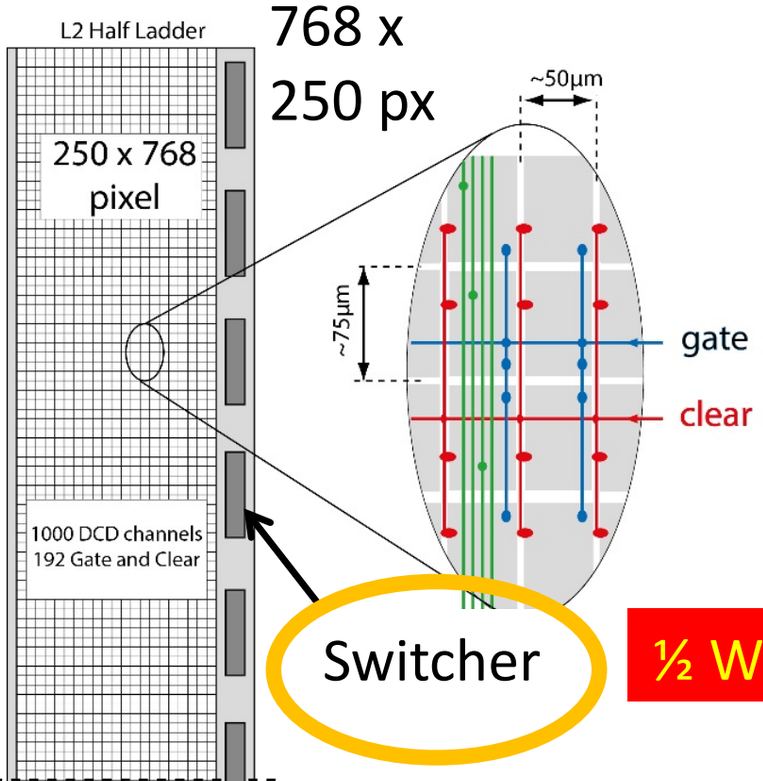
Pixels: 50 x 60(75) µm

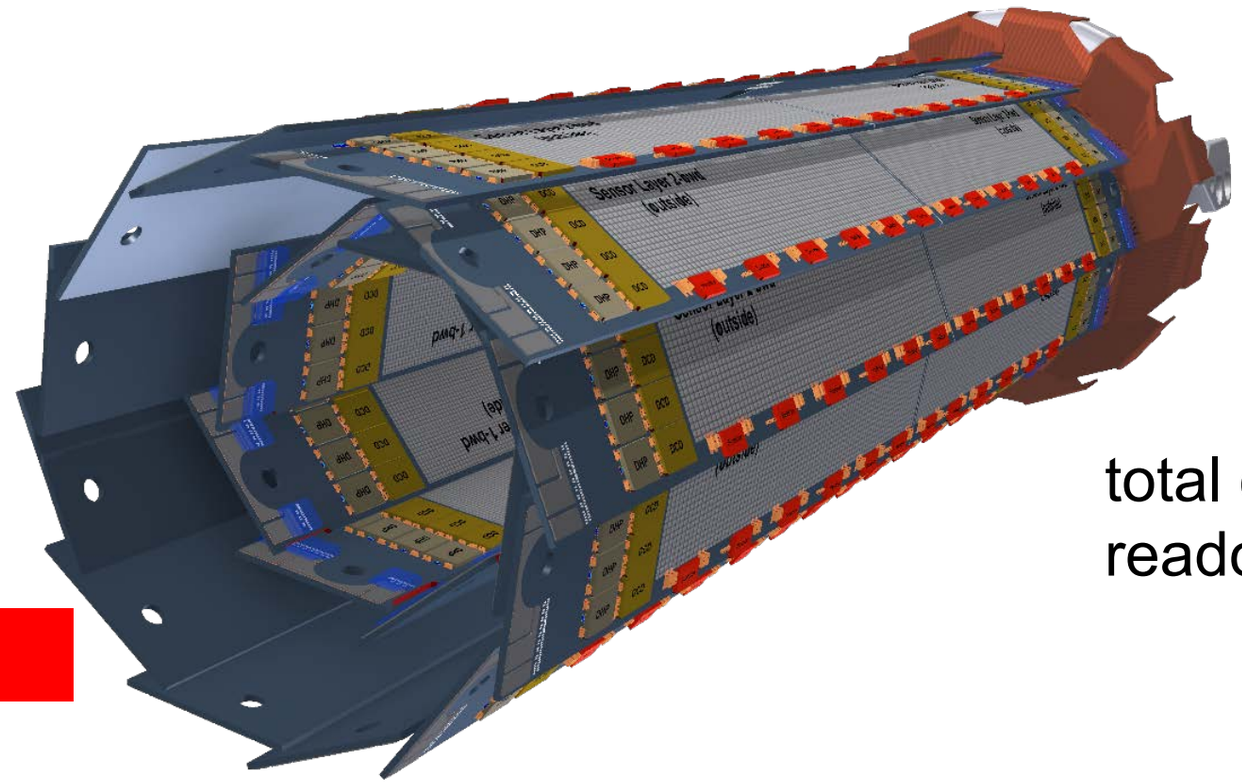
Thickness: 75 µm

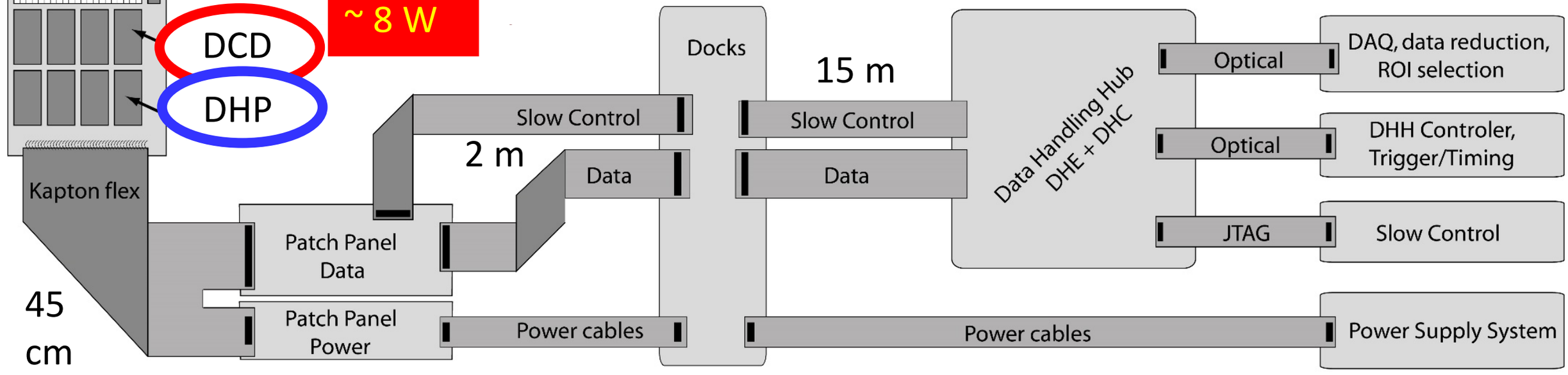
total of 8 Mpx
readout: 20 µs

Half ladder

768 x
250 px







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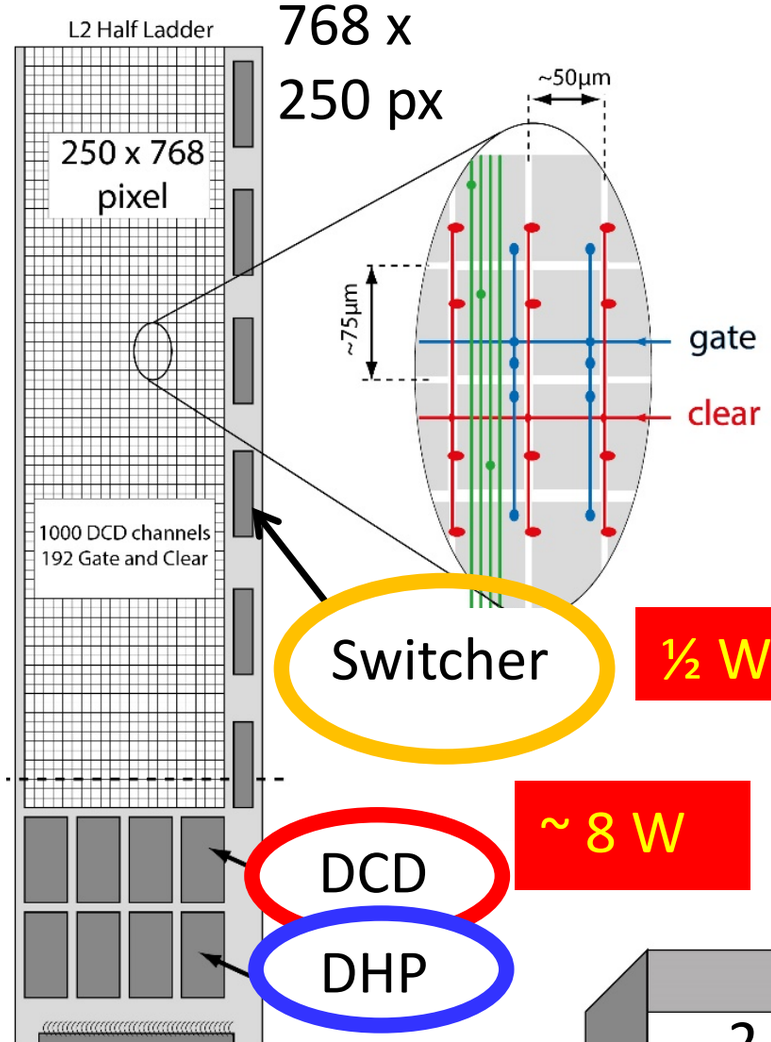
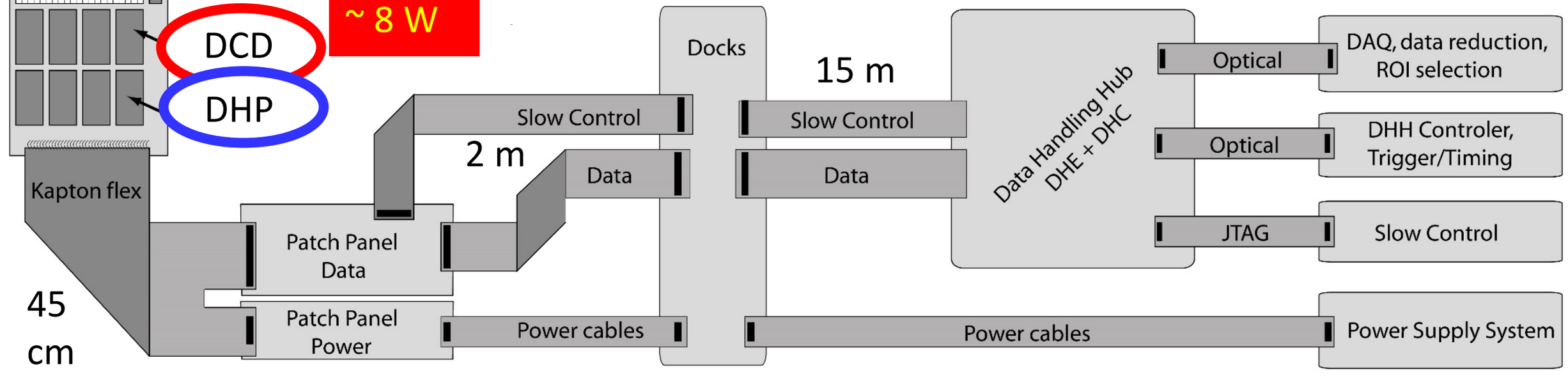


DHH: Data Handling Hybrid

- Slow control master
- Clustering

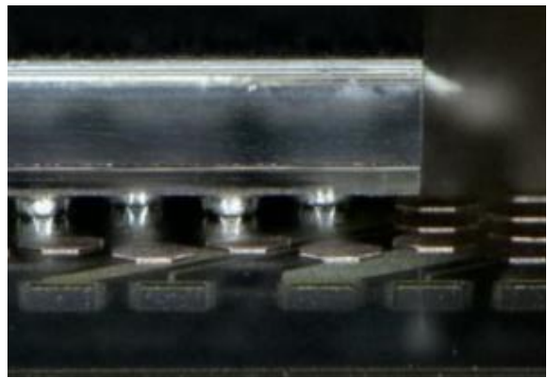
ONSEN: Online Selector Node

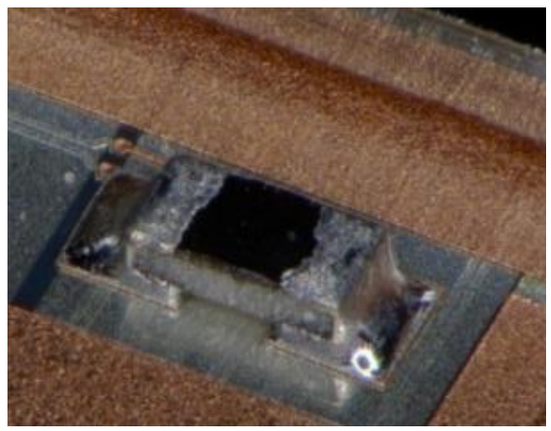
- Data Buffer
- Online data reduction via ROI selection

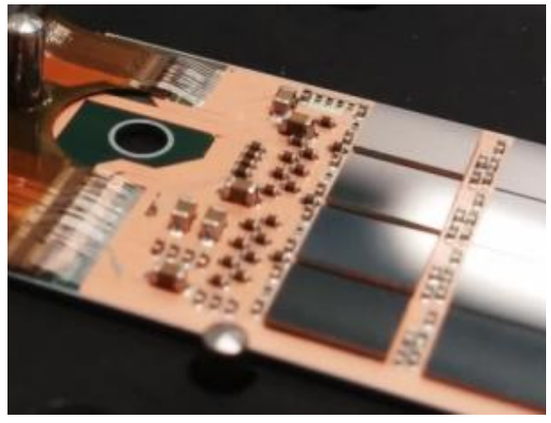


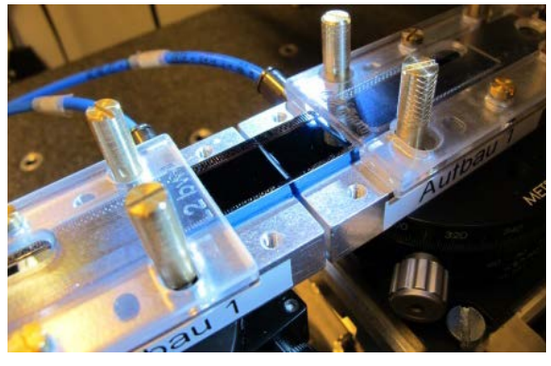
Module and Ladder Assembly

1. Flip Chip of ASICs (~240°C): √
   - Bumped ASICs have the solder balls (SAC305 and AgSn)
2. SMD placement (~200°C): √
   - Passive components (termination resistors, decoupling caps)
   - Dispense solder paste/jetting of solder balls
   - First module tests on probe station possible at this stage
3. Kapton attachment (~170°C), wire bonding and ladder gluing (room temperature):
   - Solder paste printing on kapton, soldering √
   - Wire-bond 32 µm Al bond wires √
     - Test modules √
   - Dispense adhesive, align two modules, join two modules to ladder
     - Ladder tests (presently in qualification stage)
     - Delay to be absorbed by re-arrangement of assembly procedure (kapton and ladder gluing) and acceleration of testing procedure

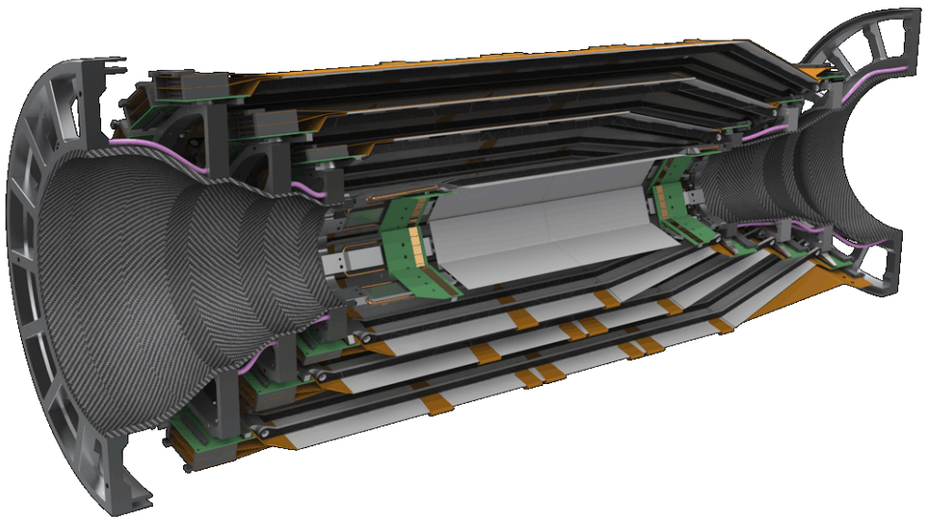








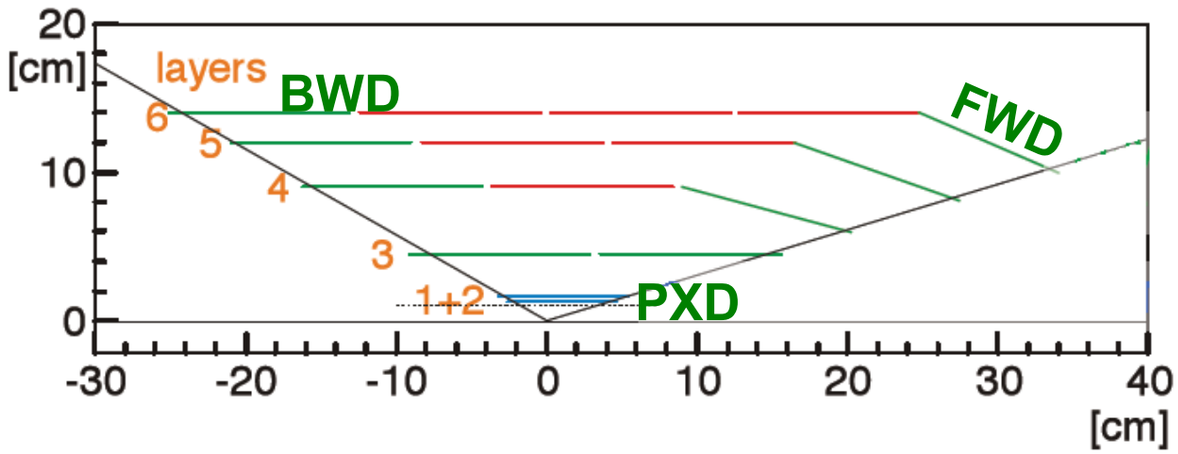
SVD Overview



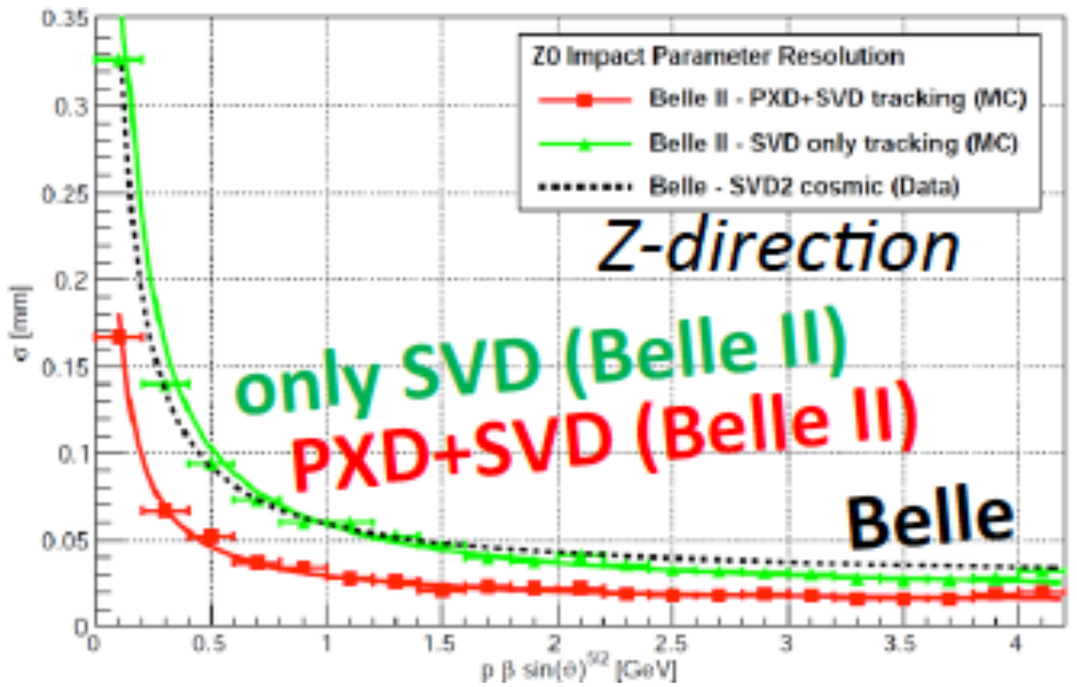
☞ Global enterprise involving groups from Australia, Asia and Europe

Layer	Ladder	Institute
3	7(+1)	Melbourne
4	10(+2)	TIFR Mumbai
5	12(+3)	HEPHY Vienna
6	16(+4)	Kavli IPMU

INFN Pisa: Layer 4-6 forward (FWD) and backward (BWD) modules



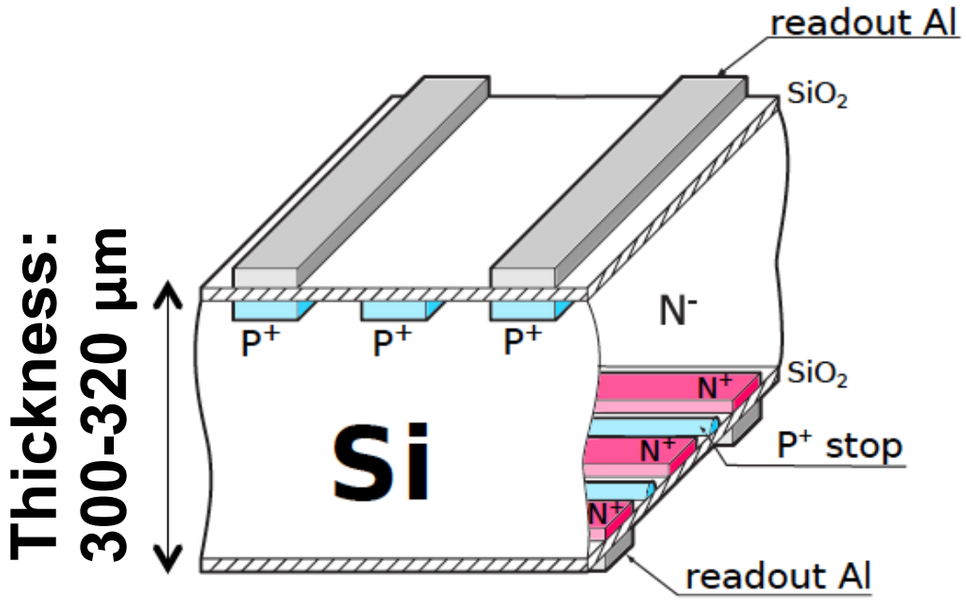
Layer	Sensor/ ladder	Origami	Length	Radius	Slant angle
3	2	0	262 mm	39 mm	0°
4	3	1	390 mm	80 mm	11.9°
5	4	2	515 mm	104 mm	17.2°
6	5	3	645 mm	135 mm	21.1°



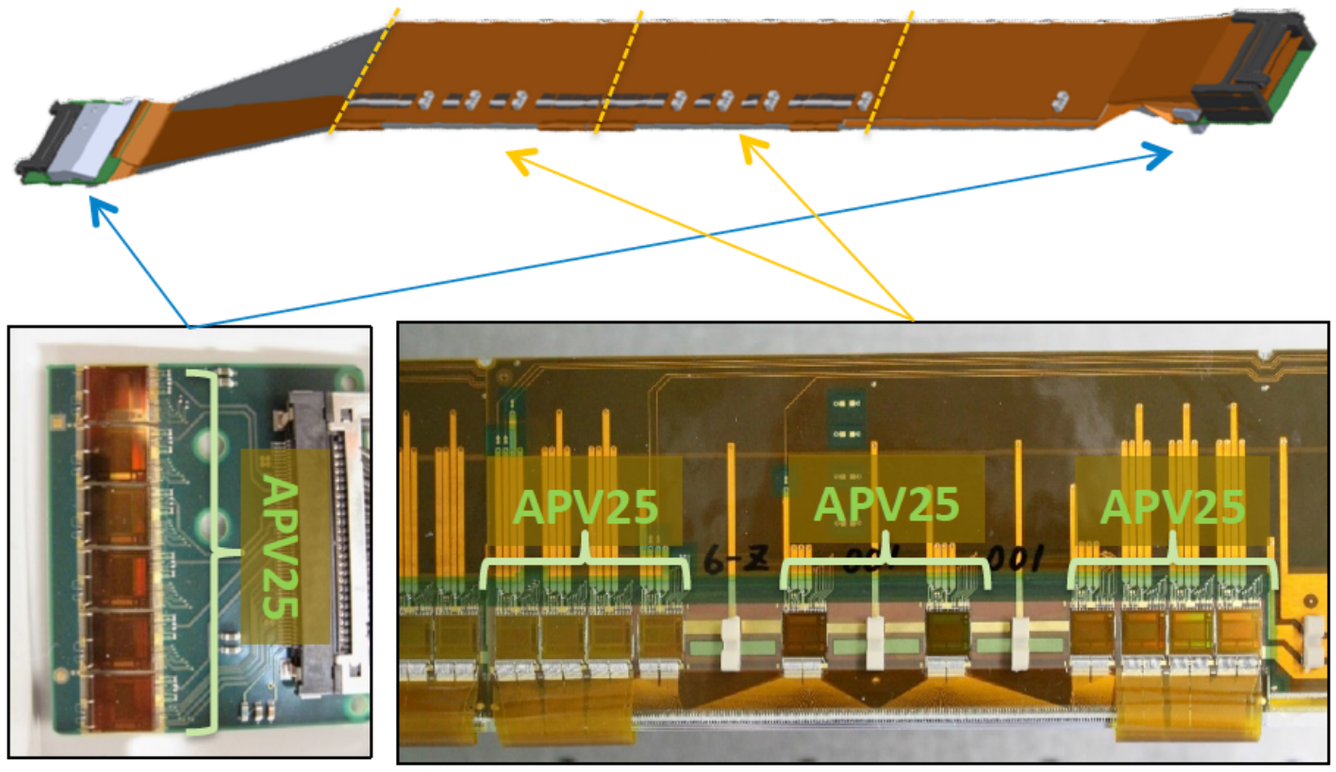
- Significantly improved resolution compared to Belle (20μm at 2 GeV)

Sensors and ASICs

➡ Double-sided silicon micro-strip detector (DSSD): p-in-n 6′ wafer



➡ APV25 chip: originally developed for CMS

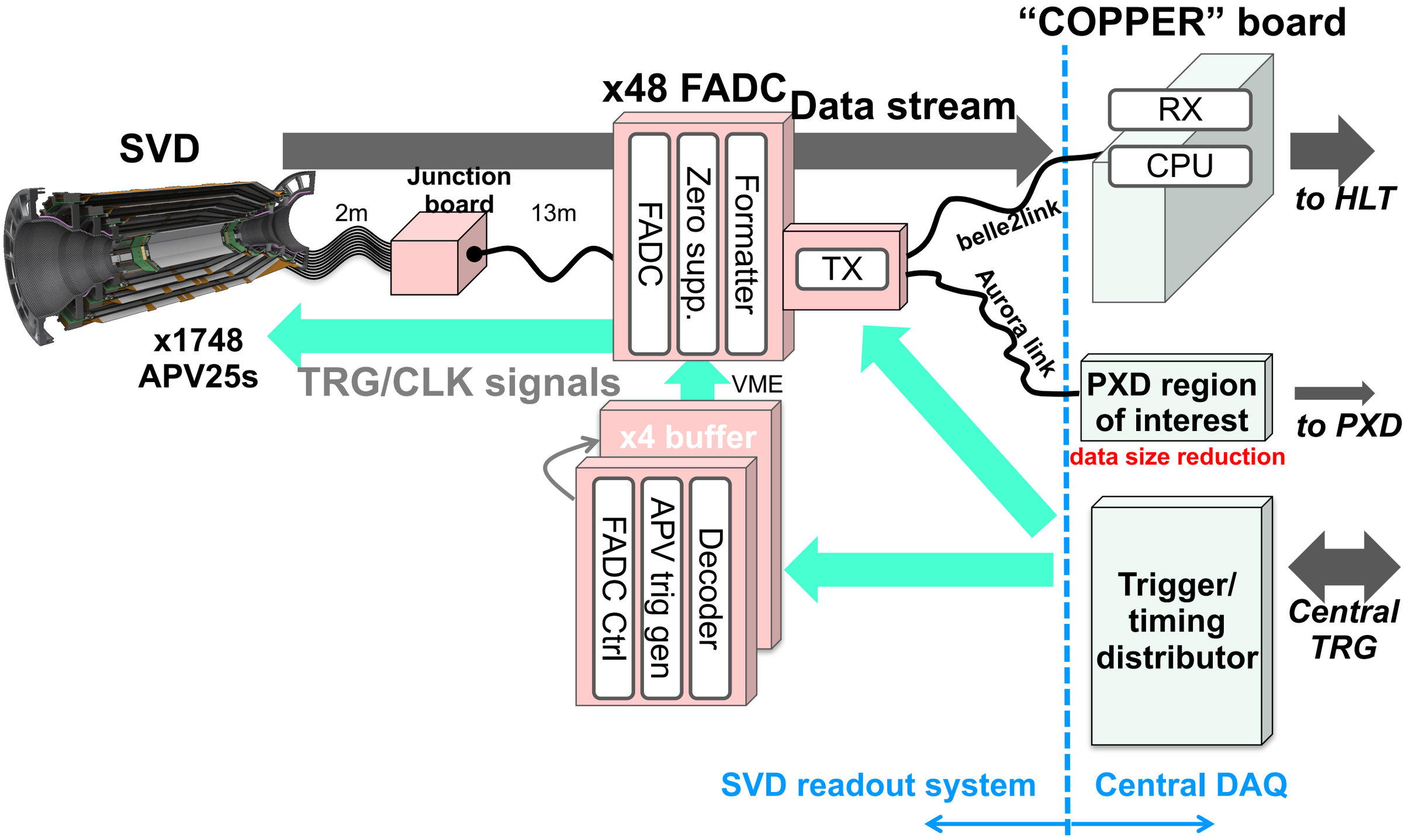


Sensors	Rectangular (Large)	Rectangular (Small)	Trapezoidal
# of *p*-strips	768	768	768
p-strip pitch	75µm	50µm	50...75µm
# of *n*-strips	512	768	512
n-strip pitch	240µm	160µm	240µm
		HPK	Micron

Requirement: short shaping time to cope with Belle-II high rate as well as high S/N

- Shaping time: 50 ns
- Radiation hardness: > 1 MGy
- # input channels: 128 per chip
- 192 cells deep-analog pipeline for dead-time reduction
- Thinned down to 100µm to reduce material budget

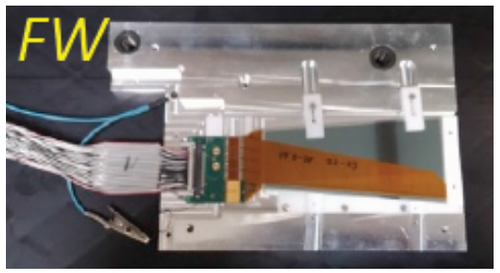
SVD Backend Electronics



☞ Prototypes of all components are developed and tested

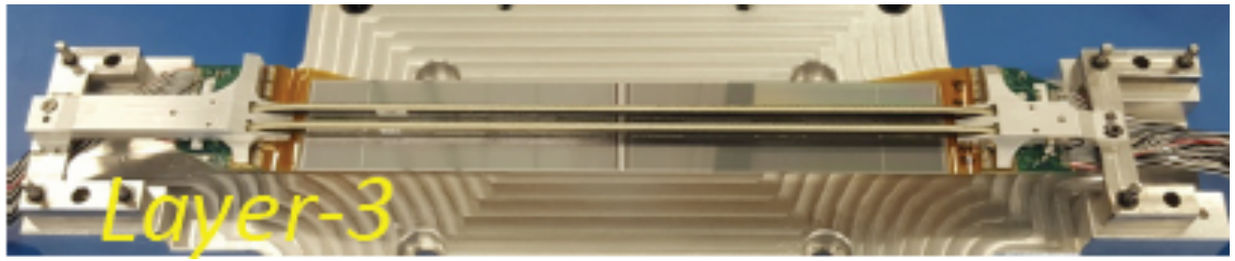
Status of SVD Assembly

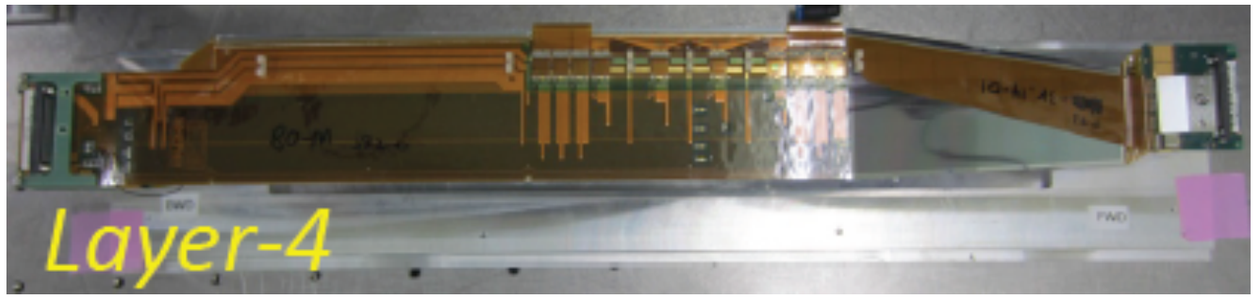
All sites into mass production for a while

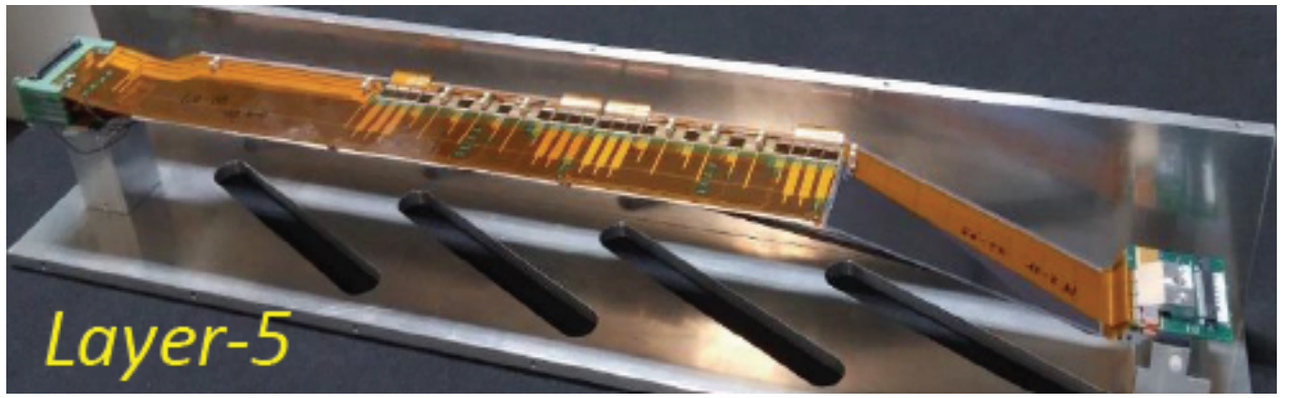


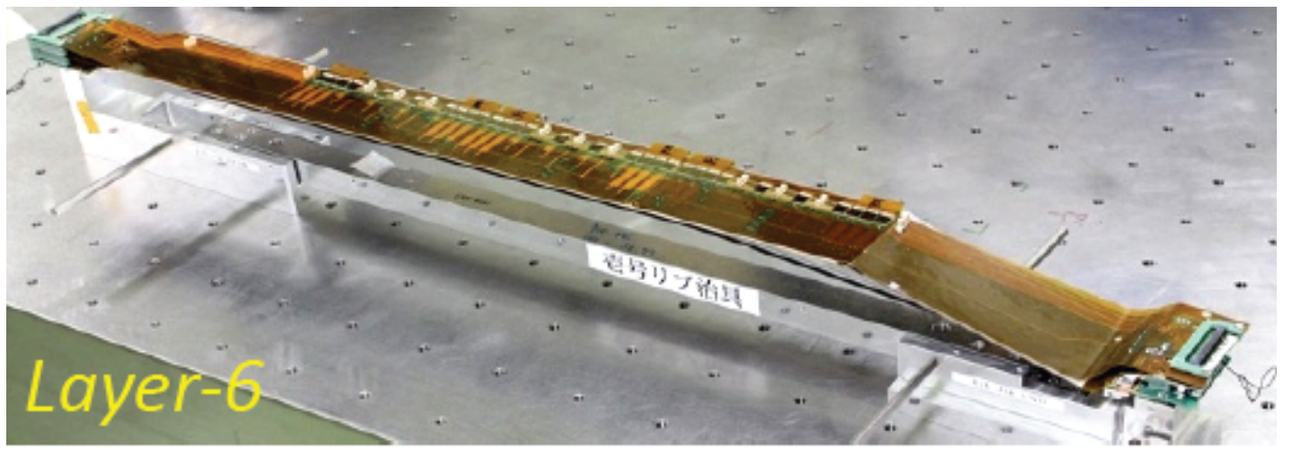
Pisa (FW/BW) **Production completed** – in total 60 class A FW and 55 BW subassemblies were built
Melbourne (L3) **Production completed** – 11 good ladders available out of 7+2 ladders needed
TIFR (L4) 8 good ladders in hand, 4 more to build (expect to finish in Jan 2018)
HEPHY (L5) **Production completed** – 15 good ladders in hand
Kavli IPMU (L6) 13 good ladders available, 7 more to go, precisely on June 2017 B2GM schedule (end of production: second half of Feb 2018)

All expected to finish by March 2018



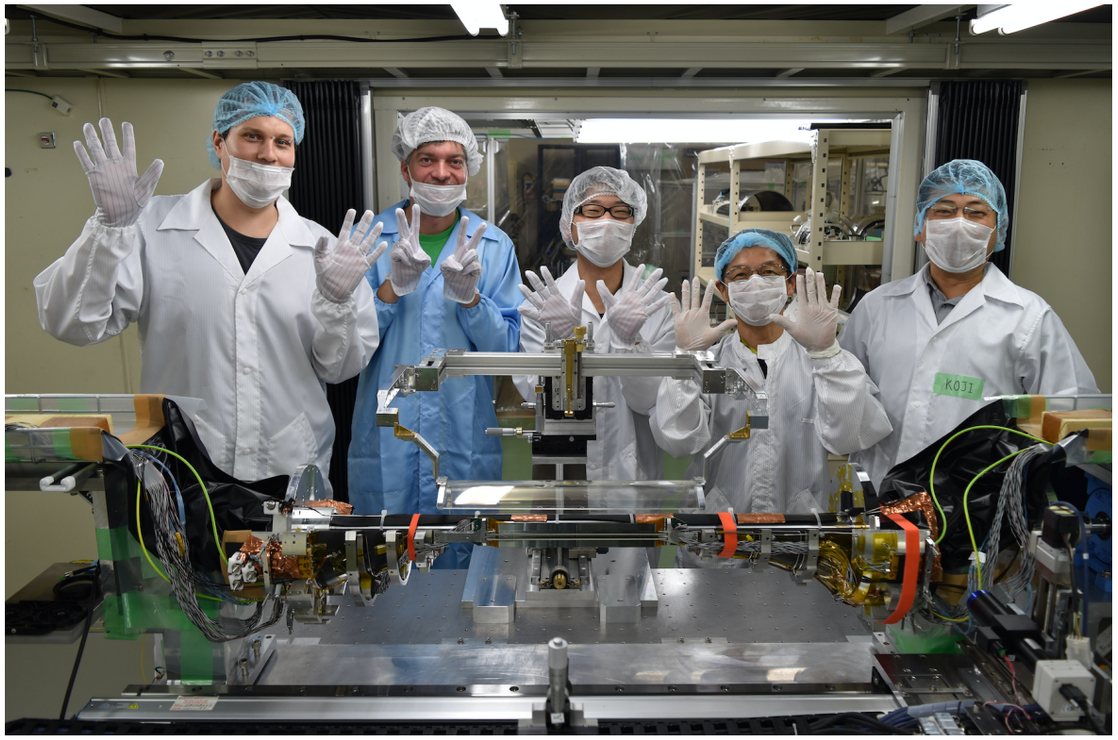






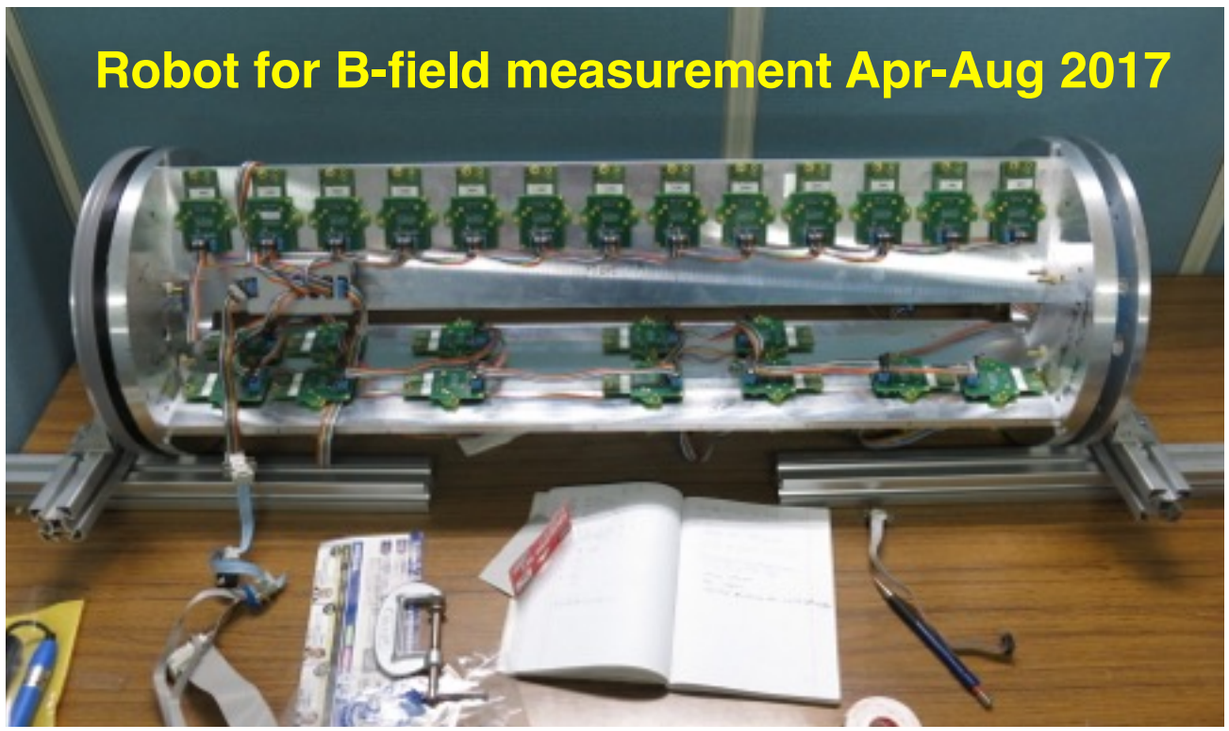
SVD Ladder Mount Schedule

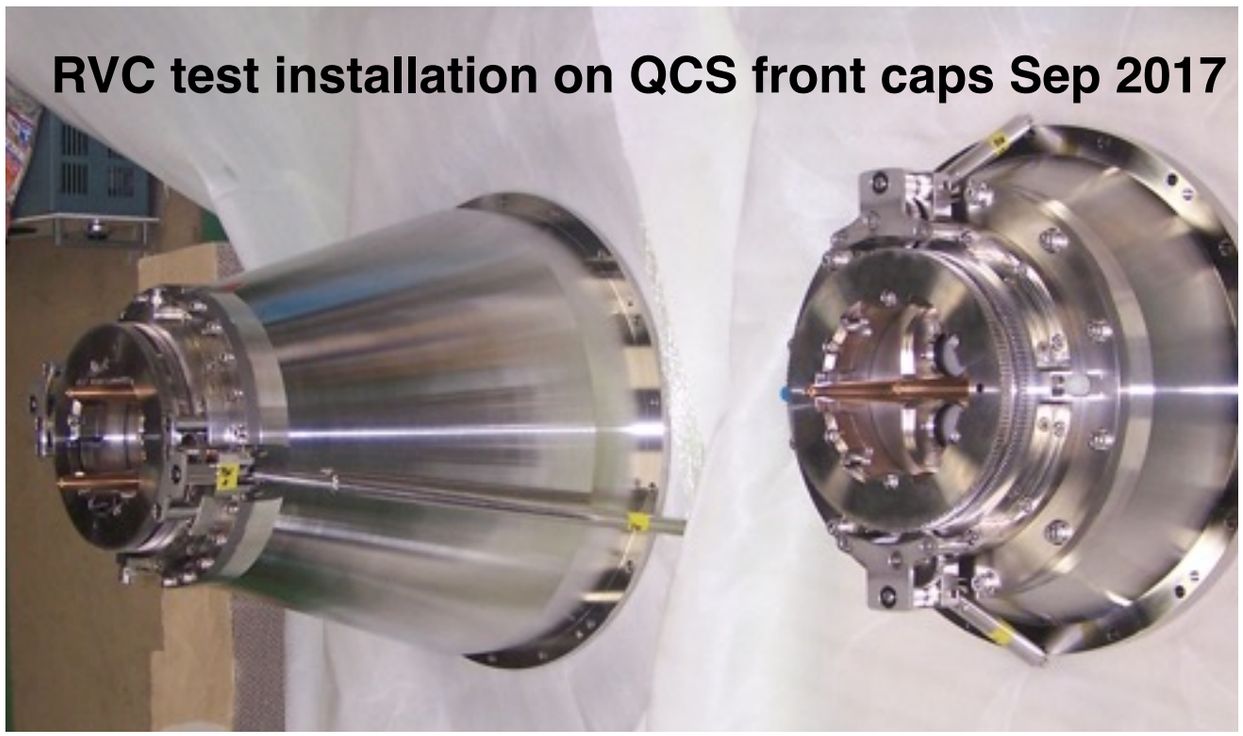
Happy LM team with the first mounted ladder



Item	Date	
Ladder mount 1st half shell start	Sep 7, 2017	√
L3 mount complete	Sep 19, 2017	√
L4 mount complete	Oct 18, 2017	
L5 mount complete	Nov 9, 2017	
L6 mount complete	Dec 6, 2017	
Completion 1st half shell (including pick up)	Dec 8, 2017	
Ladder mount 2nd half shell start	Dec 21, 2017	
Completion 2nd half shell (including pick up)	Apr 2, 2018	

Common VXD Infrastructure Activities





Phase 2 Vertex Detector: BEAST II Experiment

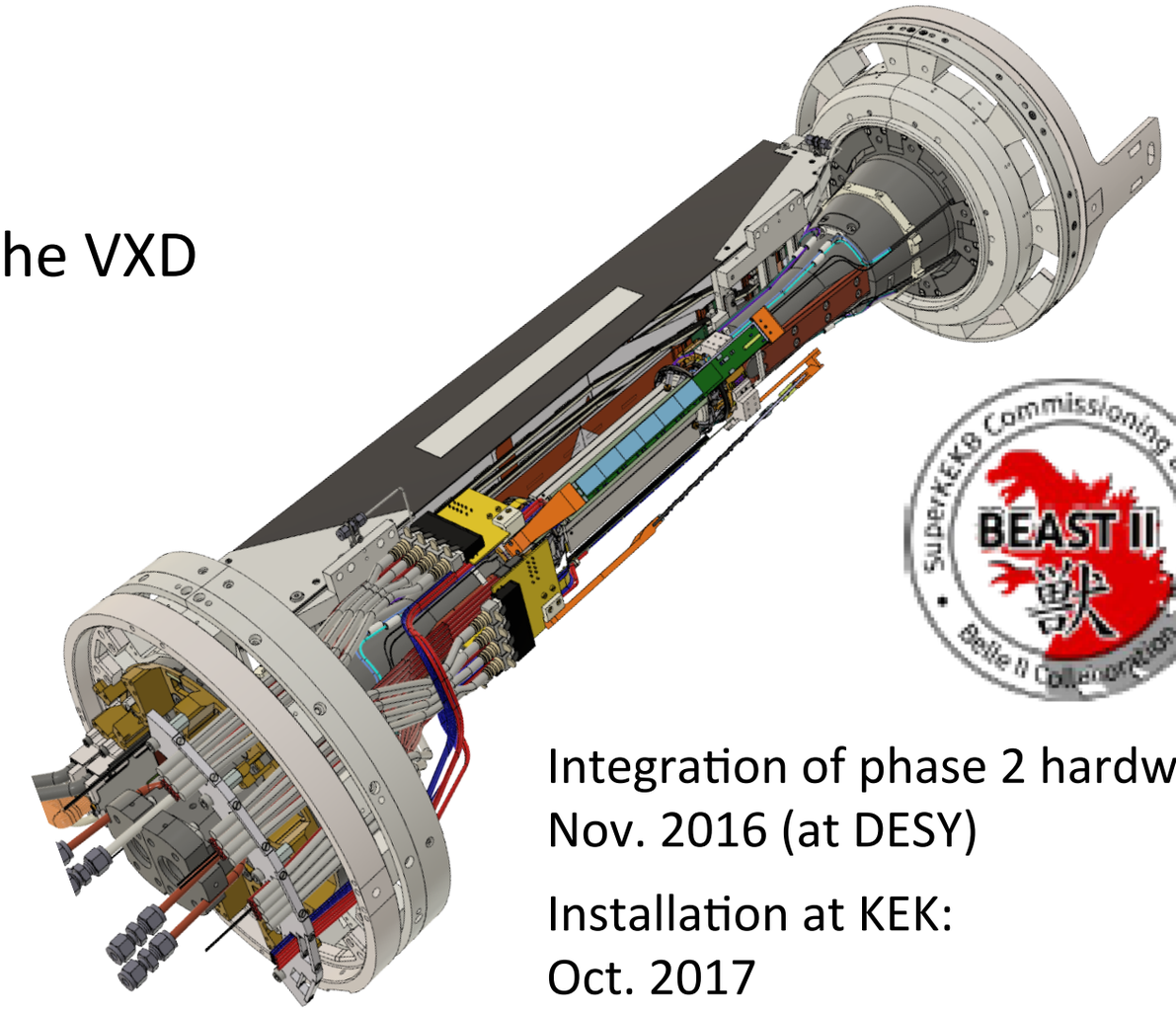
Motivation:

- Machine commissioning
- Radiation safe environment for the VXD

BEAST II detector:

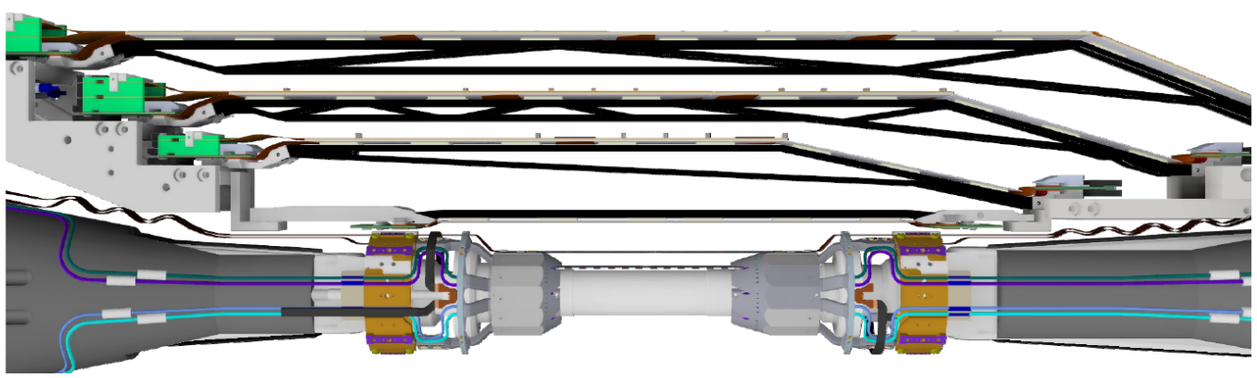
- 2 ladders PXD
- 4 ladders SVD
- Dedicated radiation monitors:
  FANGS, CLAWS, PLUME,
  radiochromic foils

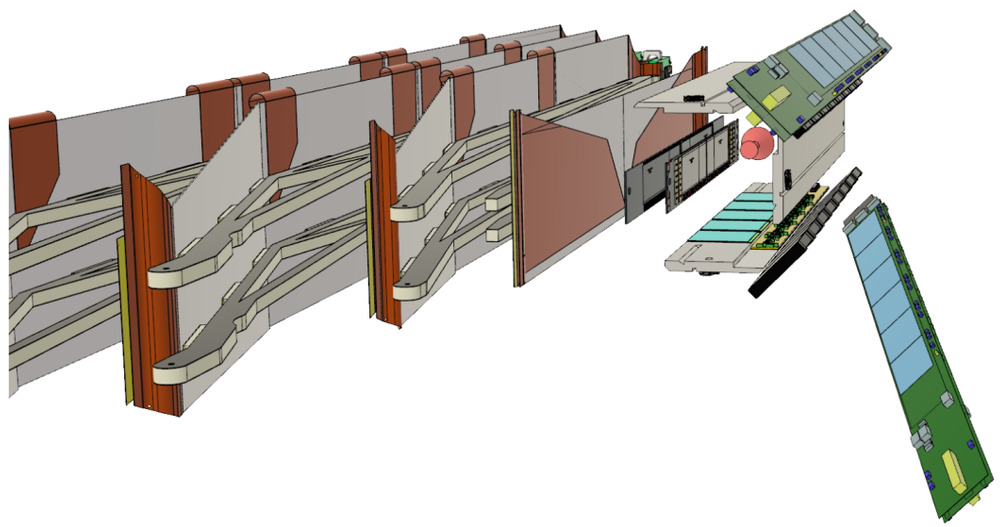
VXD sensors in +x direction
⇒ highest synchrotron radiation



Integration of phase 2 hardware:
Nov. 2016 (at DESY)

Installation at KEK:
Oct. 2017





Preparations for Phase 2

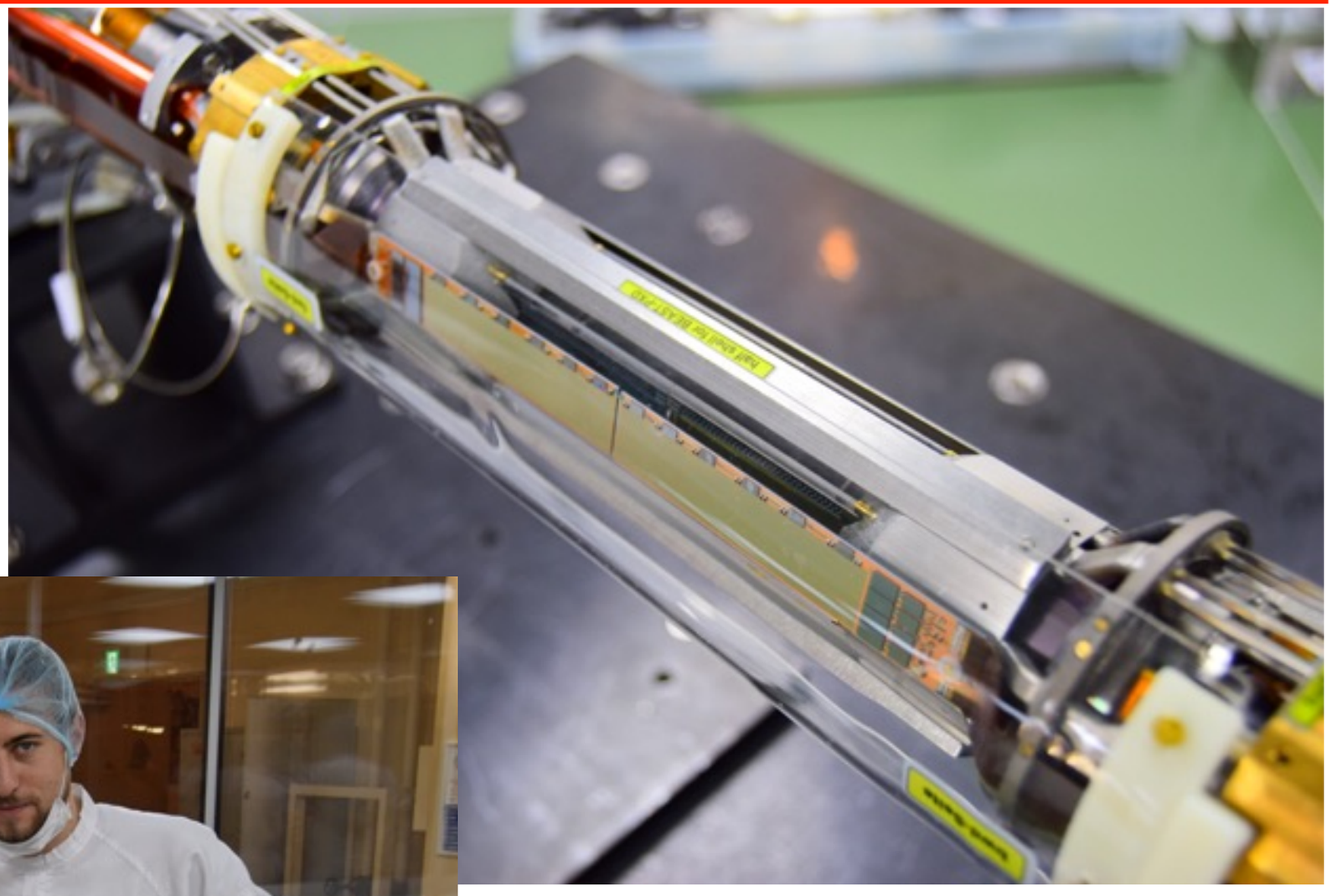
PXD transport to KEK

Clean room assembly in Tsukuba hall

Phase 2 beam pipe ready to receive BEAST II

BEAST II Assembly at KEK

PXD modules mounted on beam pipe



CLAWS + FANGS mounted as well

Plume to be installed today

SVD cartridge installation next week

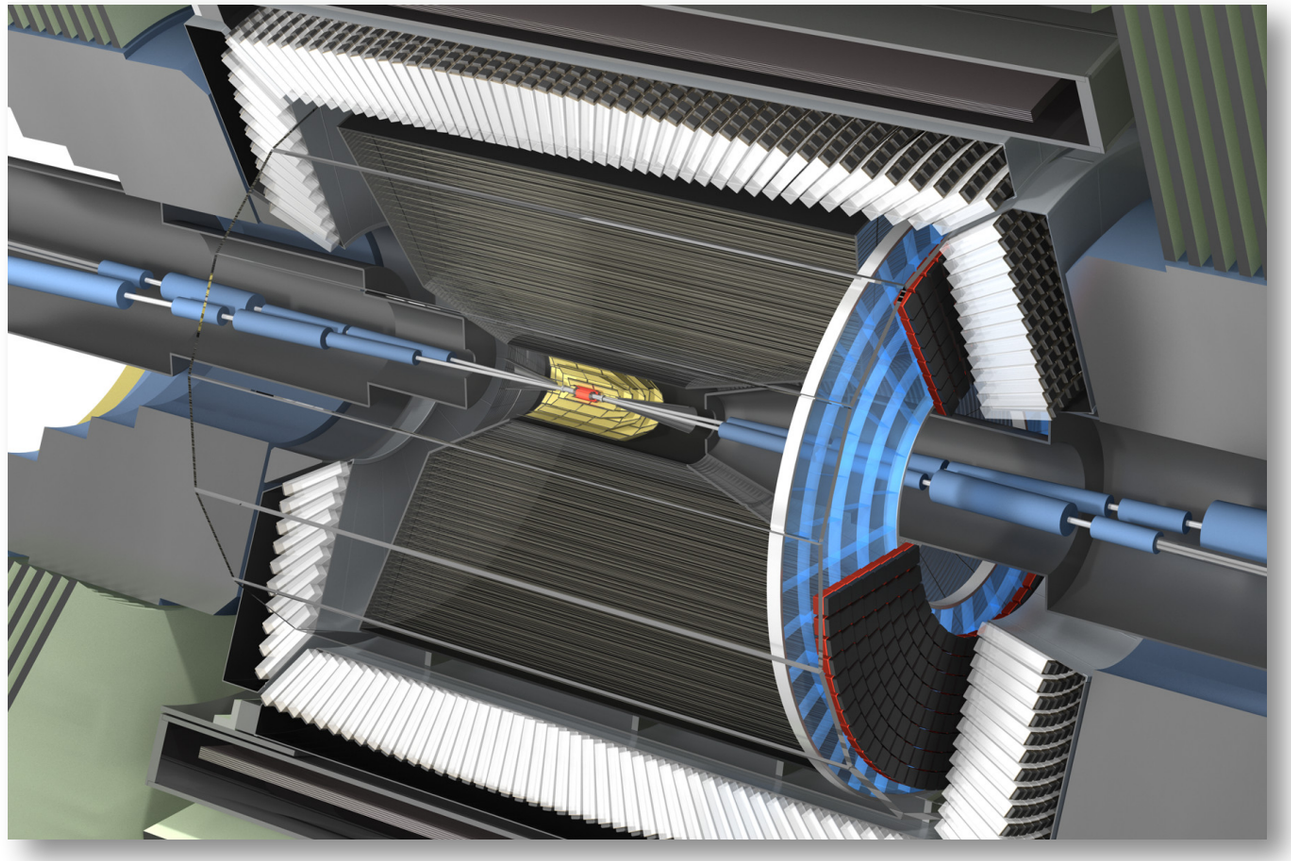
Summary

- Status of phase 2 preparations
  - BEAST II detector successfully pre-commissioned in Europe
  - Assembly of Loss Mon., PXD, FANGS, CLAWS, Plume & SVD on beam pipe currently well on schedule in Tsukuba hall B4
  - VXD installation into Belle II in November
  - First collisions with Nano beam scheme: March 2018
- Status of phase 3 preparations
  - PXD
    - Module production ongoing, ladder assembly/testing in qualification step
    - Half-shell assembly and commissioning will start in November at DESY
  - SVD
    - Ladder production in full swing
    - Important milestone reached: Start of integration of ladders to half-shells
  - Common VXD infrastructure
    - CO_2 cooling system IBBelle successfully installed and commissioned
    - VXD installation procedure verified with VXD dummy and B-field mapper
    - Clean room for VXD assembly installed in Tsukuba hall
    - Remote Vacuum Connection Systems delivered to KEK, test installation on QCS in Sep

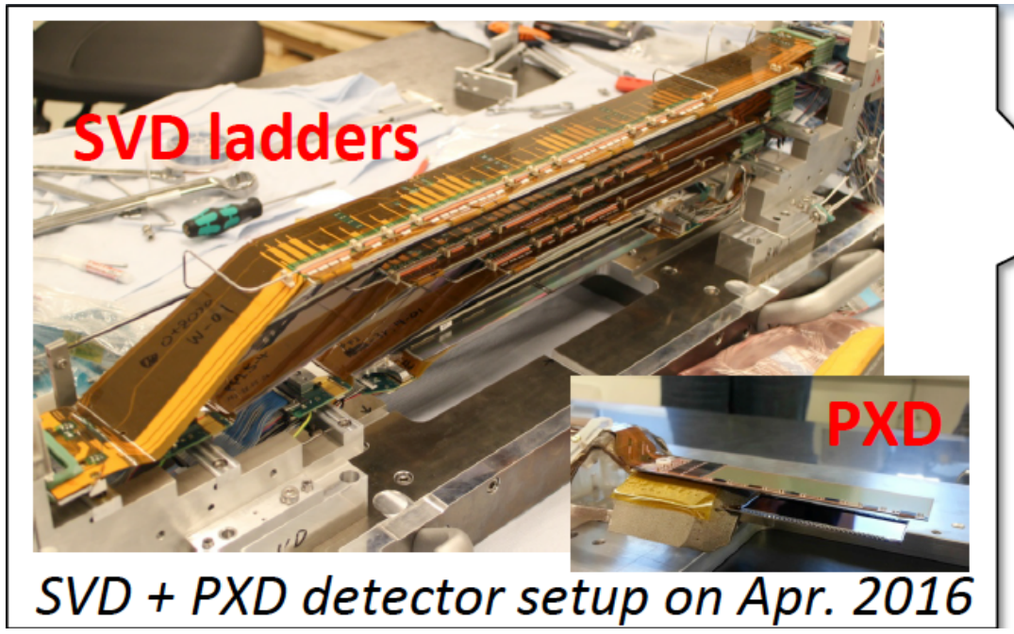
Backup

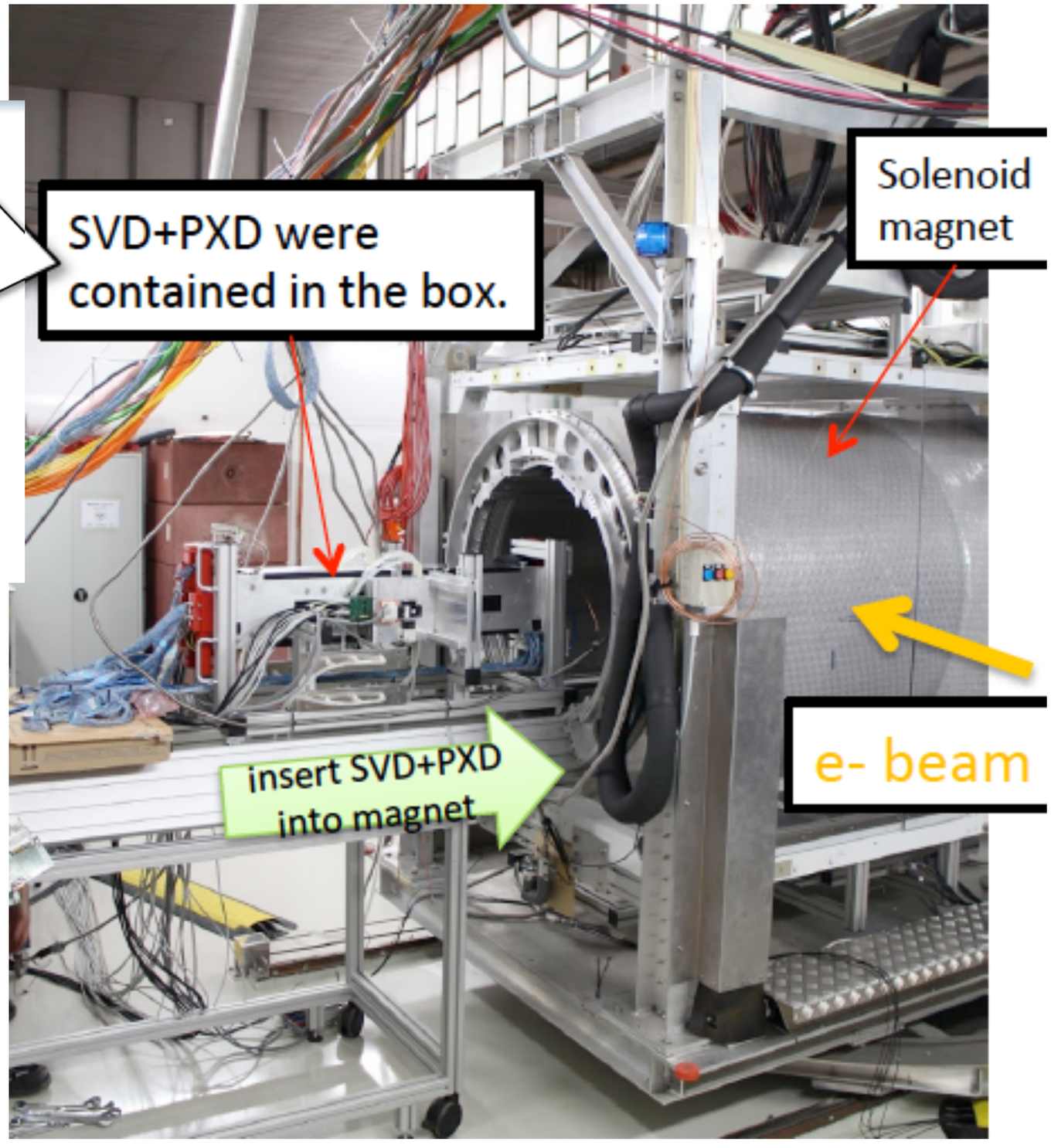
Improvements of Belle II versus Belle

- Smaller beam pipe radius allows to place the innermost PXD layer closer to the Interaction point (r = 1.4 cm)
  - significantly improved vertex resolution (compensate for reduced $\beta\gamma$ by factor 1.5)
- New PXD is part of the vertex detector with larger SVD and larger CDC
  - increased K_S efficiency, improved vertex and timing resolution, better flavor tagging
- PID: TOP and ARICH
  - better K/π separation covering the whole momentum range
  - fake rate reduced by factor 2-5
- ECL and KLM consolidation
  - improvements in ECL and KLM to compensate for larger background
- Improved hermeticity
  - geometry and reduced boost
- Improved trigger and DAQ
  - 30 kHz L1 rate
  - 10 kHz HLT output rate (300 kB/evt)
  - => need substantial computing resources



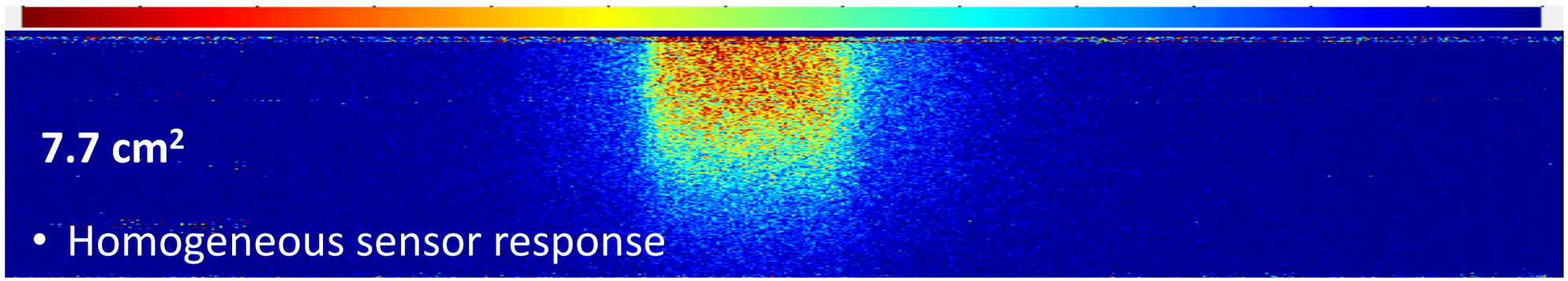
VXD Beam Tests at DESY





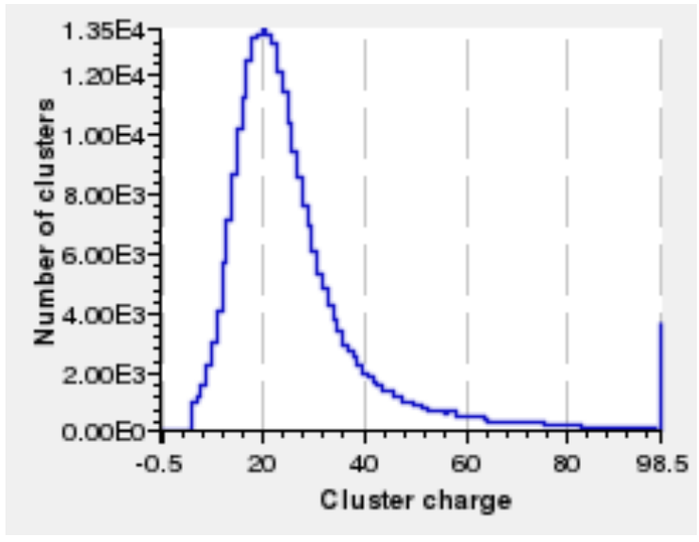
- e^- beam (2-5 GeV) at DESY in Apr 2016 **and again Feb 2017**
  - ➢ All L3-6 SVD ladders
  - ➢ + combined with PXD

PXD Performance in Beamtest



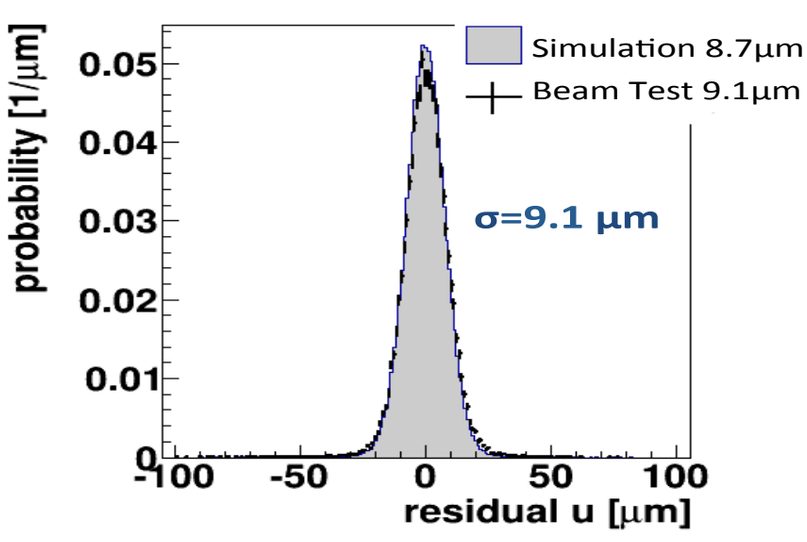
- Homogeneous sensor response

Threshold ~ 1200 electrons

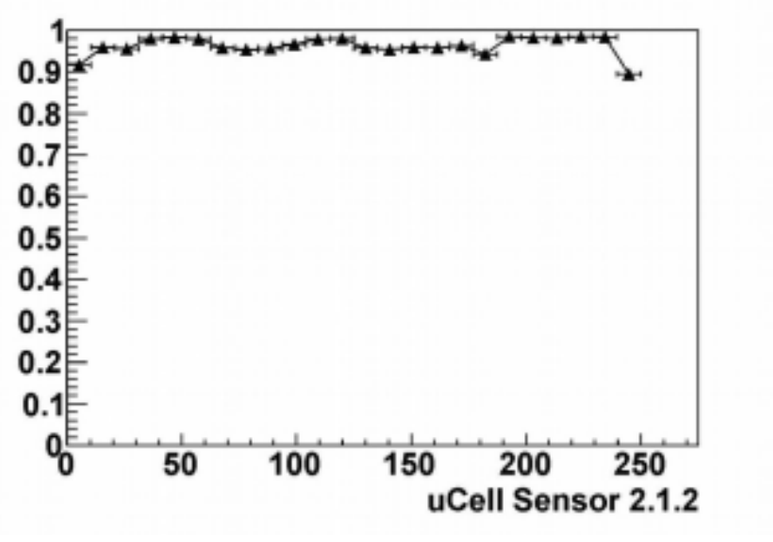


- SNR ~ 30

30° tilt: many 2 pixel clusters



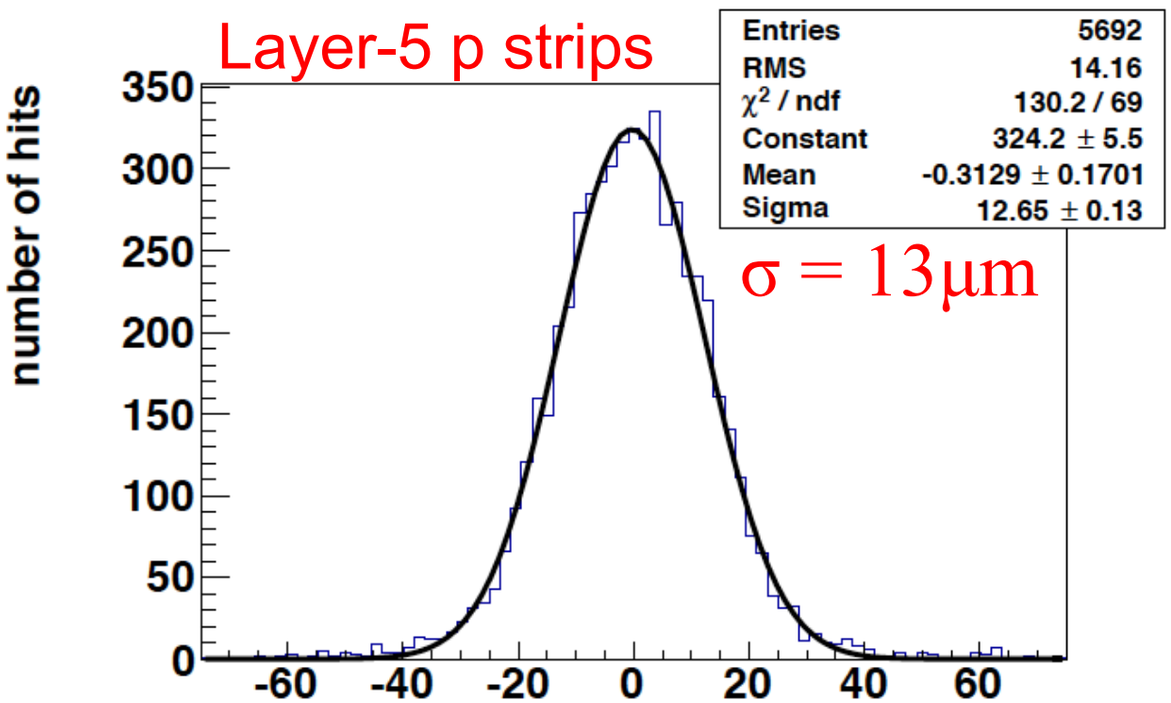
- σ = 9.1μm

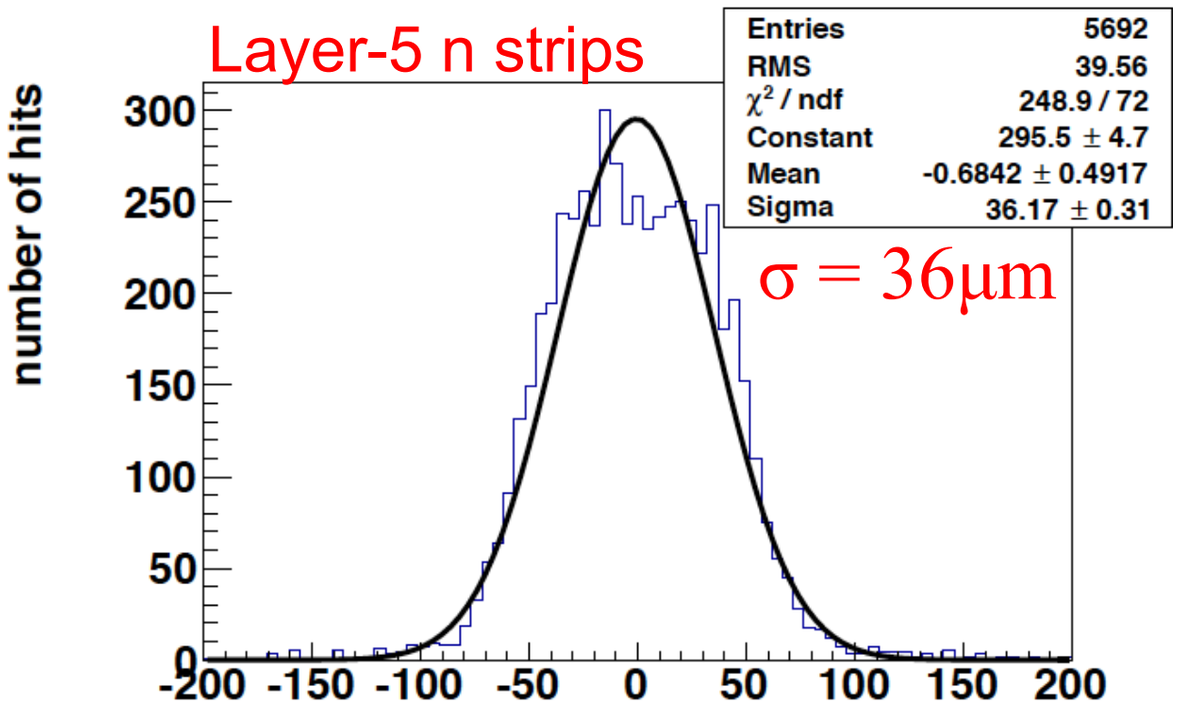


- ε > 99%

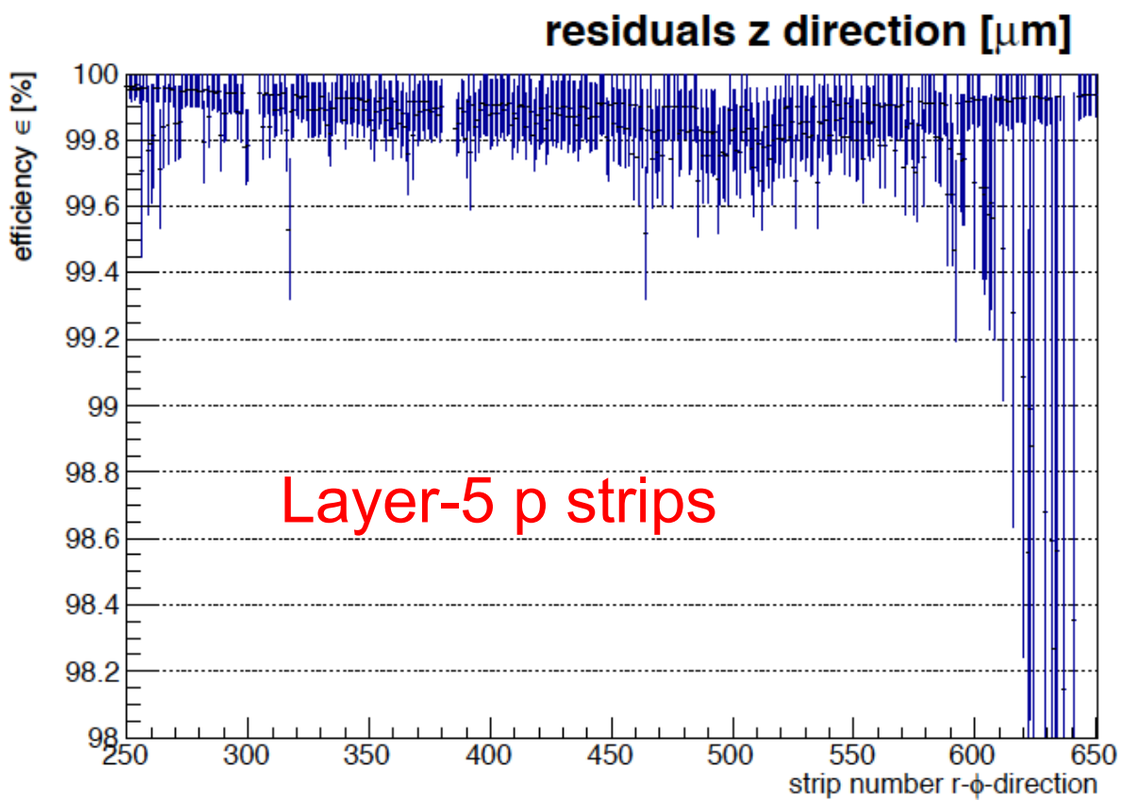
SVD Performance

- Very good spatial resolution: consistent with expectations



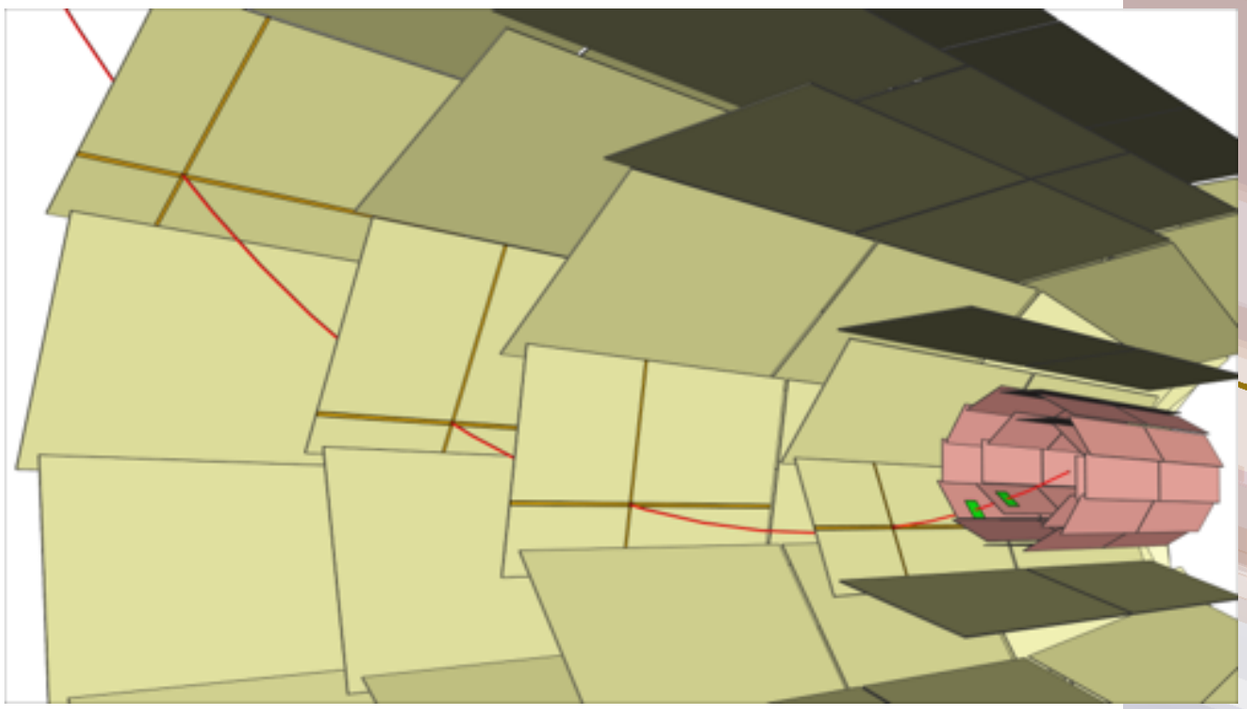


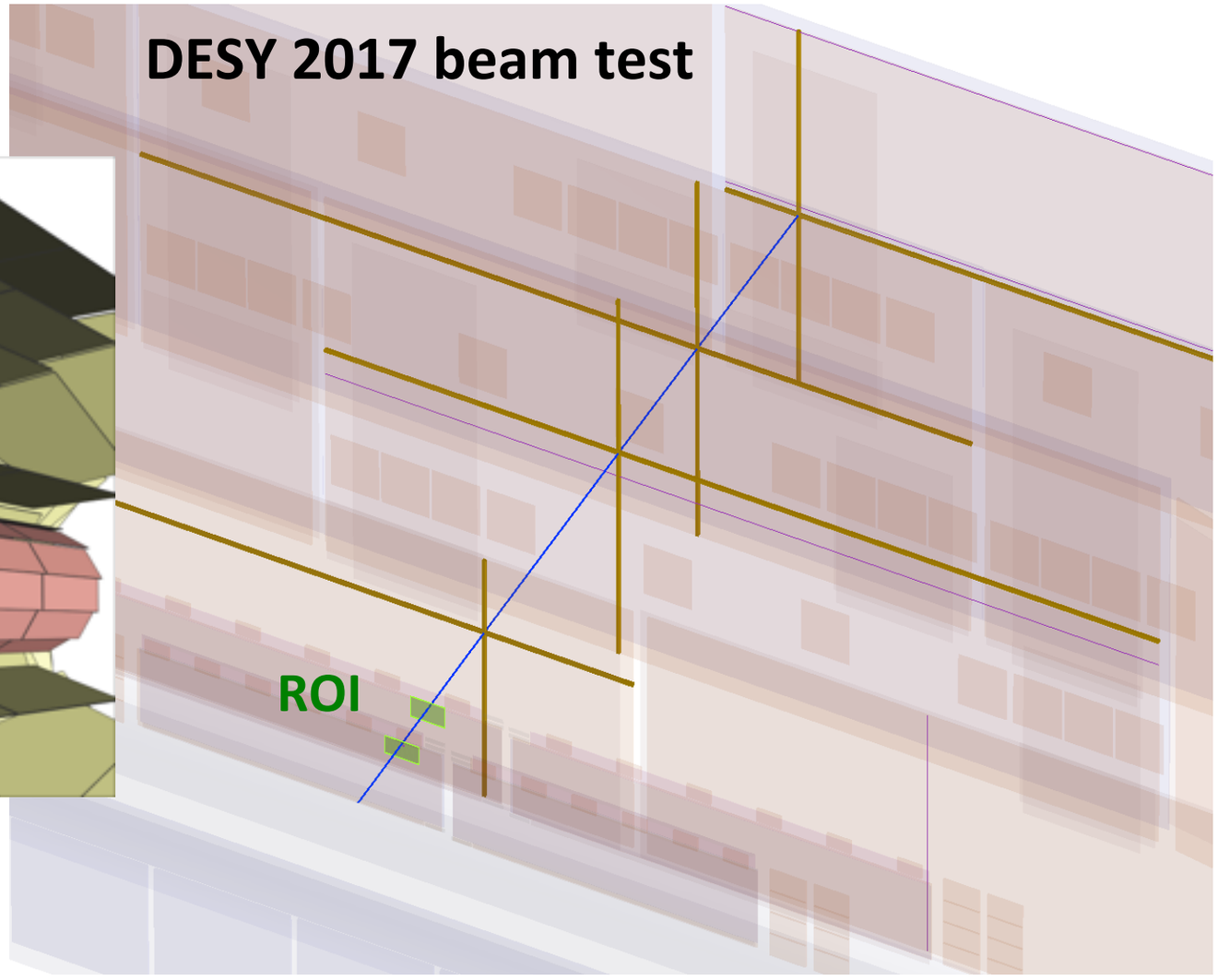
- Excellent strip hit efficiency: > 99%



PXD Online Data Reduction (ROI)

SVD track reconstruction, **extrapolation to PXD** and **Regions-of-interest finding**
performed by High Level Trigger (software) and DATCON (FPGA)





- Data reduction performance:

  ROI efficiency above 97% (small ROIs: 2.5×2.5 mm^2) for **data reduction factor > 10**