Characterisation of prototype SiGe monolithic pixel detectors for the TT-PET project

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On behalf of the TT-PET Collaboration

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CERN

UNIVERSITÉ DE GENÈVE
FACULTÉ DES SCIENCES
Section de physique

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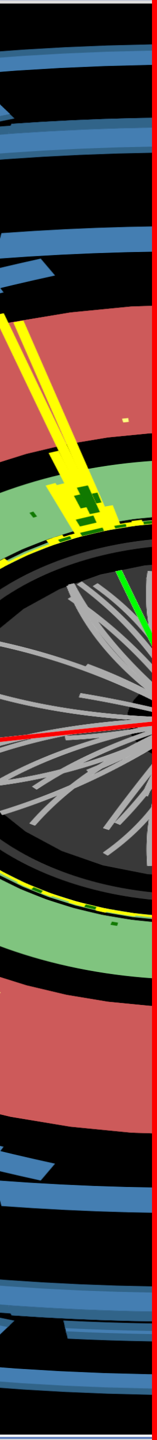

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- TT-PET Project
- Scanner Overview
- Monolithic Chip
- Test beam characterization
- TOF simulation
- Prototype-0

The TT-PET Project

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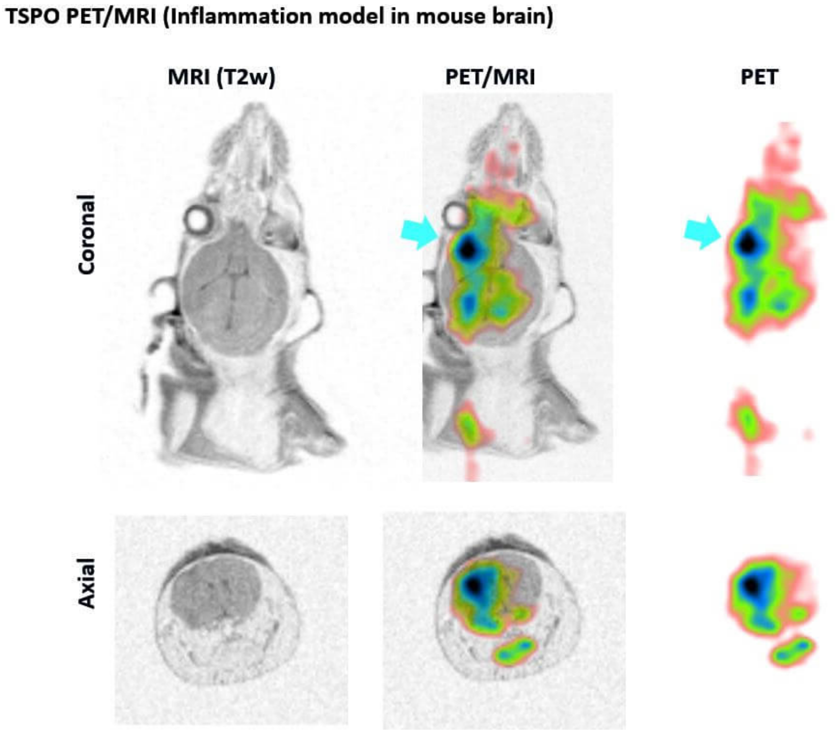
- 3-year project to produce a PET Scanner for small animals based on silicon detector technology, insertable in an MRI machine and with 30ps RMS time resolution. The project started in March 2016.

- Collaborating institutes:
  - University of Geneva
  - University of Bern
  - Hôpital cantonale de Genève
  - INFN of Roma Tor Vergata
  - CERN



Why use Time-of-Flight?

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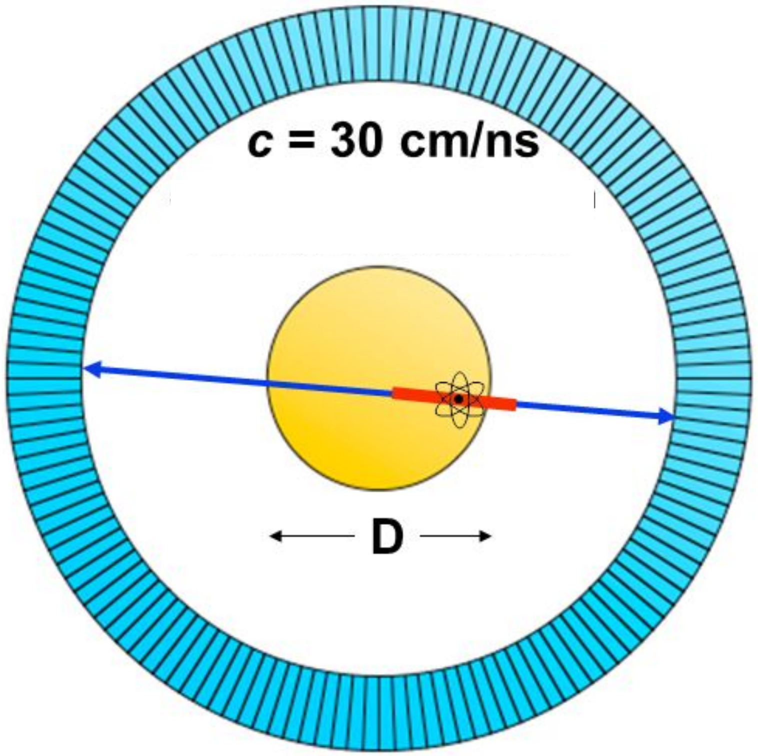
- Adding Time-of-Flight information to a PET scan can dramatically increase its performance!
- It is used to localize the source along the line of flight
- It leads to much lower noise, which can be used to increase image quality or decrease radiation dose to the patient



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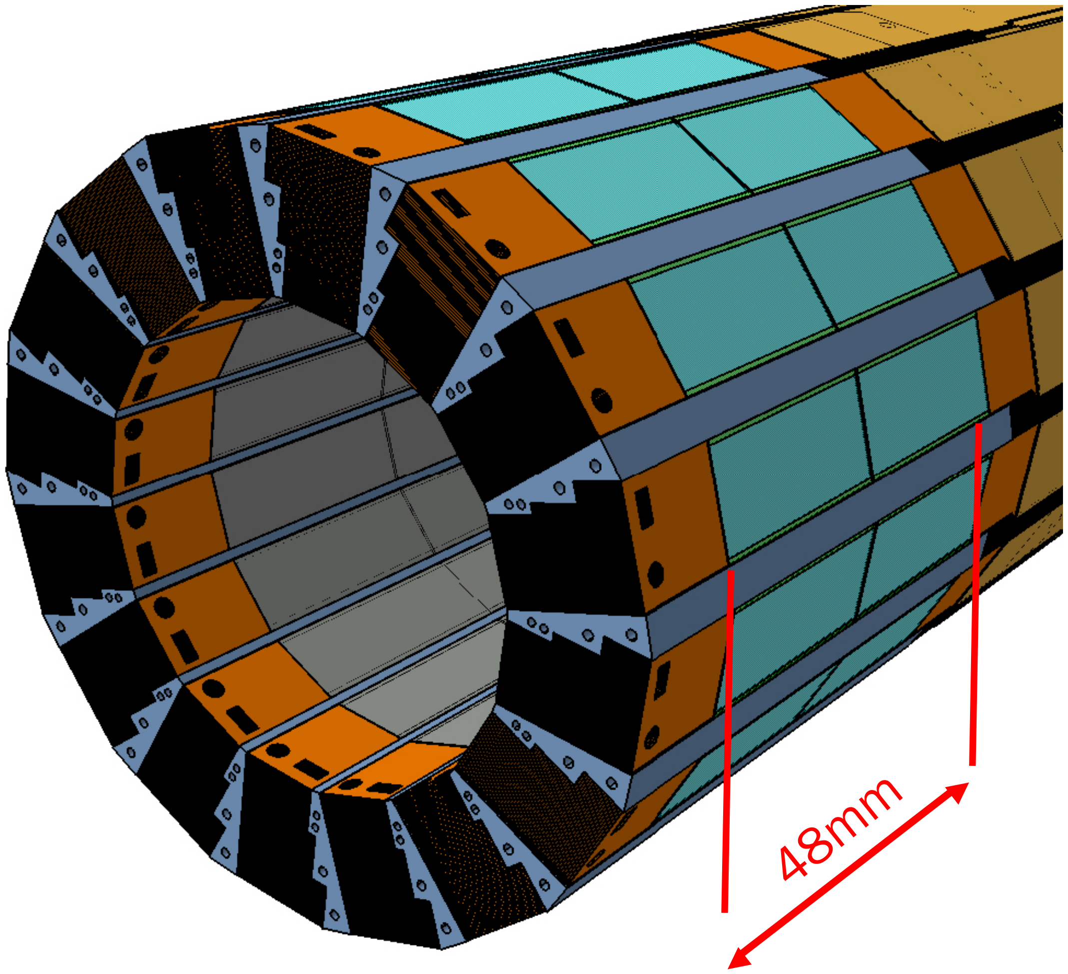
Scanner Overview

- Designed to fit inside removable RF-Coil for nanoScan 3T
- 16 sensitive towers
- 16 cooling blocks: ceramic/ 3d printed
- Exterior carbon fiber support and cooling pipes not shown
- Inner radius: 65mm
- Outer radius: 80mm
- Total Pixel channels: 1,413,120
- Pixel size: 500x500μm^2



Scanner Overview

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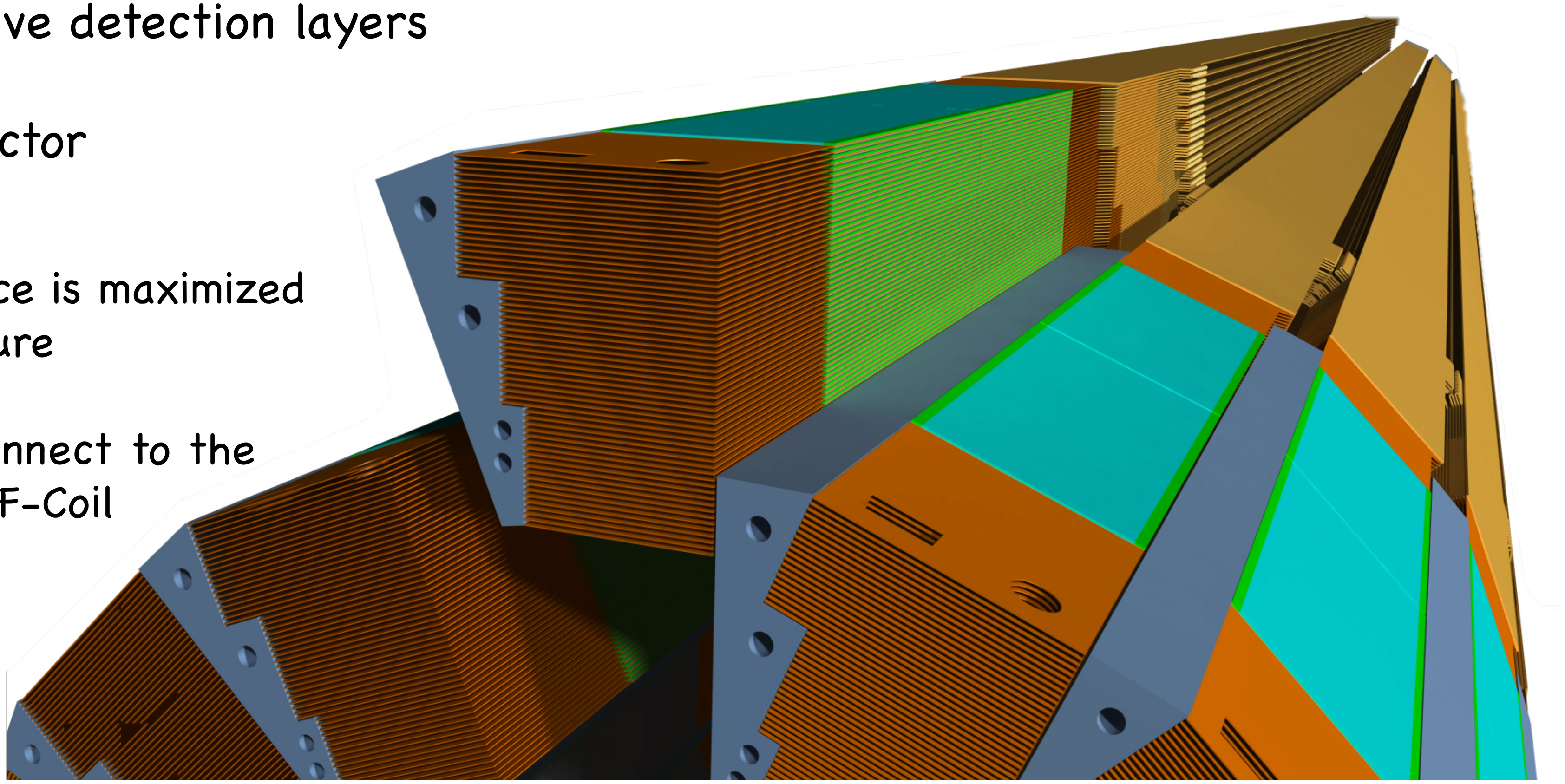
- Sensitive towers composed of many layers of lead, flex circuit, and monolithic pixels sensors
- 1 tower = 60 sensitive detection layers
- Sampling style detector
- Geometrical acceptance is maximized using step like structure
- Longer data cables connect to the DAQ outside of the RF-Coil



Single detection layer

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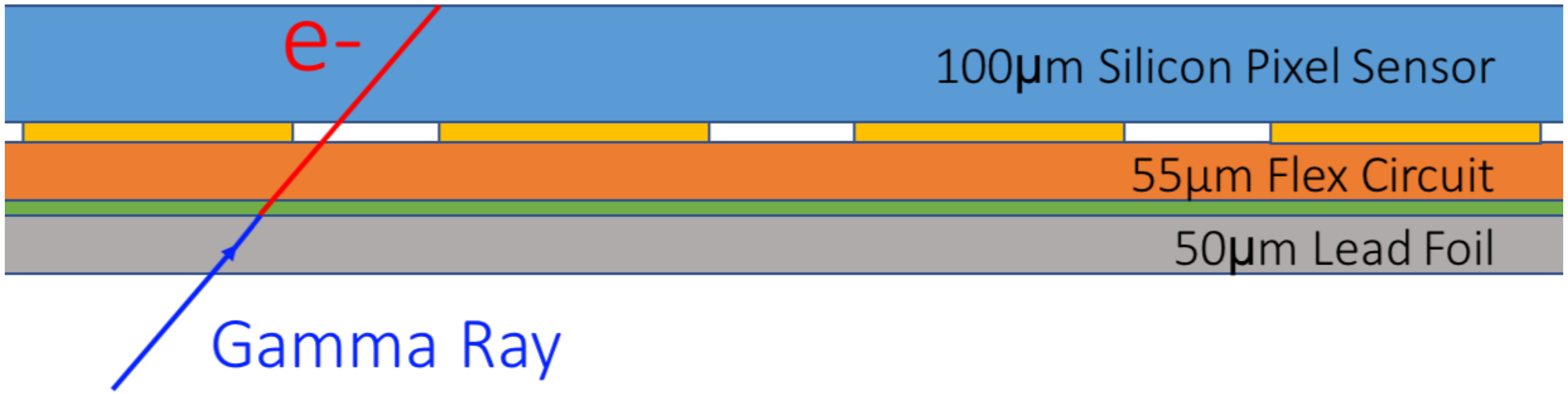

- 500x500μm pixels
- Baseline option: bump bond monolithic chip to flex circuit
- Second option: stack multiple chips on top of each other and wire bond together (same process as inside memory chips)

Single detection layer

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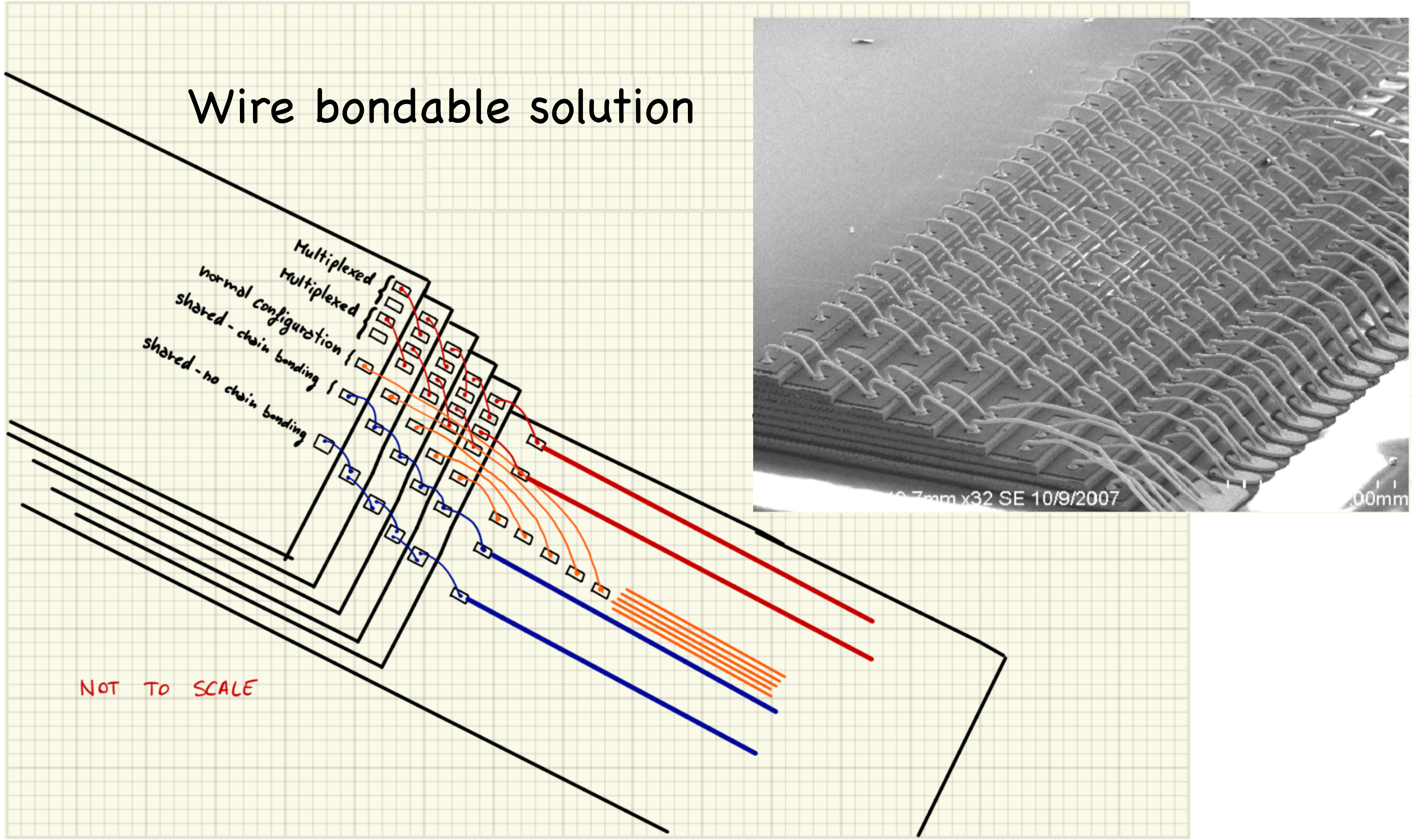

Mechanics

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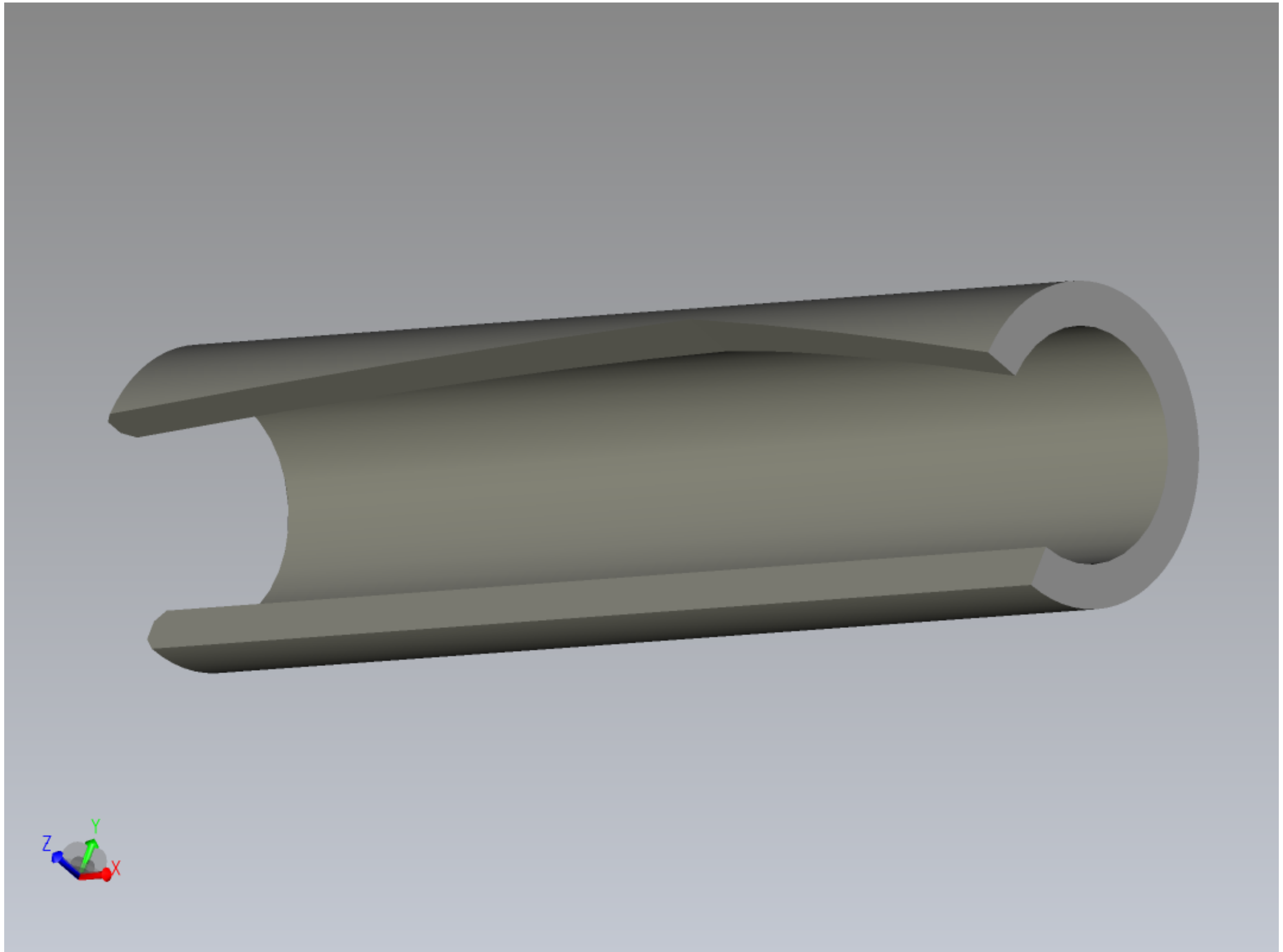

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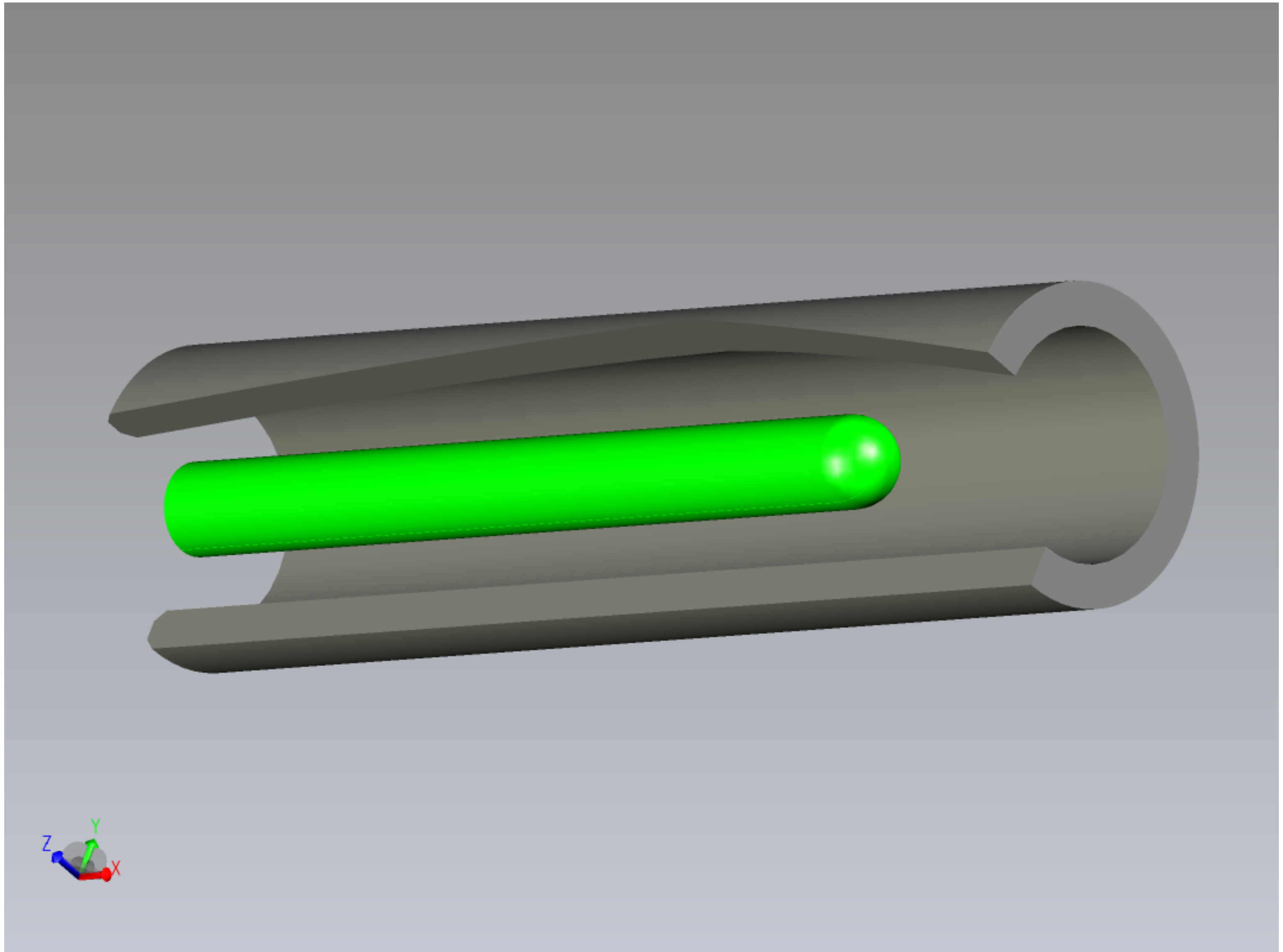

Mechanics

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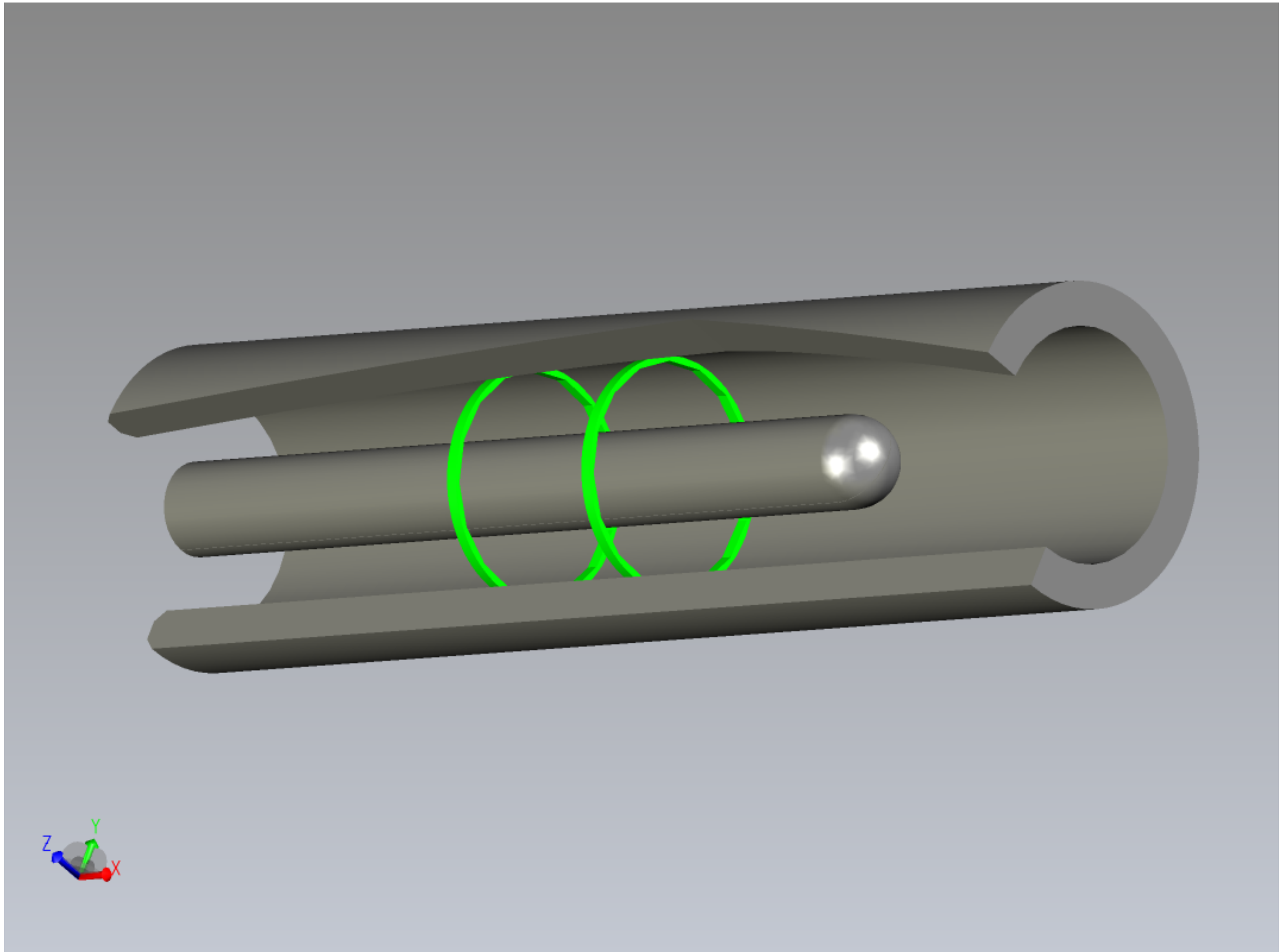

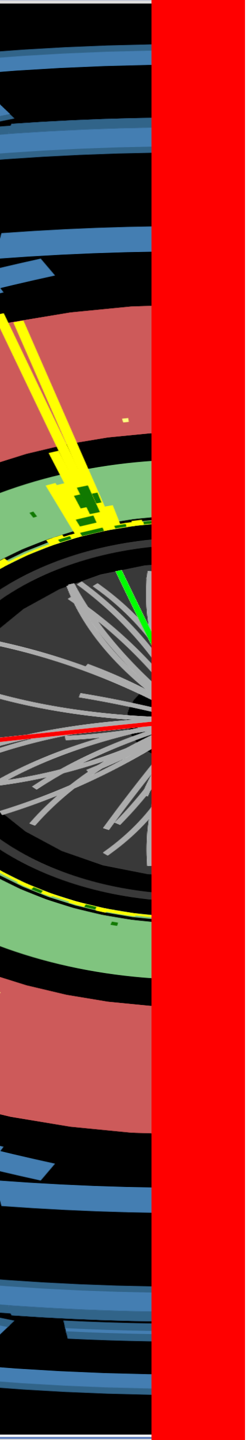

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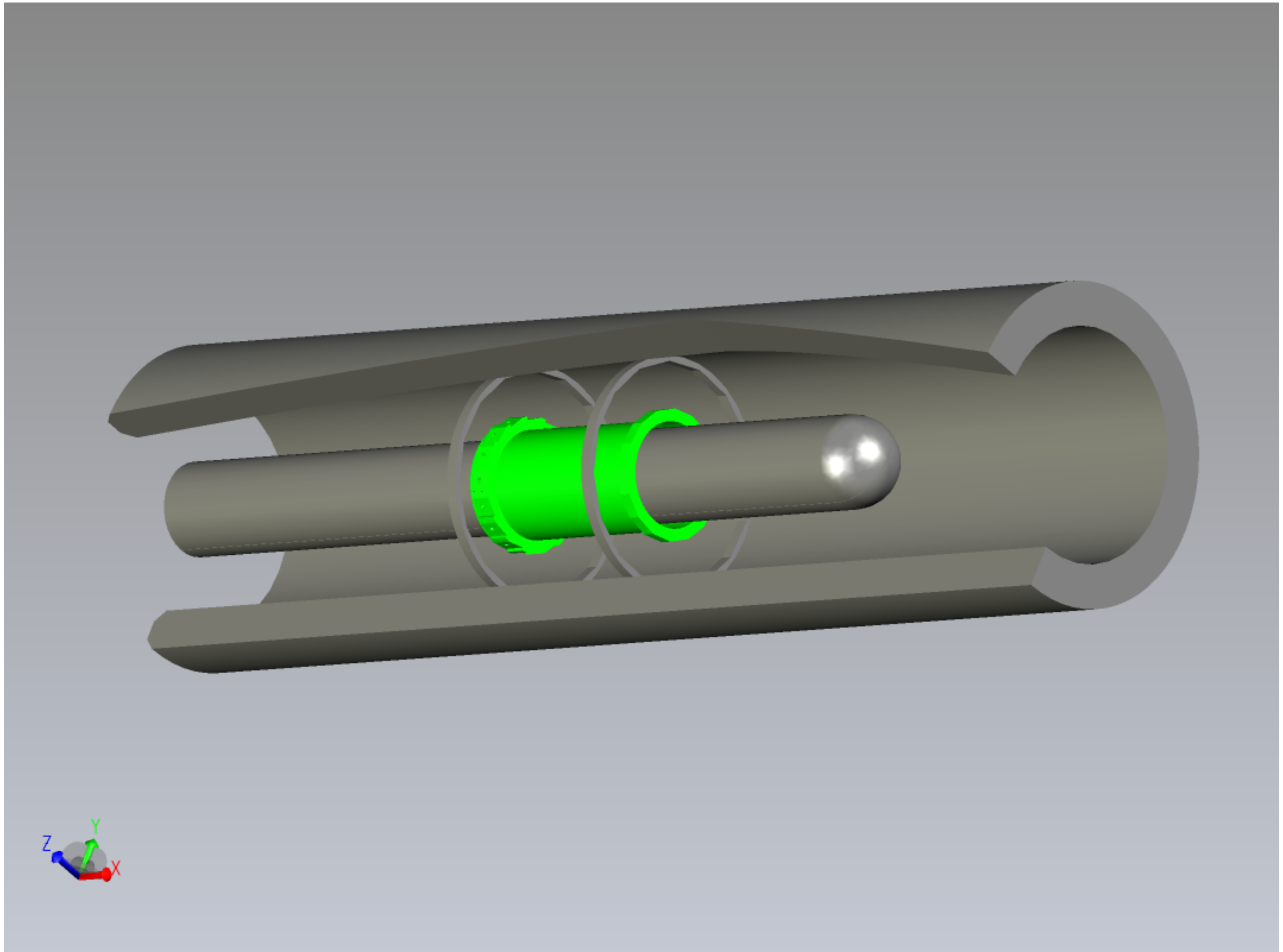

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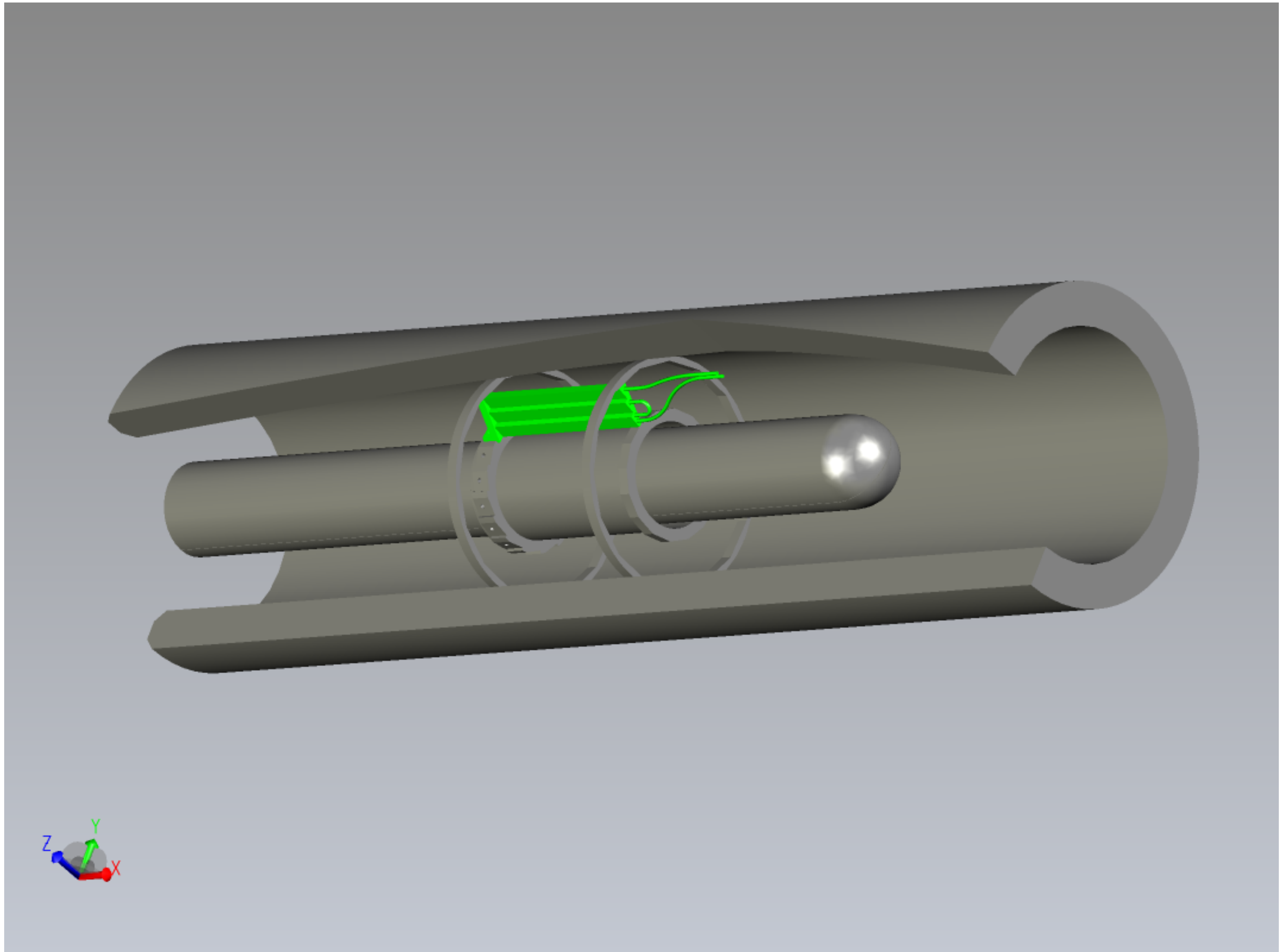

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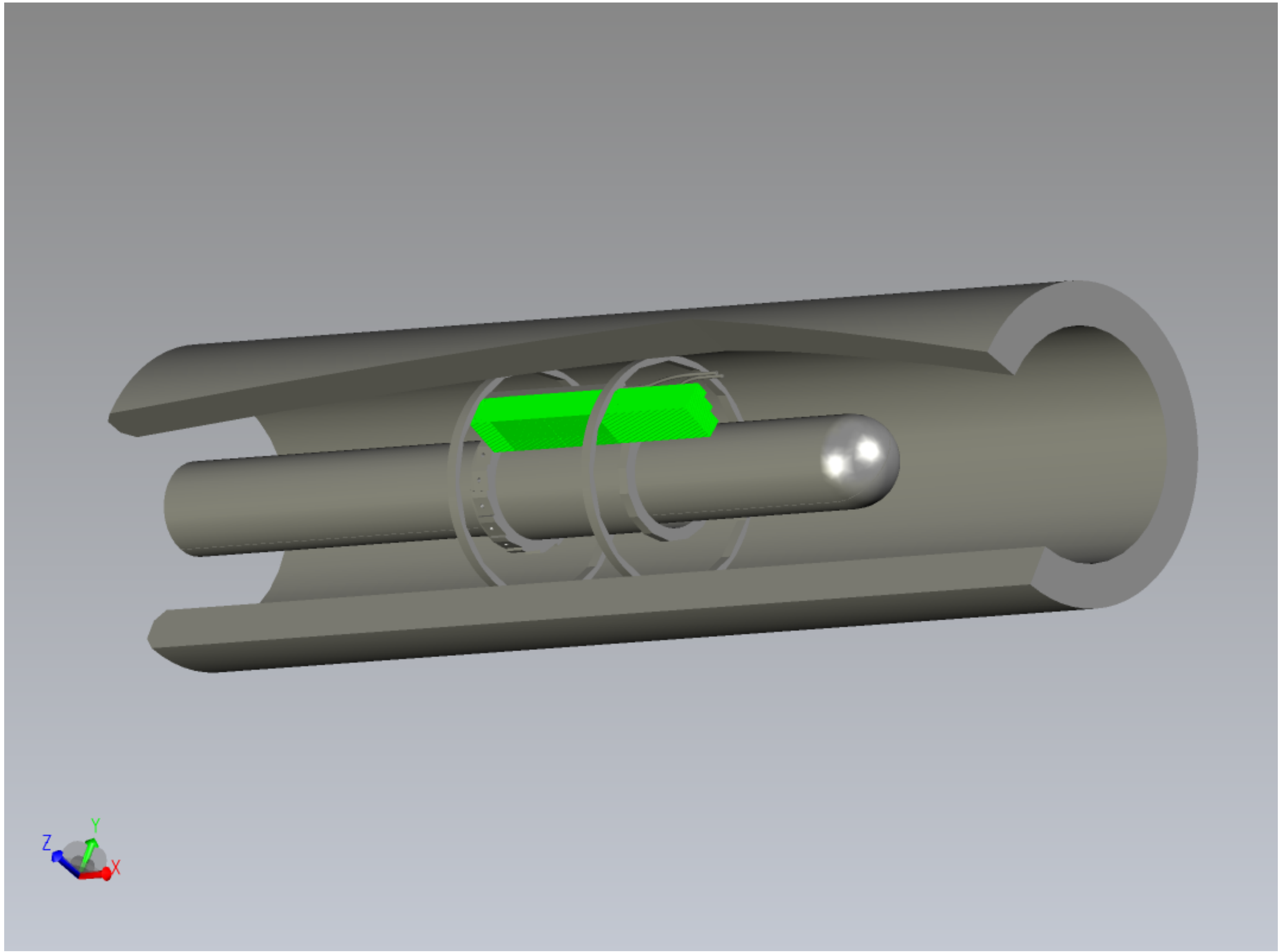

Mechanics

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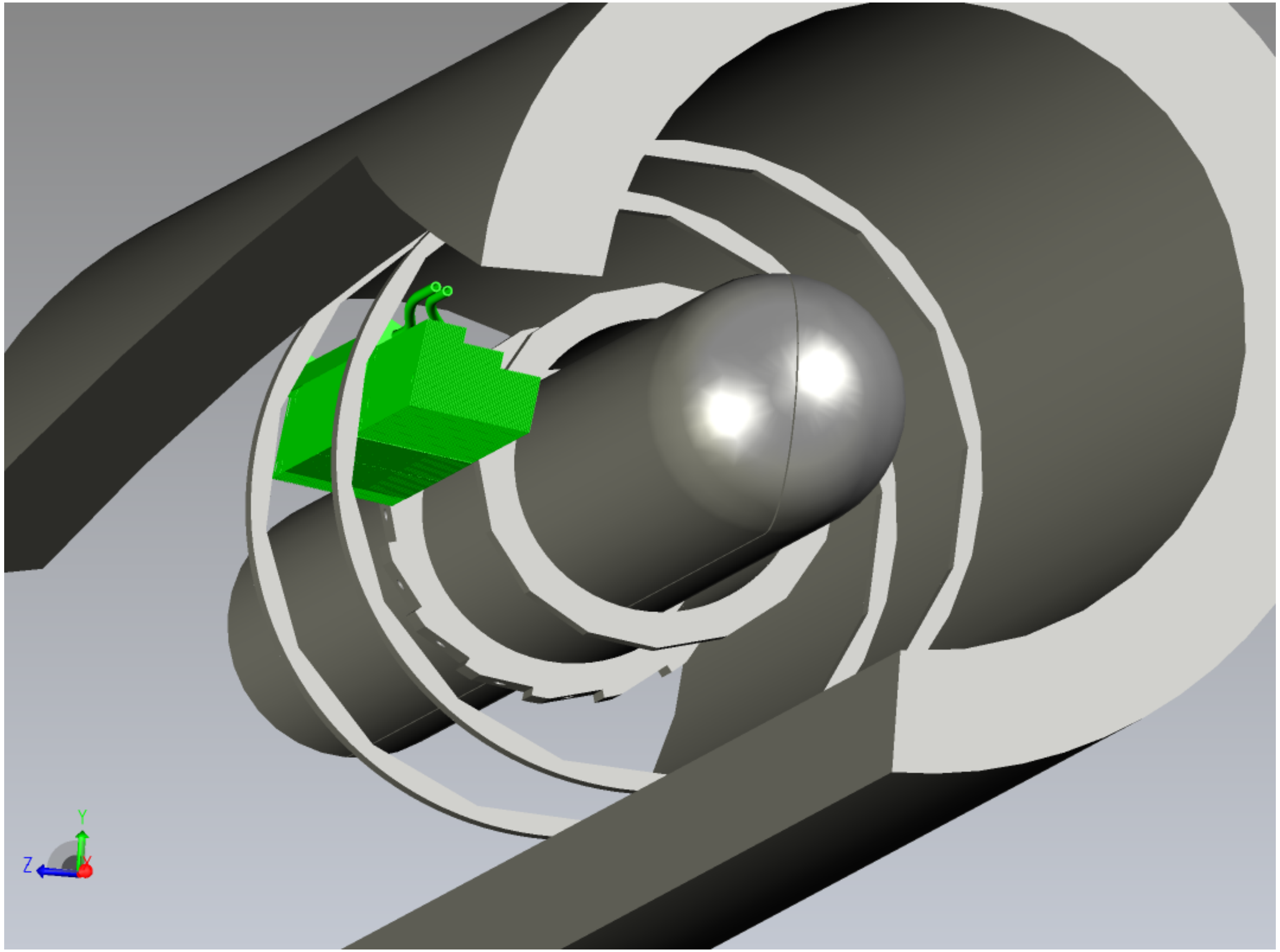

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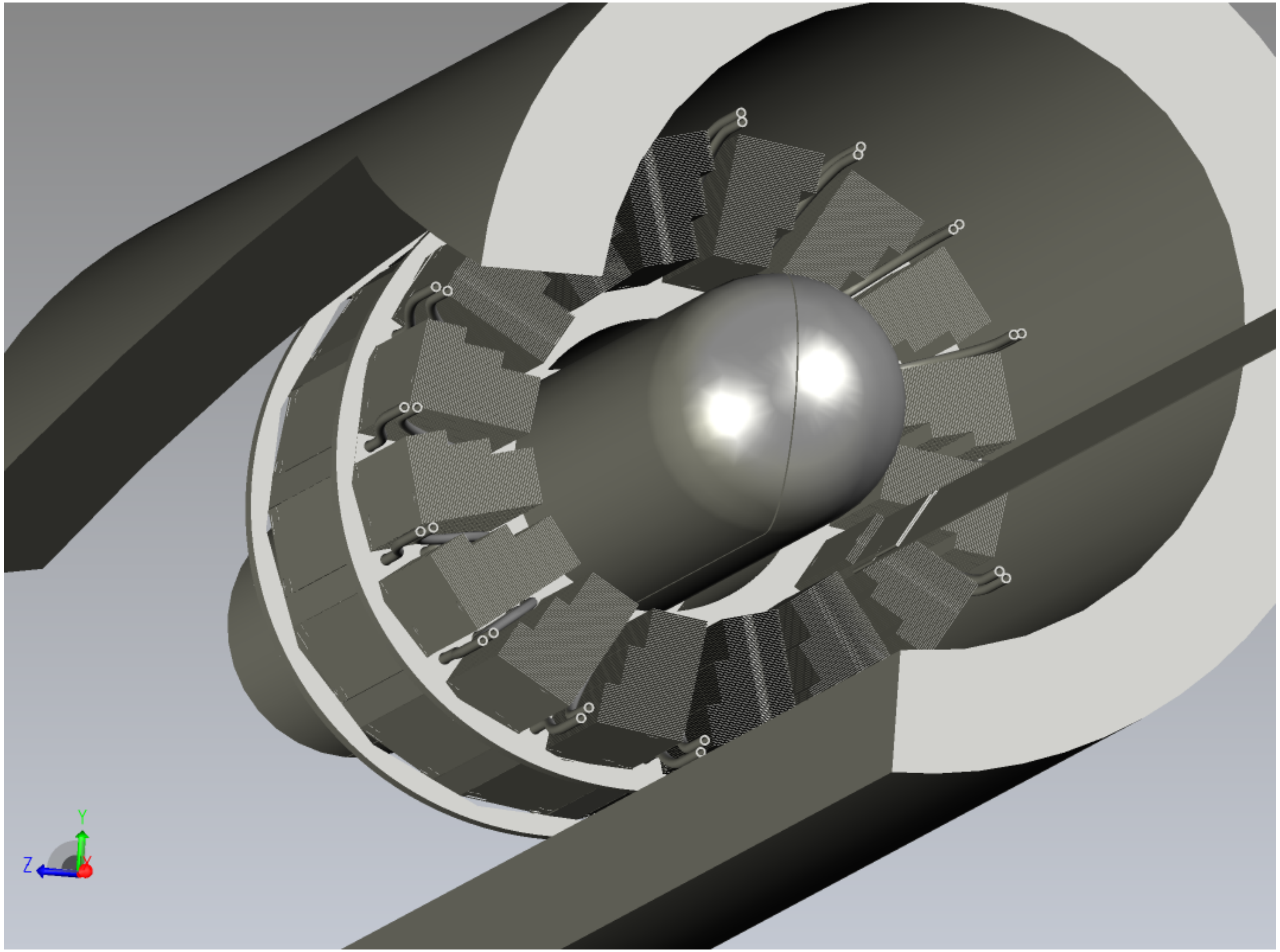

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Event Rate and Data Pressure

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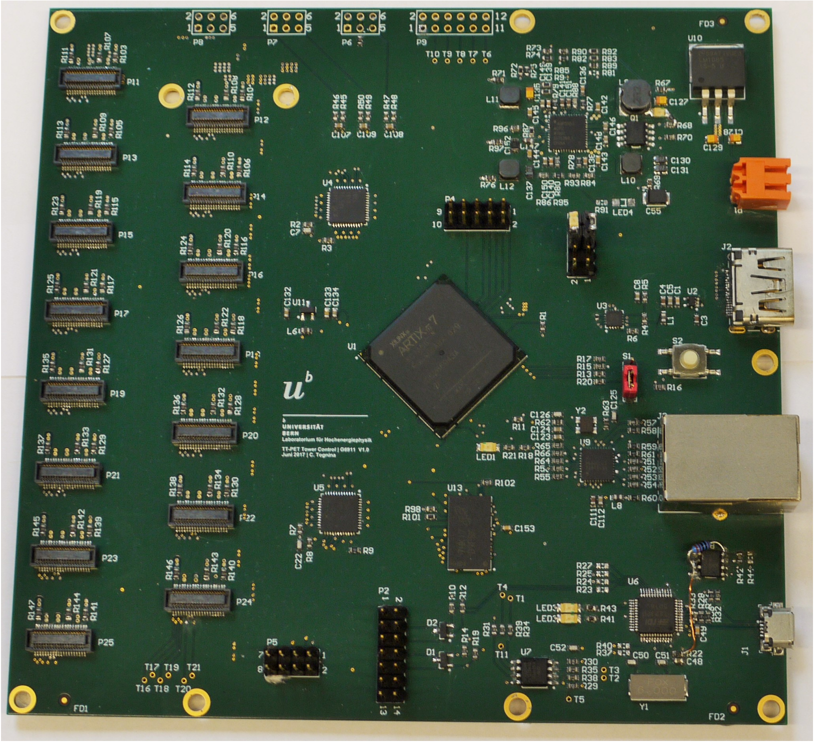
- Readout designed for 50MBq source
  - 19.2 MHz single hit rate
  - 5 MHz possible coincidences
  - 1.2 MHz real coincidences
- System designed for scalability
  - Custom Designed Tower Control board to control one Tower
  - Commercial components used where possible
  - CERN VLDB board (GBTx) used to multiplex multiple tower control DAQ boards



DAQ chain

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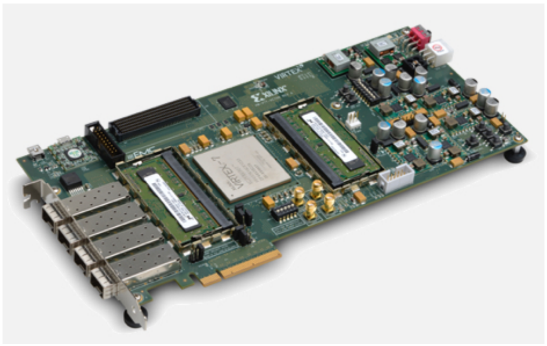
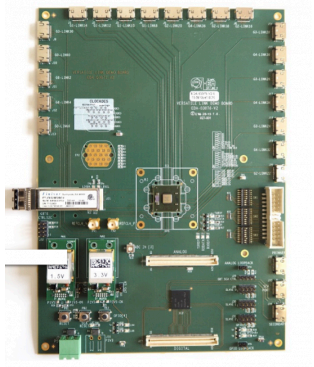
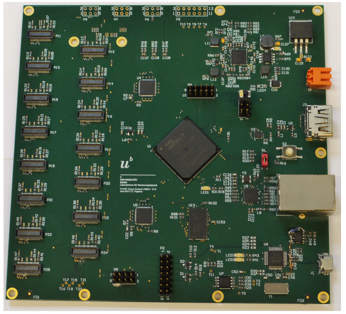
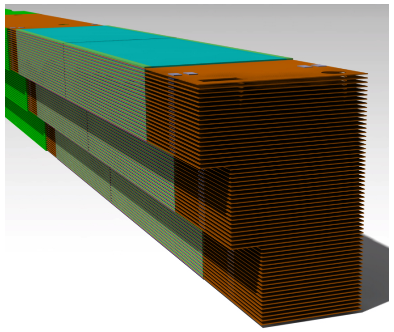
Xilinx ZC709







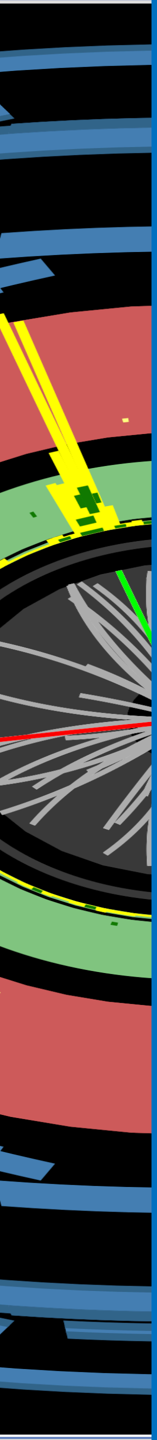


PC —PCIe— Central Trigger Processor —Optical GBTx— VLDB —Electrical— Tower Control (x16) —Electrical— Sensor Layer (60 per Tower)

Central Trigger Processor
- Control full DAQ chain
- Coincidence check
- Calibration control

VLDB
- Multiplexer
- Optical to electrical
- Clk fanout

Tower Control
- Custom FPGA board
- Temporary data storage
- Easily scalable



Pro's and Con's

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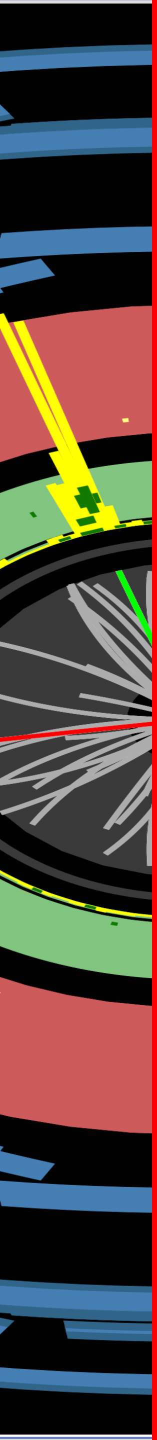
- Very high granularity, with access to DOI and TOF information for every hit
- Faster signals mean ability to have high-precision timing measurements
- The scanner can be designed to be compatible with an MRI scanner, providing combined MRI-PET images

- On the other hand…
- The mechanics of the scanner are really complex (especially the data flex)
- There are a very large number of channels, so the data acquisition scheme is critical
- Every channel must be calibrated → very long procedure



- TT-PET Collaboration
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- **Monolithic Chip**
- Test beam characterization
- TOF simulation
- Prototype-0

Monolithic Test chip

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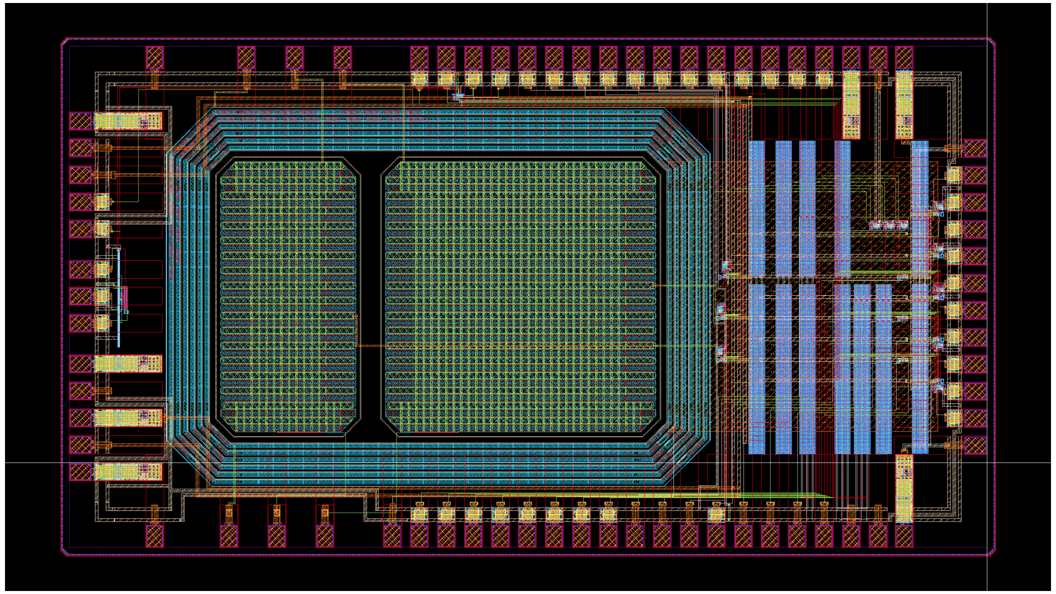
- First Monolithic Test ASIC
- SG13S SiGe BiCMOS process from IHP microelectronics (130nm)
- Very High CMOS resistivity suitability (1kΩcm)
- Test custom guard ring design and qualify HV tolerance (180V)
- 1 small pixel 900x450μm^2
- 1 large pixel 900x900μm^2
- Geometry type: n-in-p
- ToF RMS (mips): 100ps



Monolithic Test chip

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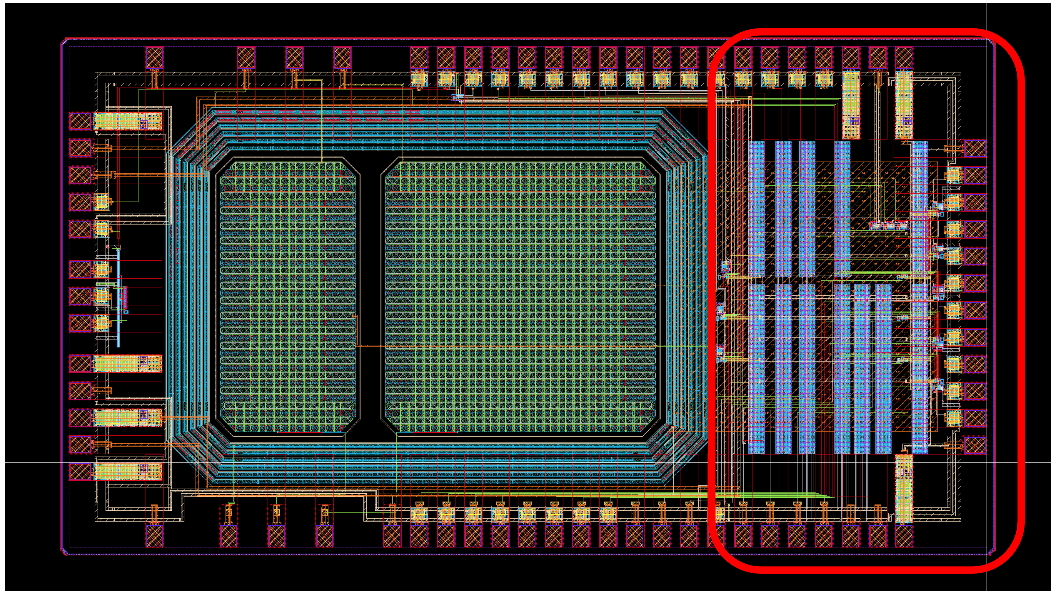
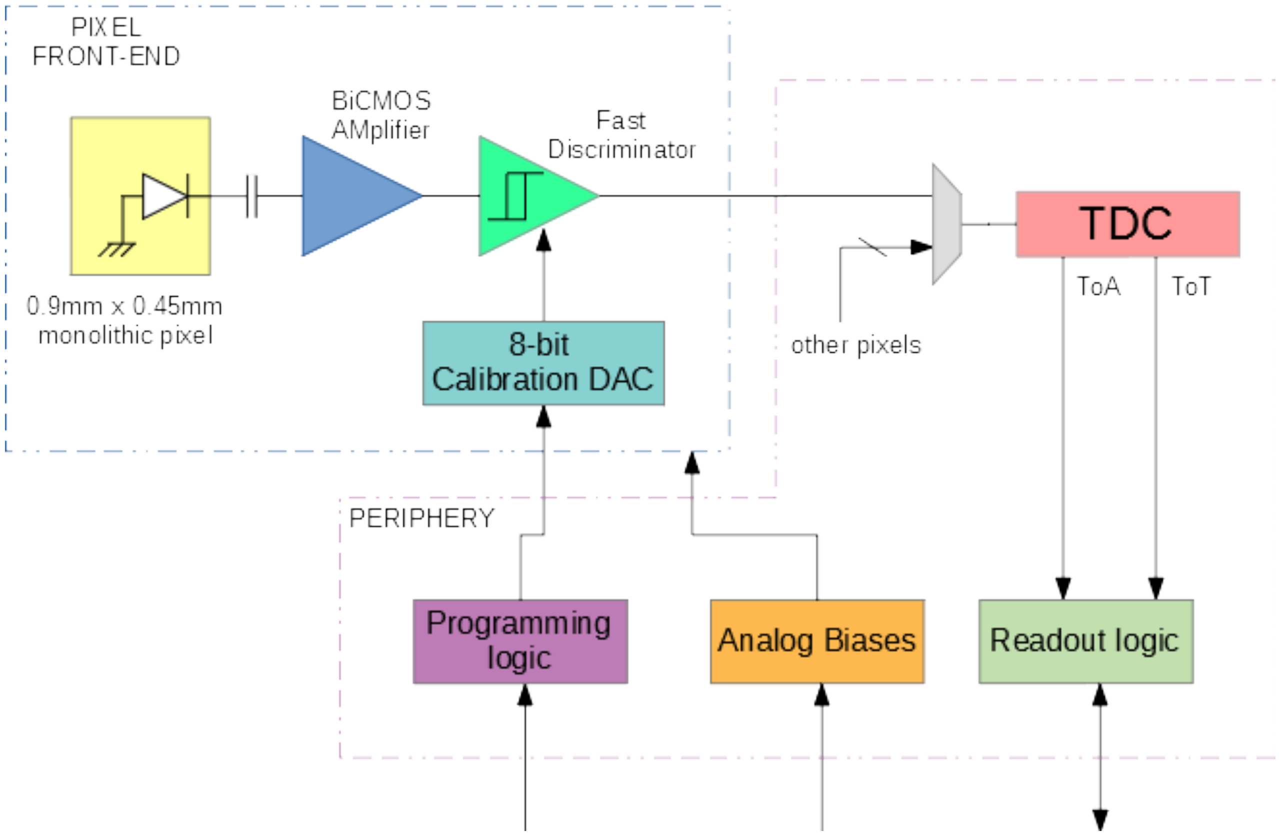
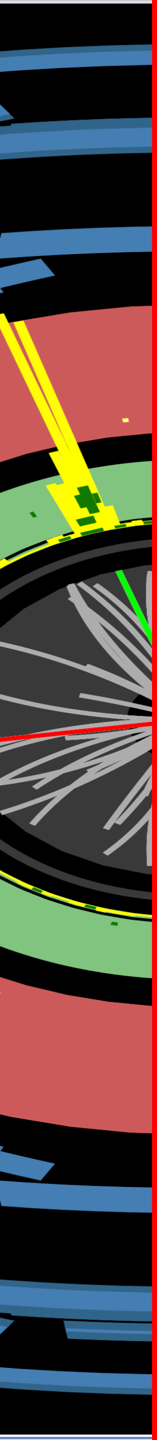
- Electronics placed outside of the pixel guard



Monolithic Test chip

- Electronics placed outside of the pixel guard
- SiGe pre-amplifier
- Amplifier rise time 1-2ns
- Discriminator
- Time-over-Threshold measurement





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- TT-PET Collaboration
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- **Test beam characterization**
- TOF simulation
- Other prototypes

Test beam setup

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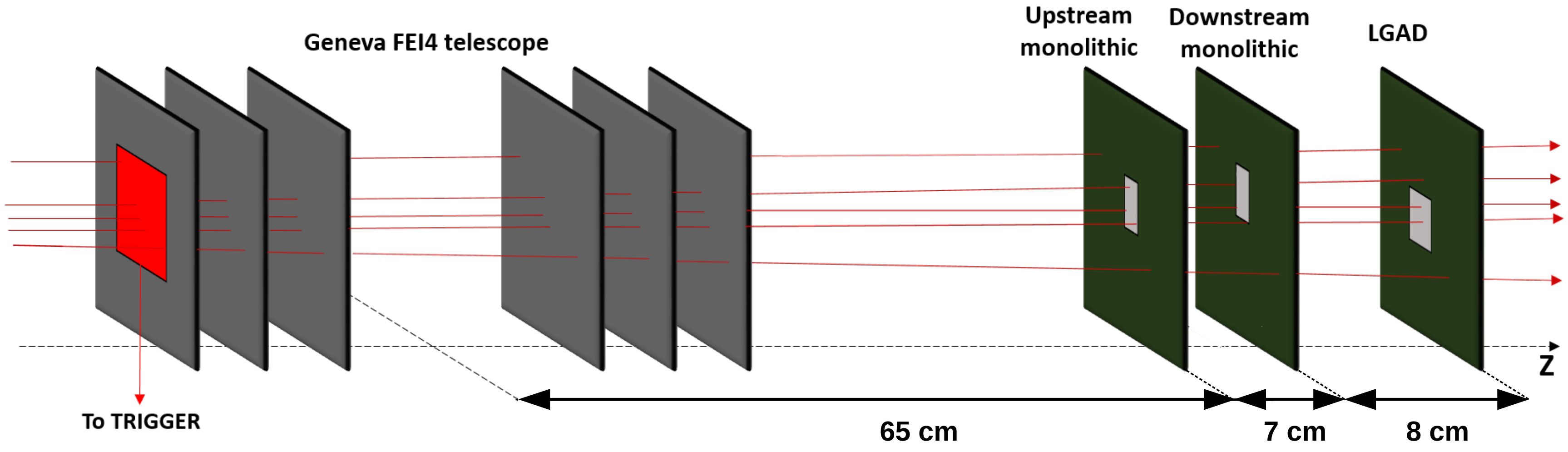
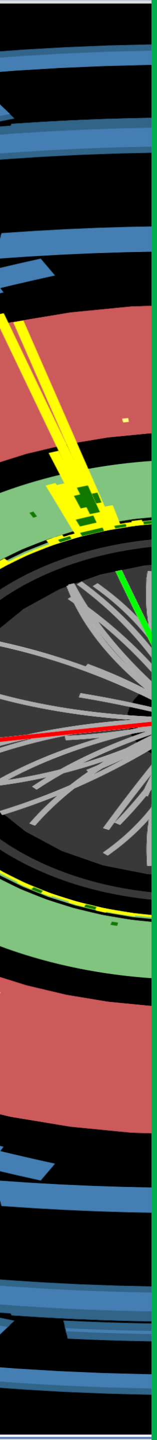


- 180 GeV/c pion beam used (CERN SPS beamline)
- Particle telescope (Geneva FE-I4 telescope) used for tracking
- 2 Monolithic test chips operated at 180V (backside not metalized, and referenced to Gnd)
- LGAD sensor used as final plane (timing reference)



Efficiency result

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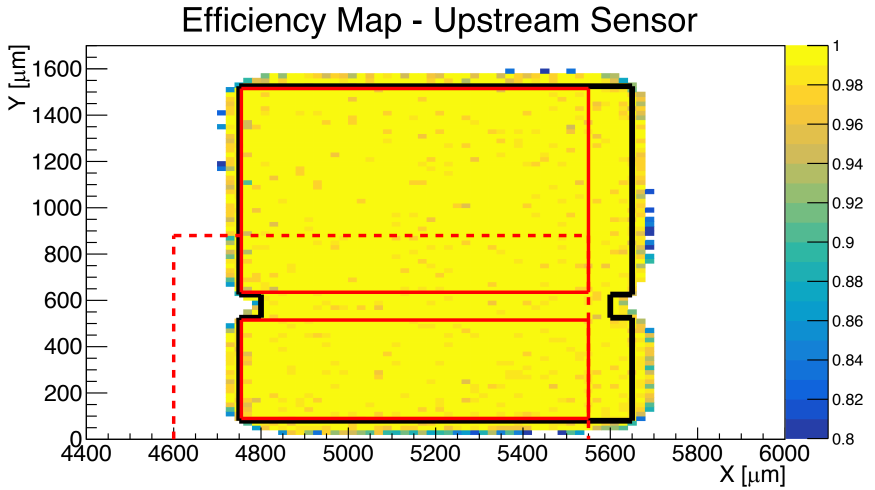
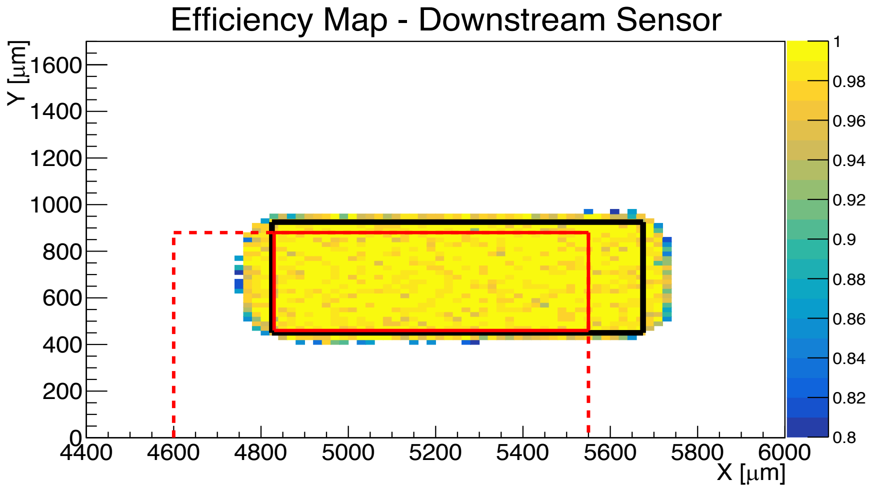
- Overlap region (red dashed box)
- Only particle tracks that intersect this ROI are used
- Upstream Sensor efficiency (99.79 ± 0.01)%
- Downstream efficiency (99.09 ± 0.04)%
- No areas of large inefficiency





Charge Uniformity

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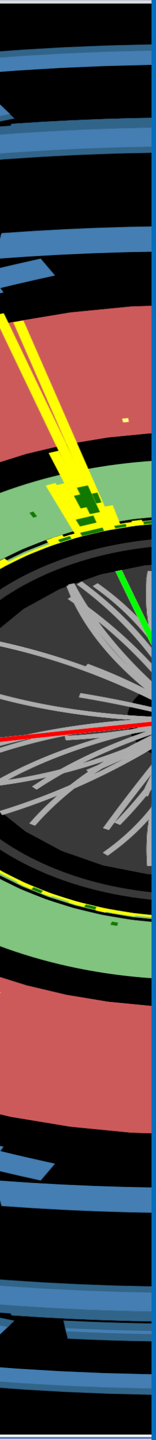
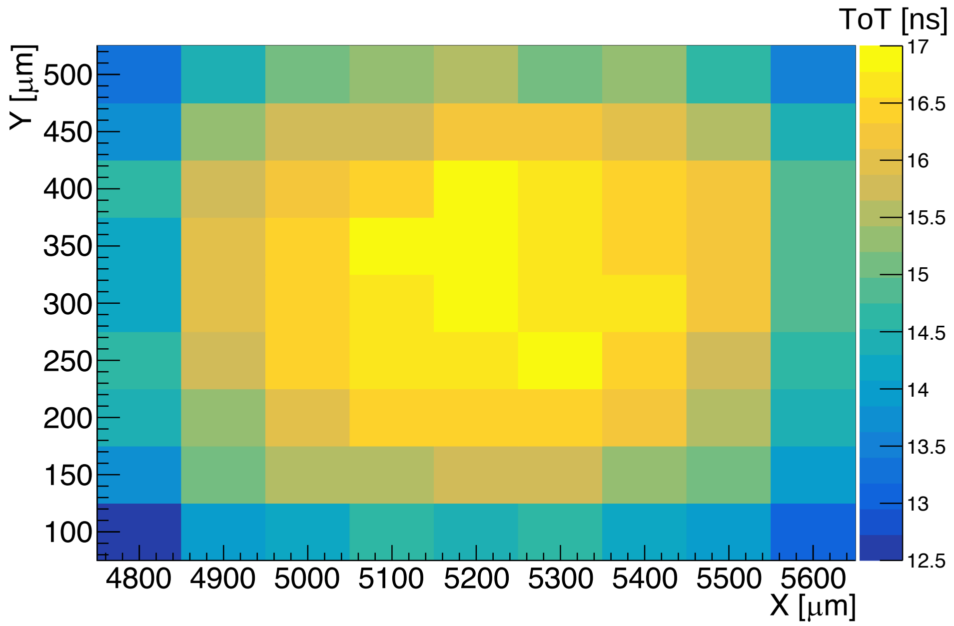
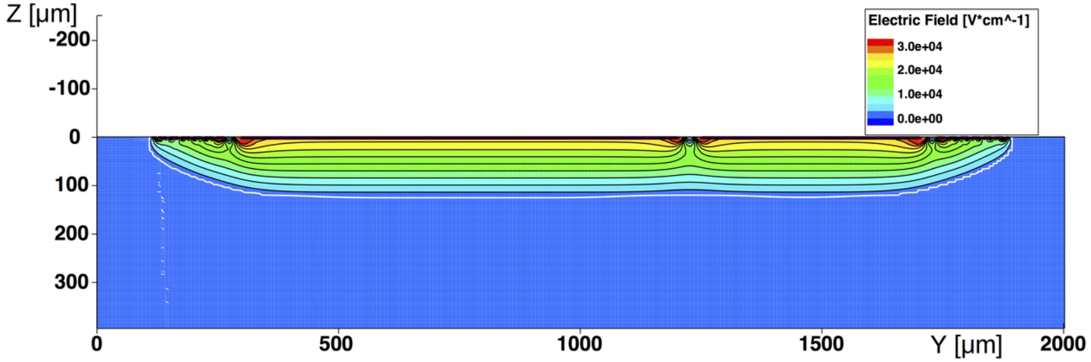
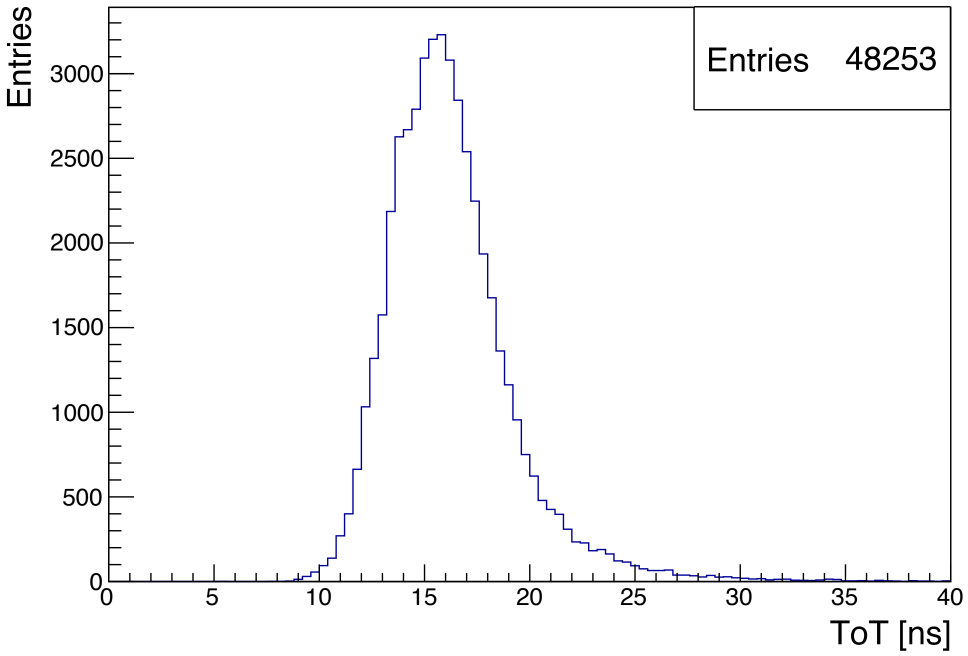


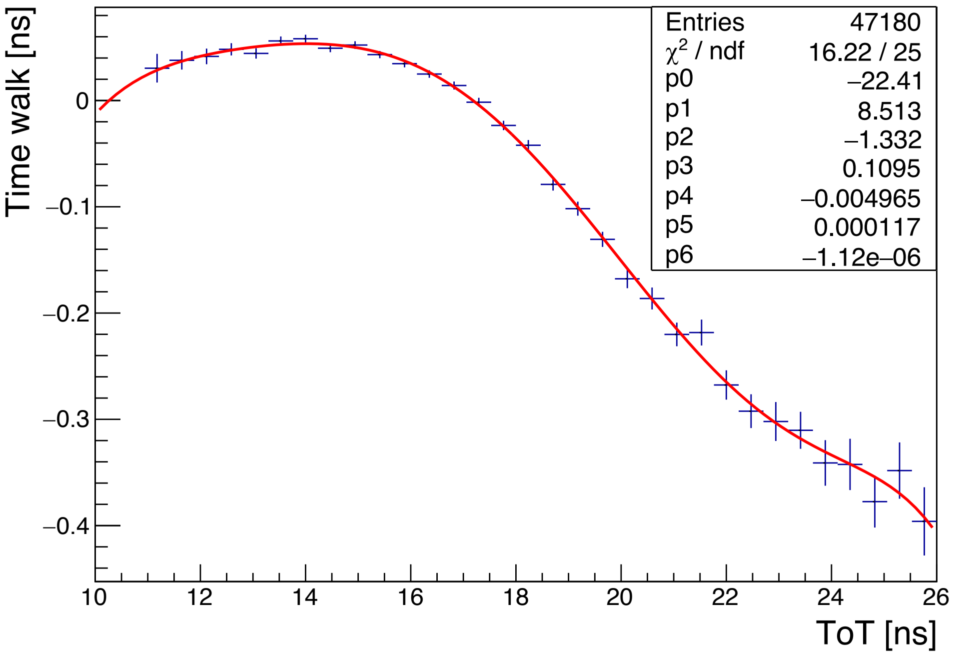




- Amount of charge shown in ToT
- Drop in amount of charge collected around edges of pixel
- Non-uniform electric field near edges
- Sensor not thinned down to 100um and not backside metalised
- Aim for 2-3 V/um to maximise e^- carrier mobility

ToT and time-walk correction





- Tot distribution on left
- Time-walk correction done using a polynomial fit
- Spread of the time-walk and SNR information used to estimate actual pre-amp peaking time <2ns (agree with our cadence simulations)

ToF measurement

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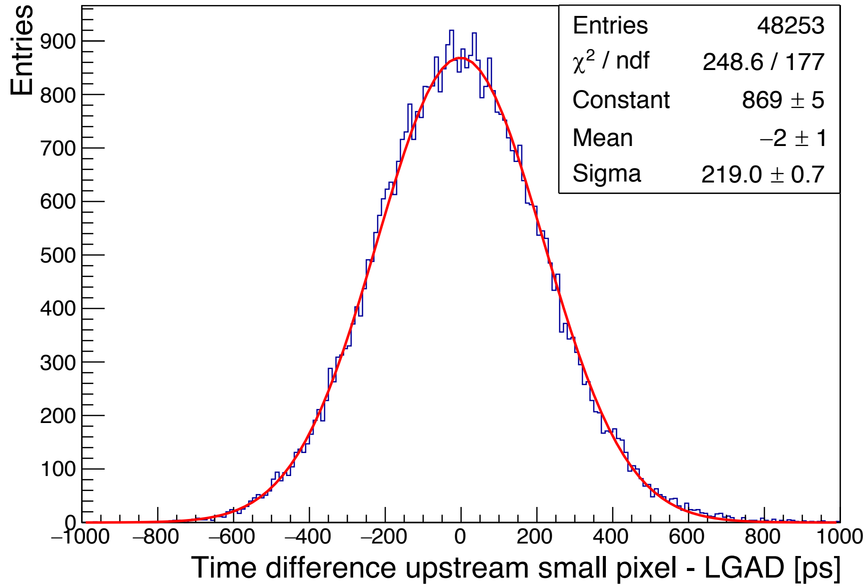
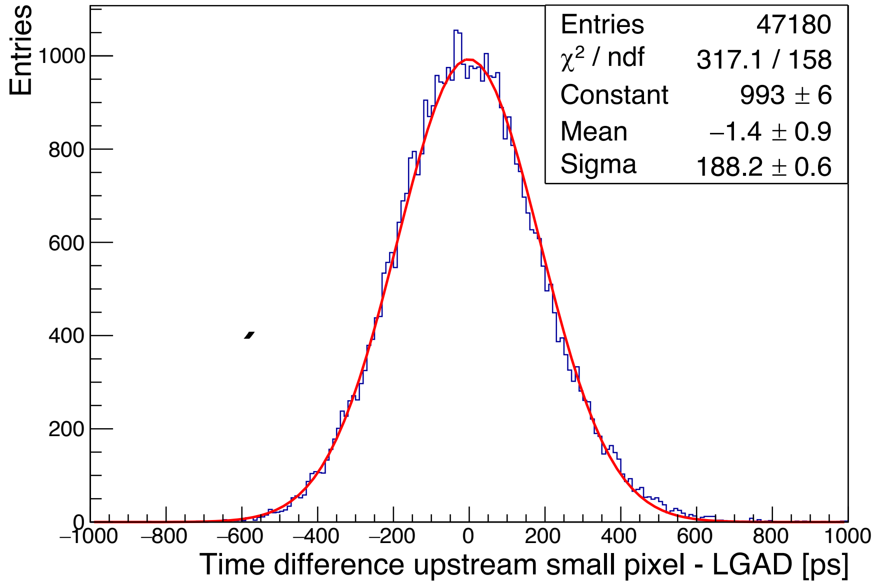
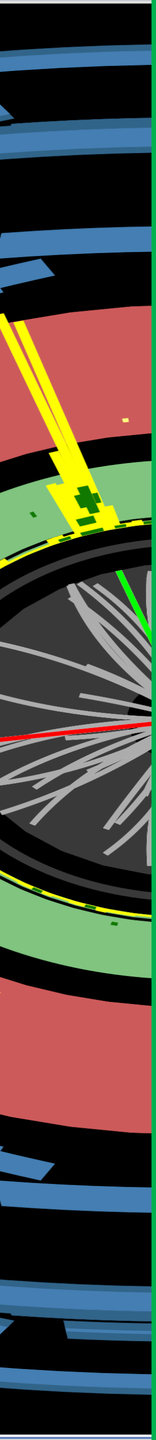




	Time resolution [ps]	
Pixel	w/o position correction	with position correction
Downstream Small	202.3 ± 0.8	167.7 ± 0.7
Upstream Small	219.0 ± 0.7	188.2 ± 0.6
Upstream Large	265 ± 1	212 ± 1

Despite lack of vital processing steps ToF no so far away from 100ps for MIP's expected



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Simple phantom simulation

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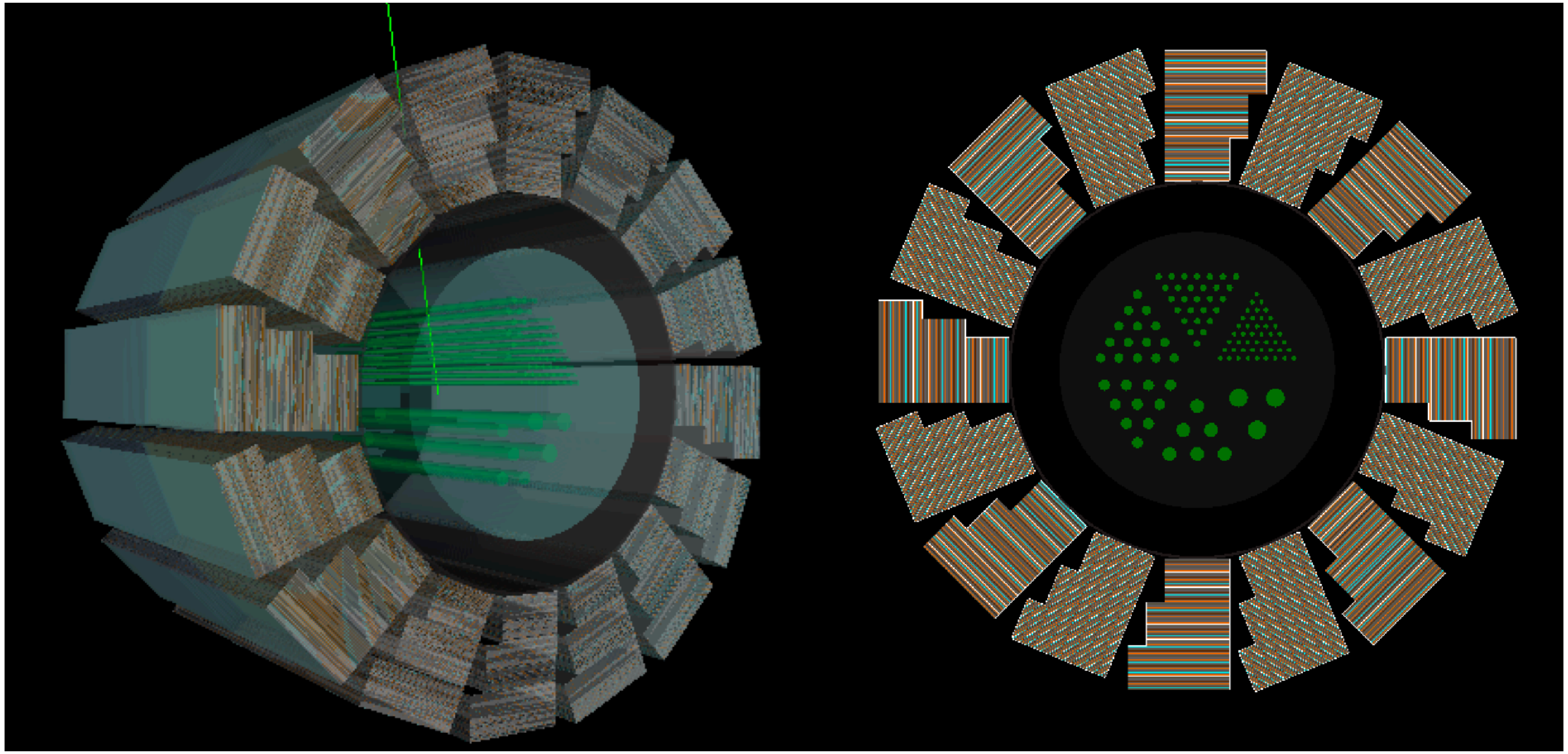
- Geant4 simulation
- Scanner geometry with acrylic phantom (variable rod sizes) filled with F18 (50MBq)



Phantom D = 15mm

Rod d = 0.5mm
0.7mm
1.0mm
1.2mm
1.5mm
2.0mm

Inter-rod distance 2d

Simple phantom simulation

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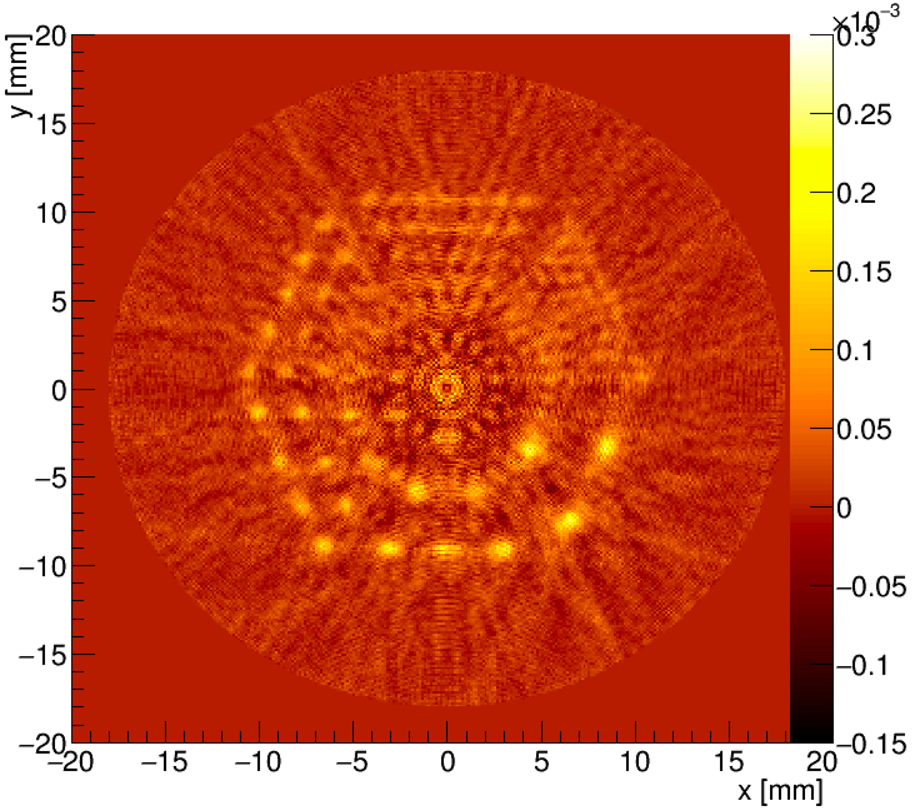
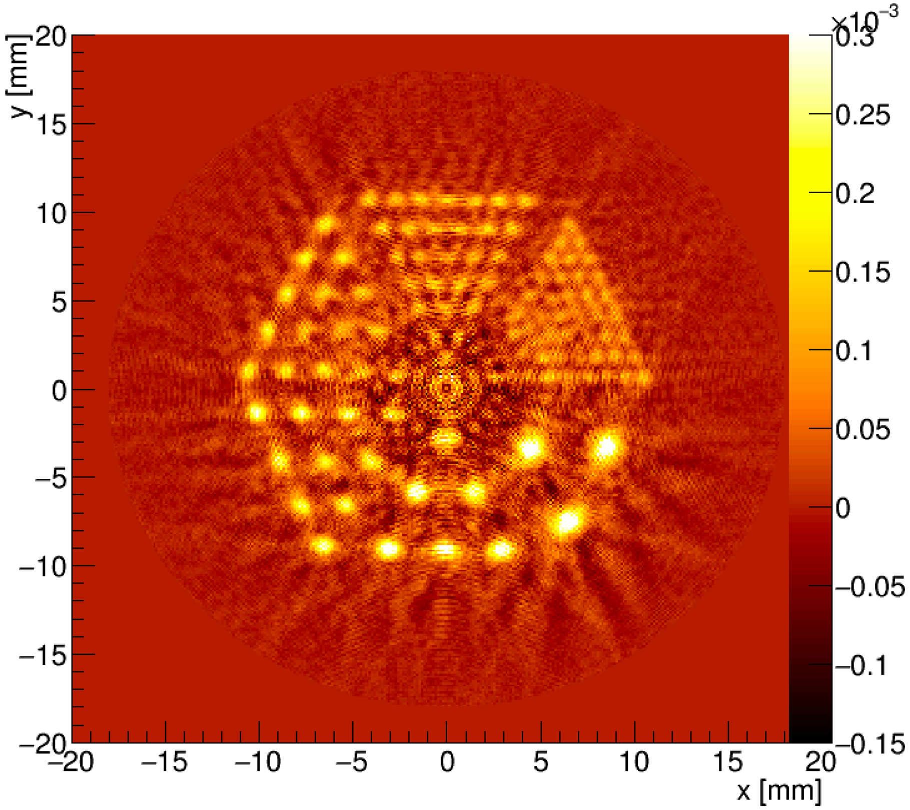
- Simple reconstruction (FBP)
- $>10^9$ events simulated
- Expected detector response included

no – TOF information



TOF information



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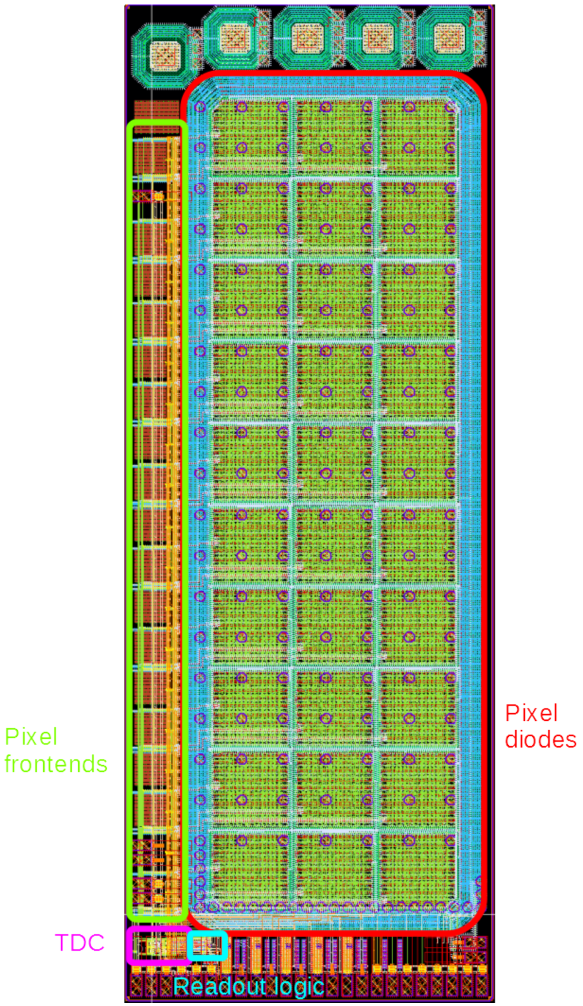
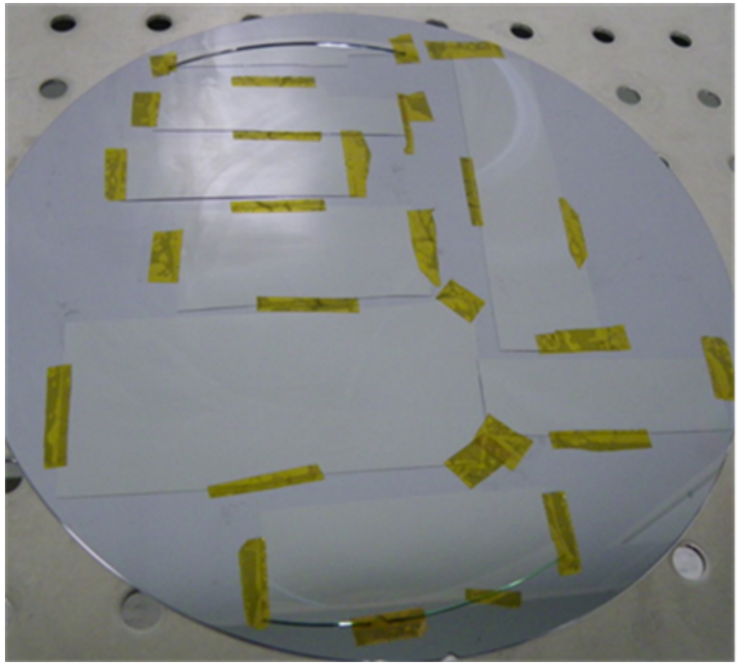
Prototype-0

- A fully featured prototype was submitted in April 2017 (MPW run)
- It has a smaller matrix (30 pixels) and a simplified readout scheme, but it's otherwise complete
- Low resistivity wafer first (check HV doesn't interfere with LV electronics
- It's useful to test integration issues (power delivery, crosstalk…)



Prototype-0 HR

- Delays in high resistivity delivery
- Thin wafers broke at backside metaisation and dicing stage
- 4 MPW runs per year, ~4 month process time
- HR backside metalised diced chips delivered last week
- HV tested to work upto target 300V



Test setups

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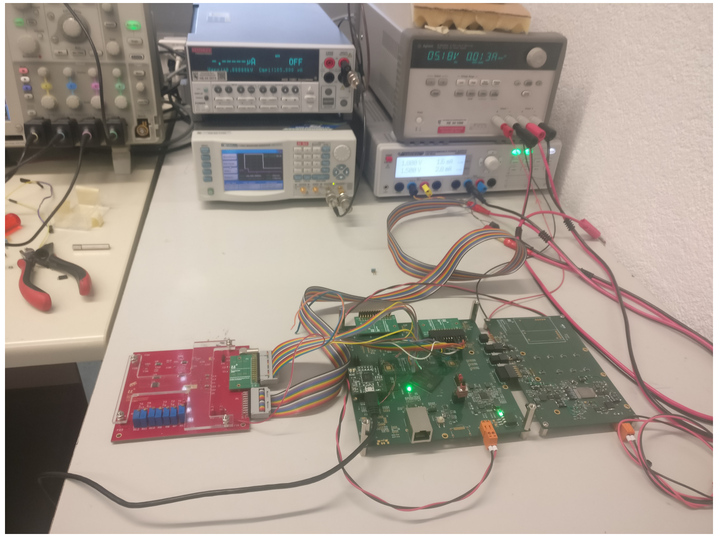

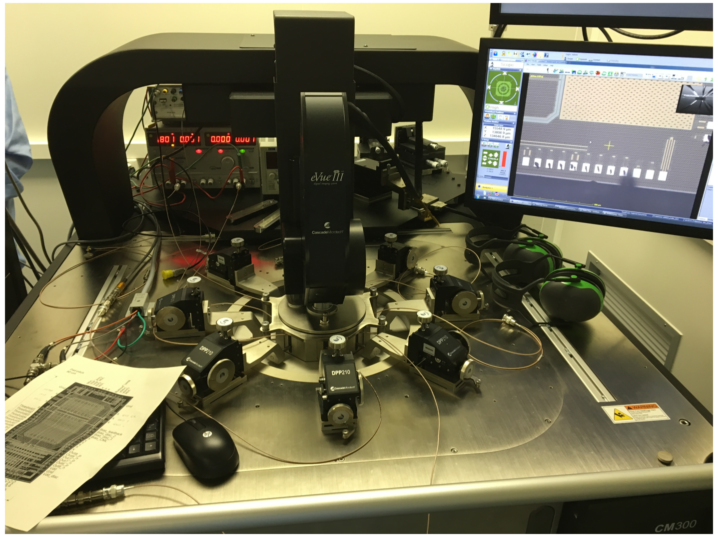

- DAQ software and firmware has already been developed
- Continued to to be improved
- Additional power module for the each Tower control FPGA board has been completed
- Top left: Prototype-0 (red PCB) being tested at Bern

- Probe station used to characterize monolithic chips before being mounted on PCB's for testing (R&D)

Future Tests

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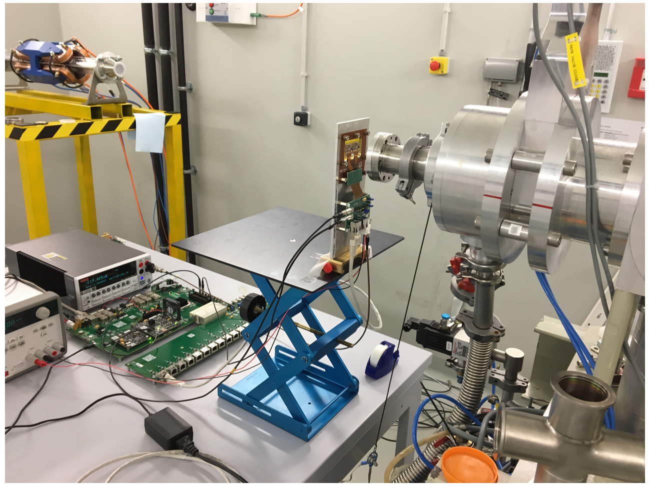
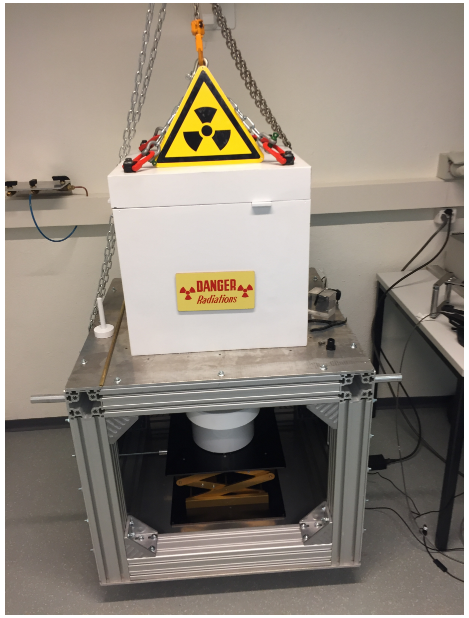
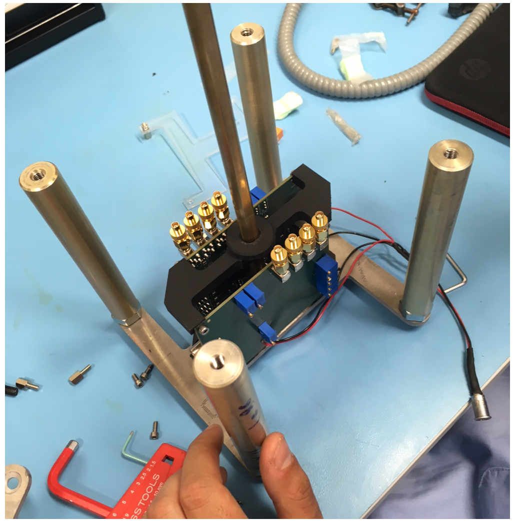
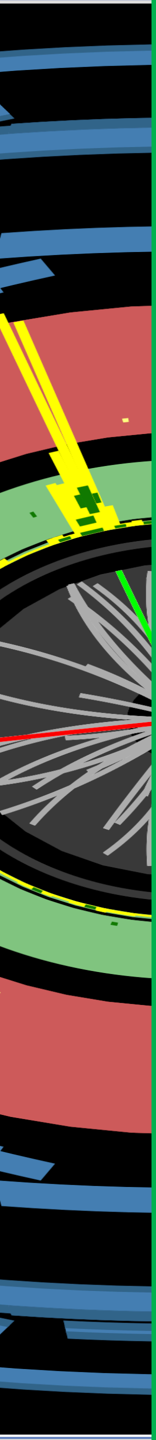


- Now that Prototype-0 HR has been delivered
- ToF / coincidence measurements will be performed in the coming weeks at Bern cyclotron using custom F18 phantom's
- ToF measurements using cyclotron 18 MeV proton beam
- CFRP support + protective skin going through final revisions





- Na22 ToF at Geneva University shortly
- Final monolithic design submission expected Sept/October 2018



Thank You

Questions?

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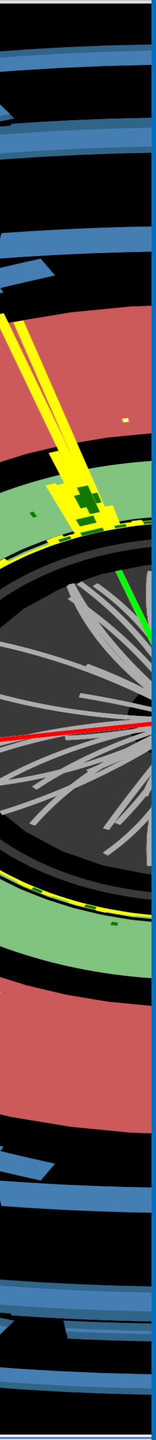
dforshaw@cern.ch



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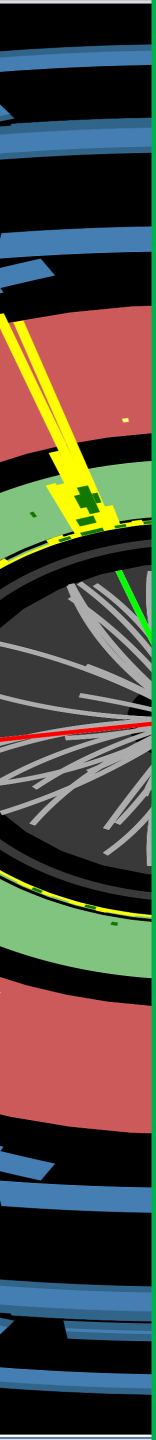
Backup



Why use Time-of-Flight?

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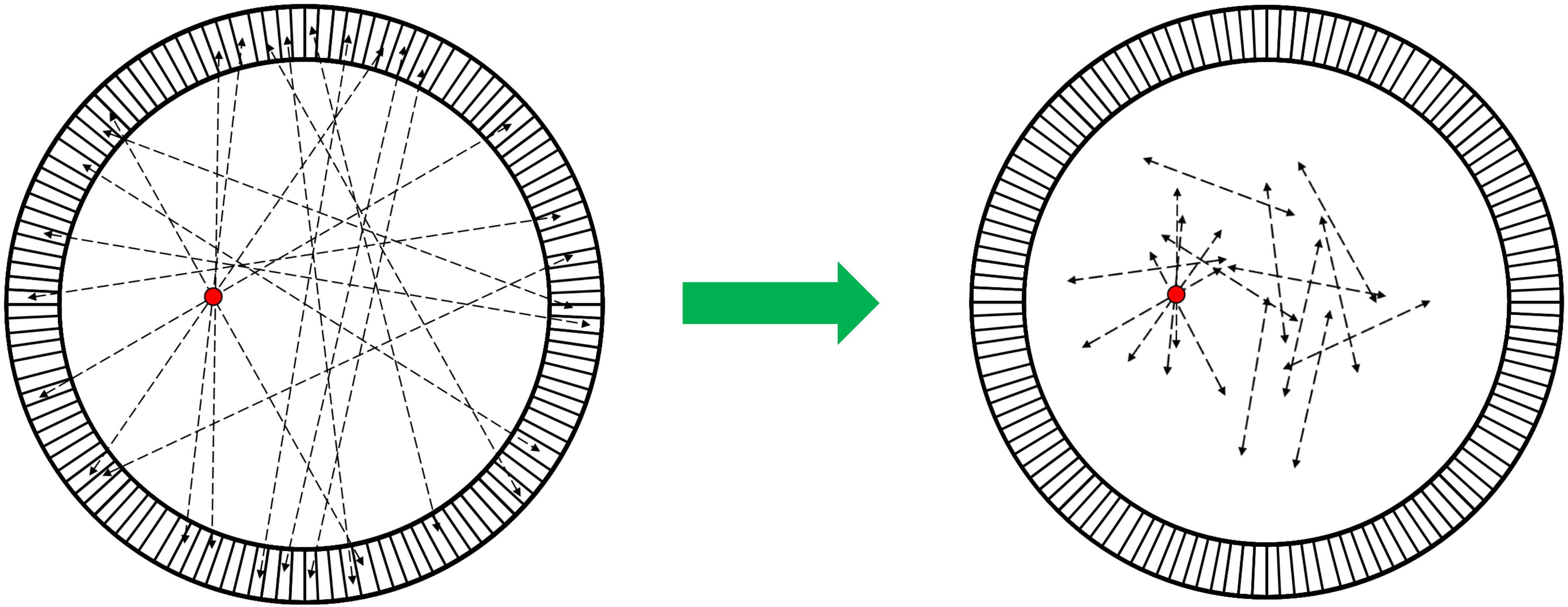
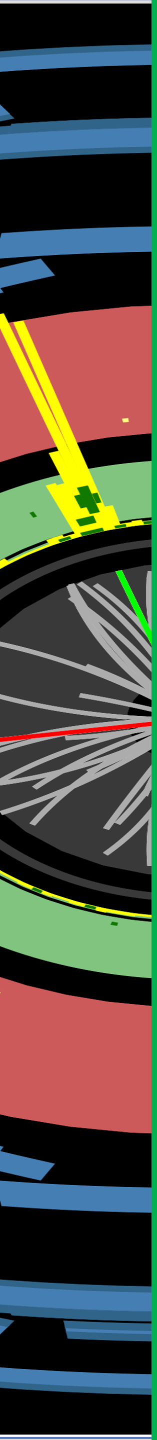
Conventional PET

TOF PET





Time resolution

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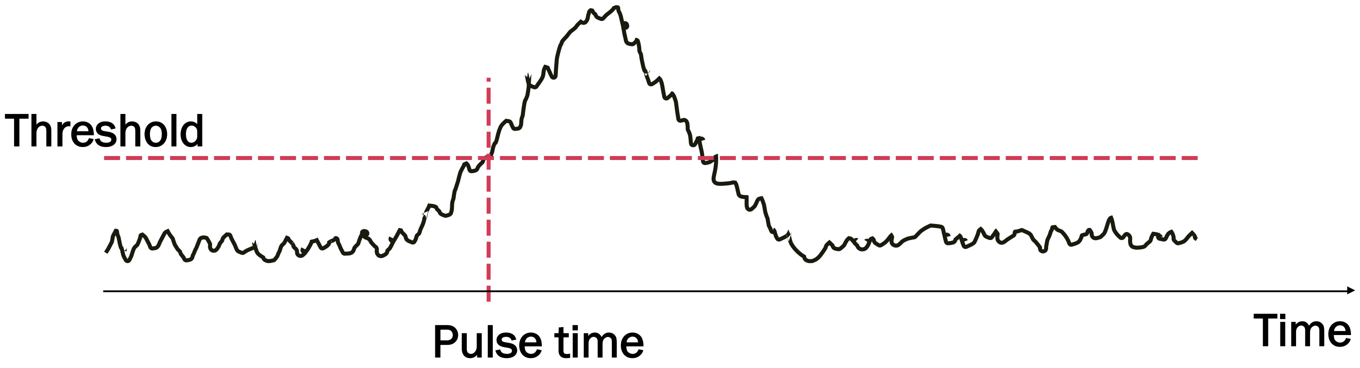
- Detector time resolution depends mostly on the amplifier performance.

$$\sigma_t = \frac{\sigma_V}{\frac{dV}{dt}} \cong \frac{t_{rise}}{Signal/_{Noise}}$$



Time-over-Threshold

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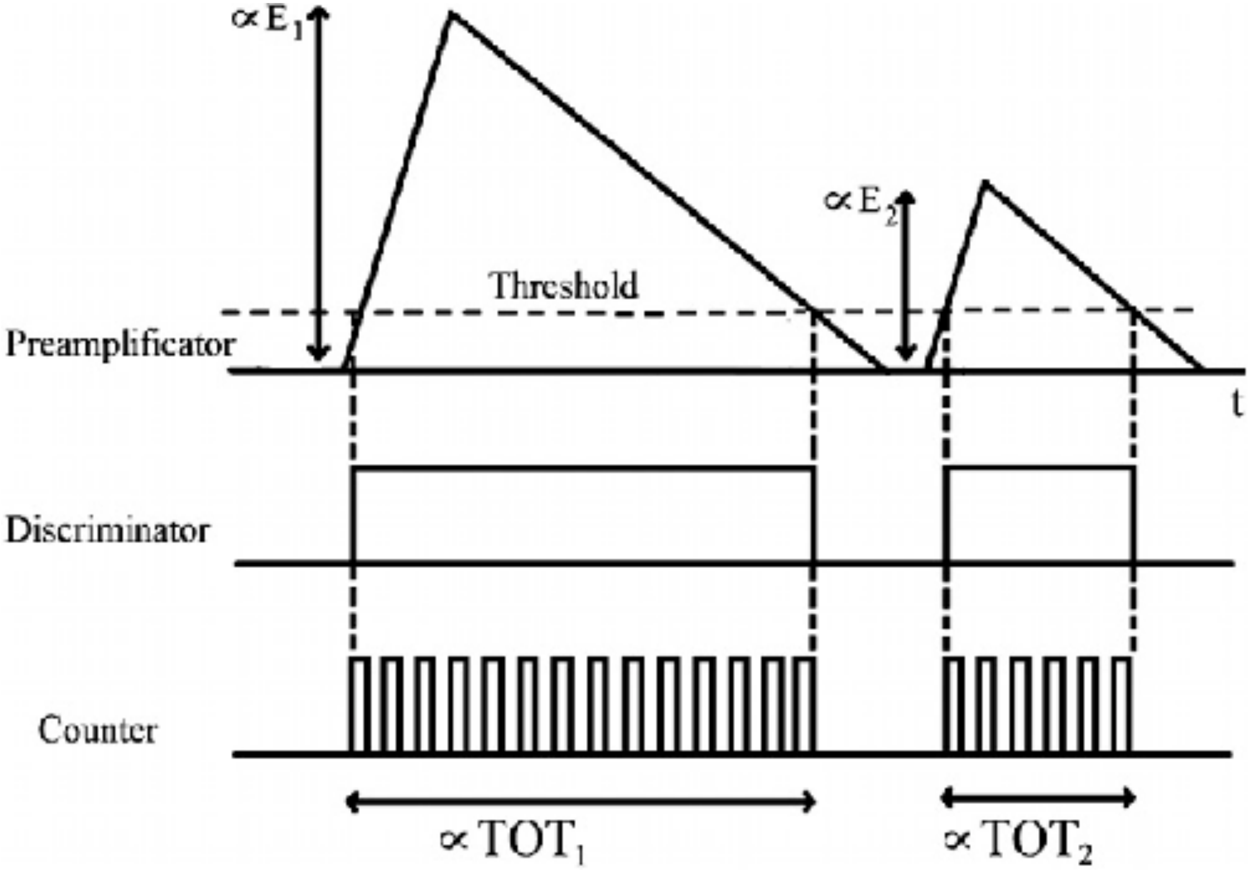

Event Rate and Data Pressure

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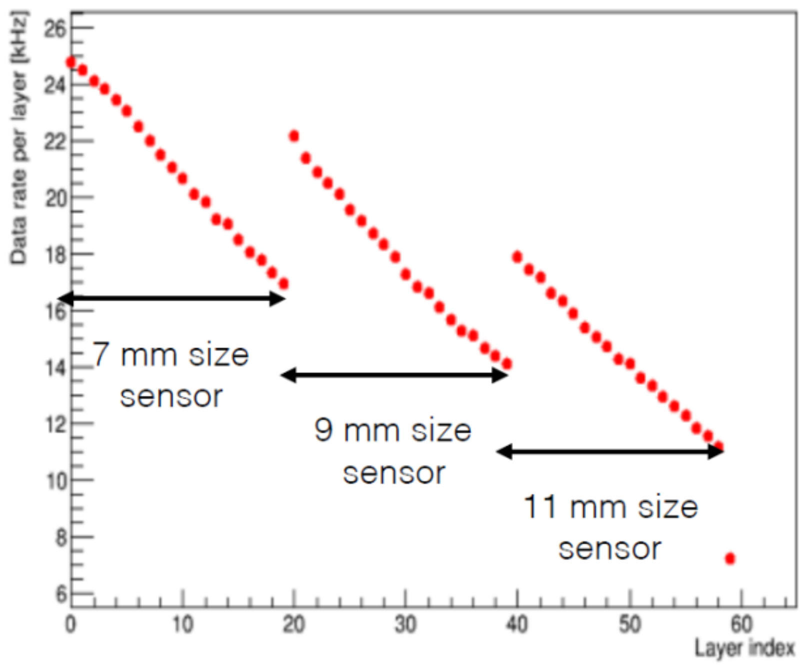
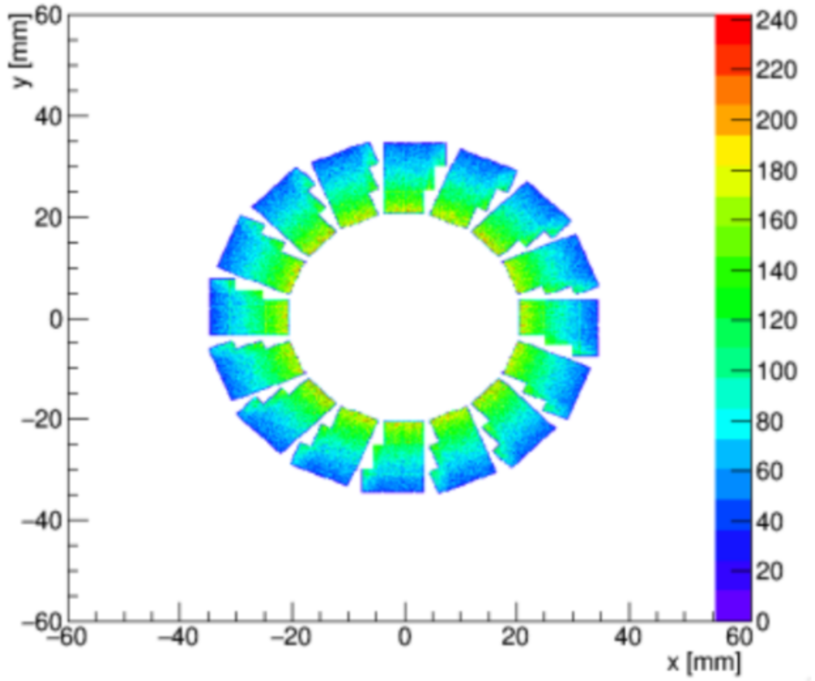
- Hit rate for a 50 MBq point source is still < 25kHz per layer





- Geant4 Simulation

Monolithic Test chip

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