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FERS-5200: a distributed and scalable Front-End Readout System for large detector arrays.

FERS-5200 is a Front-End Readout System designed for the readout of large detector arrays, such as SiPMs, multi-anode PMTs, Silicon Strip detectors, Wire Chambers, GEM, Gas Tubes and others. FERS is a distributed and scalable system, where each unit is a small card that houses 32 or 64 channels with preamplifier, shaper, discriminator, A/D converter, trigger logic, synchronization, local memory and readout interface. FERS is a flexible platform: keeping the same back-end (that is a readout architecture and interface), different types of front-end will be developed to fit a variety of detectors. Typically, the front-end is based on ASIC chips that allow for high density, cost-effective integration of multi-channel readout electronics into small size and low power modules. The first unit being developed is the A5202 that uses the Citiroc-2A chip produced by Weeroc for SiPM readout, but there will be a complete line of FERS units using different Weeroc chips as well as ASIC from other vendors or even preamps made of discrete components. Depending on the used Front End ASIC, the system may have self-triggering capabilities and provide energy (pulse height or charge) and/or timing information, either independently channel by channel or simultaneously on all channels

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