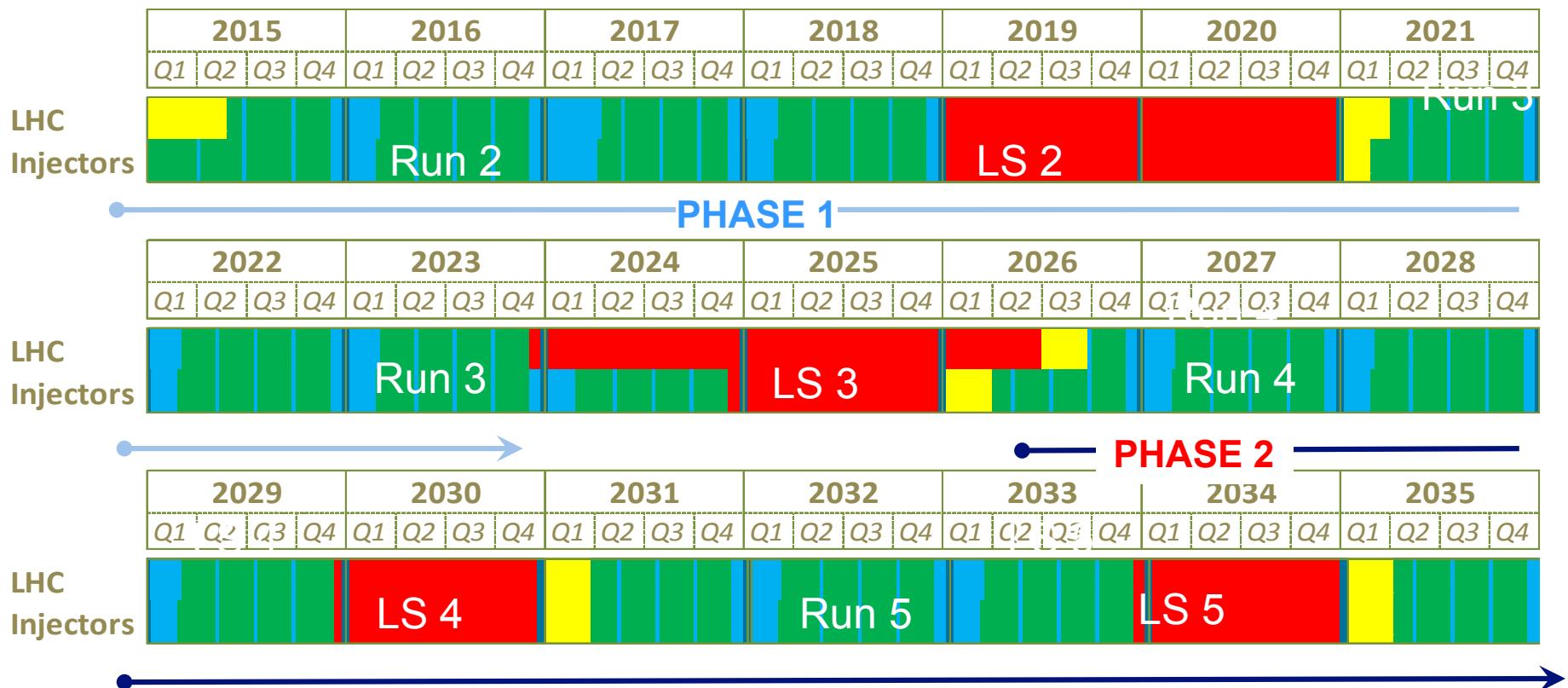


CMS

Consiglio di Sezione INFN – 30/06/2017

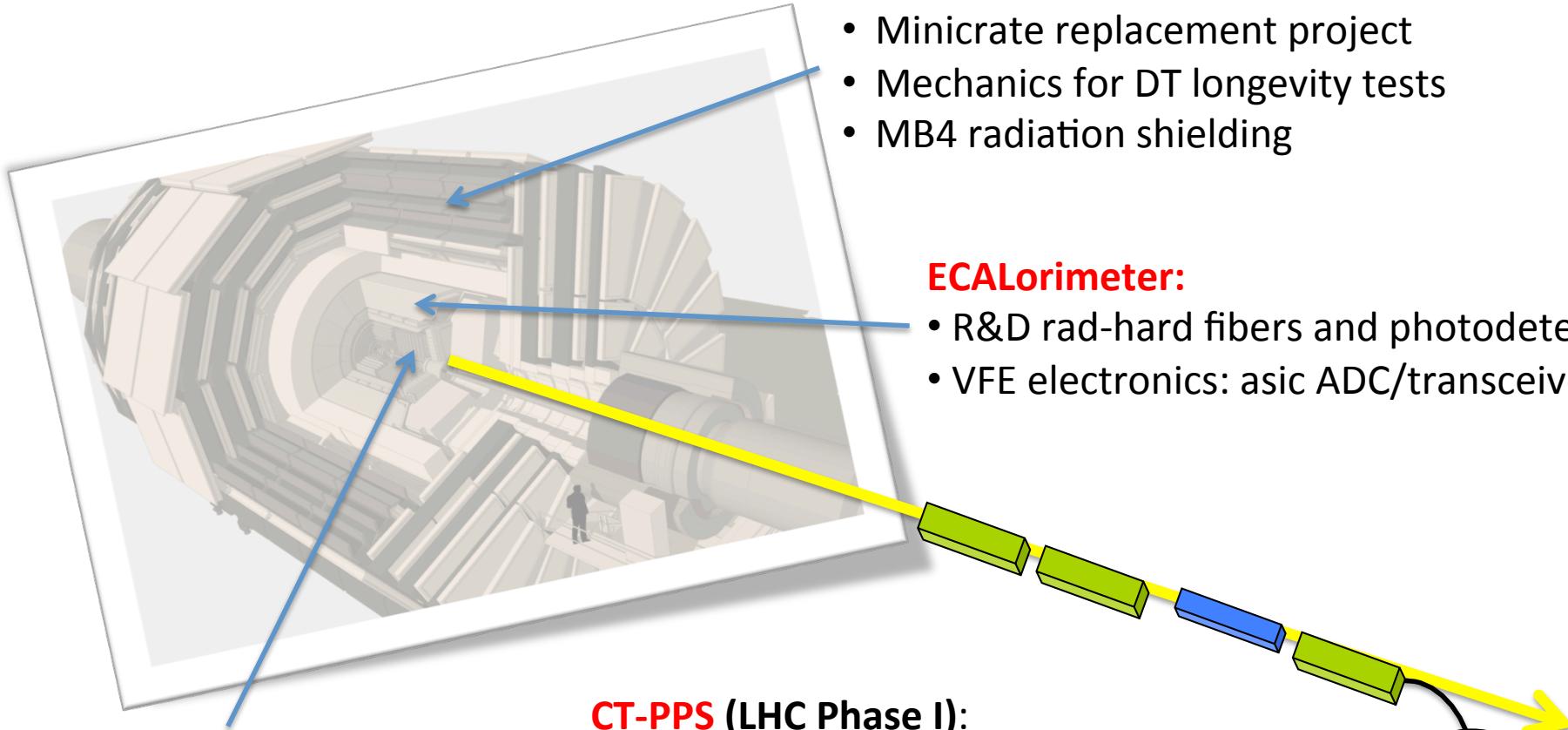
LHC roadmap to HL-LHC (Phase 2)

- High Luminosity $5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$
- High pile-up (average is 140 interactions per bunch crossing, could be higher)





Detector activities in Torino towards HL-LHC

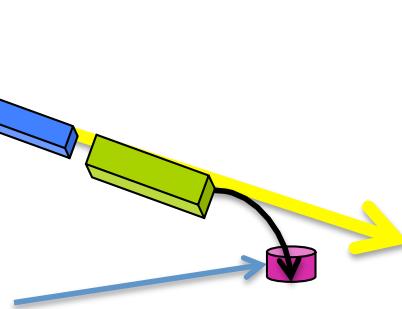


Tracker:

- R&D new ROC 65nm
- R&D 3D pixel sensors

CT-PPS (LHC Phase I):

- Both side of CMS experiment (~220 m from IP)
- 3D modules for the tracking stations
- UFSDs for the timing stations





DT for HL-LHC

Torino activities



R&D Phase 2 program:

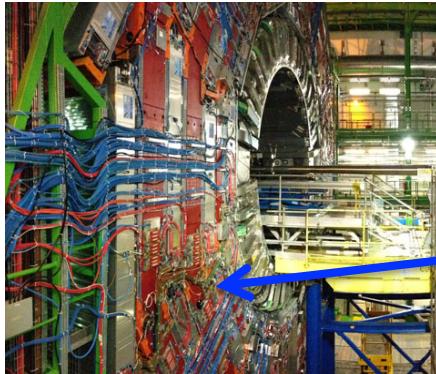
- Design and realization mechanics for DT Longevity tests
- New Minicrates: R&D optical links for new electronics L1 on chambers

Design and realization by Lab
Tecnologico (Dattola + 1 Tecnico)

Design and realization by Lab
Elettronica (De Remigis, Rotondo)



Barrel Muon Drift Tubes Electronics Phase2 LHC Upgrade



- Replace on chamber electronics (Minicrate)
- Move trigger and readout complexity to USC (outside of radiation environment)

Original Minicrates

17 different boards:
Some of them not radiation tolerant for HL-LHC
Limitation in readout bandwidth

Readout

Time digitization
Event matching

Trigger

segment finding, angle measurement=>
single chamber trigger generation

New Minicrates (Phase2)

1 type of board (OBDT):
Based on FPGA radiation tolerant for HL-LHC
Readout bandwidth 1 MHz L1

Readout

Time digitization

Digital information sent through optical link to the counting room (GBT Links)

Complexity is brought into the counting room.

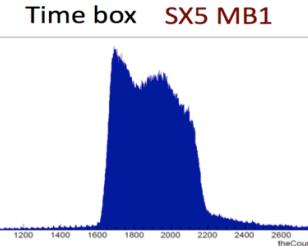
De Remigis
Rotondo

Barrel Muon Drift Tubes Electronics Demonstrator - Current Activity

DT L1 and Readout
System specification
defined with
demonstrator



Sizing of the
upgraded
architecture
components, which
bring the whole raw
TDC data through
optical links from
front-end to remote
electronics.



– 2x 10Gbps links to TwinMux

10x LVDS cables from Front End
(160 channels)

2x Virtex 7 Evaluation Boards
(276 TDCs)

4x Input FMC mezzanines

1x VLDB (GBT) for clock
distribution

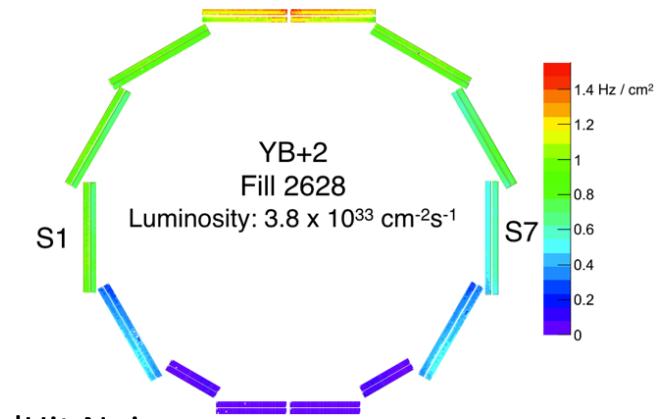
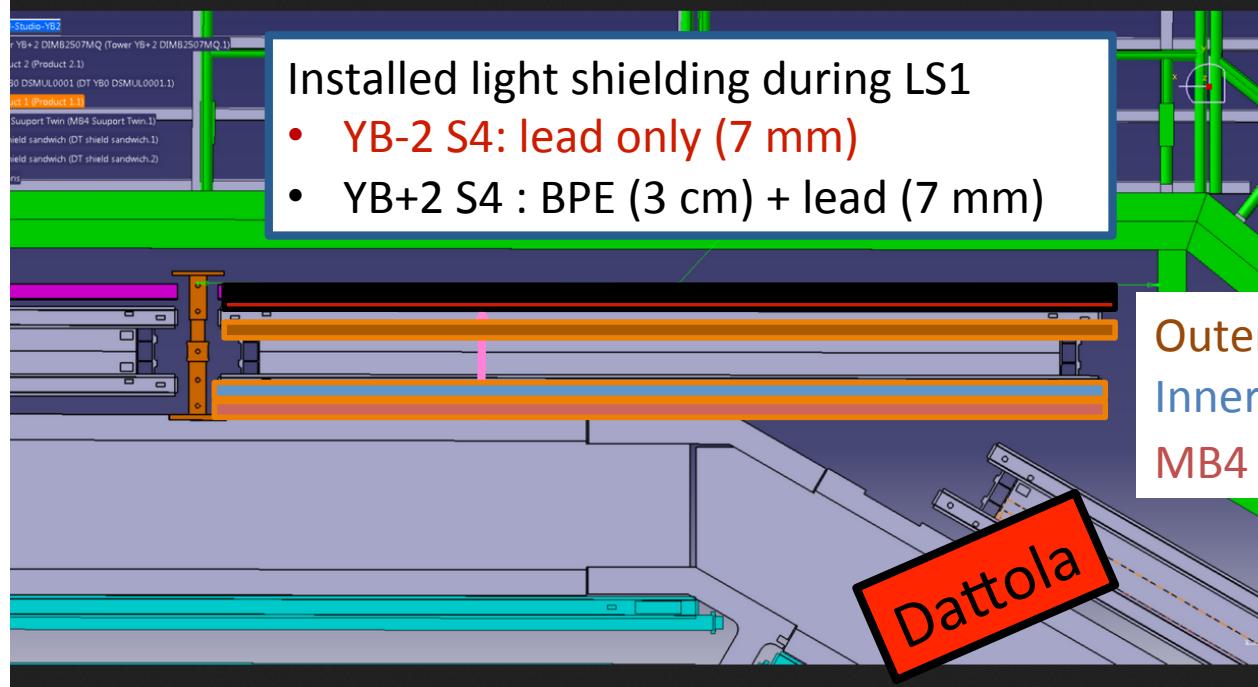
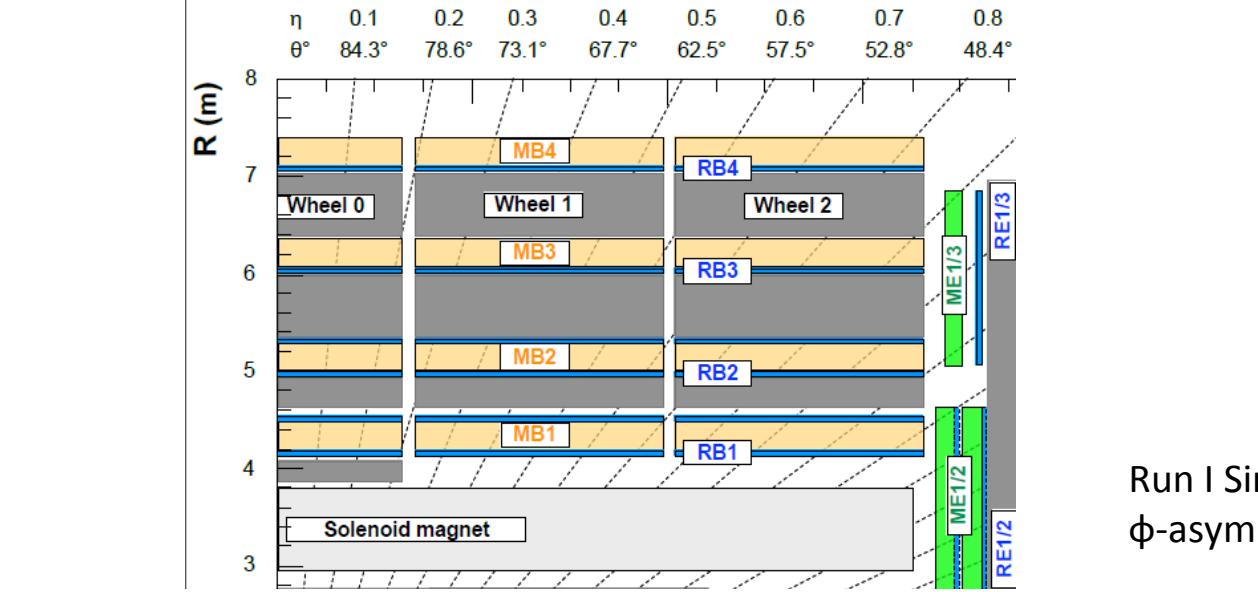
2x Slow Control (Ipbus)



De Remigis
Rotondo



DT Chambers Neutron Shielding



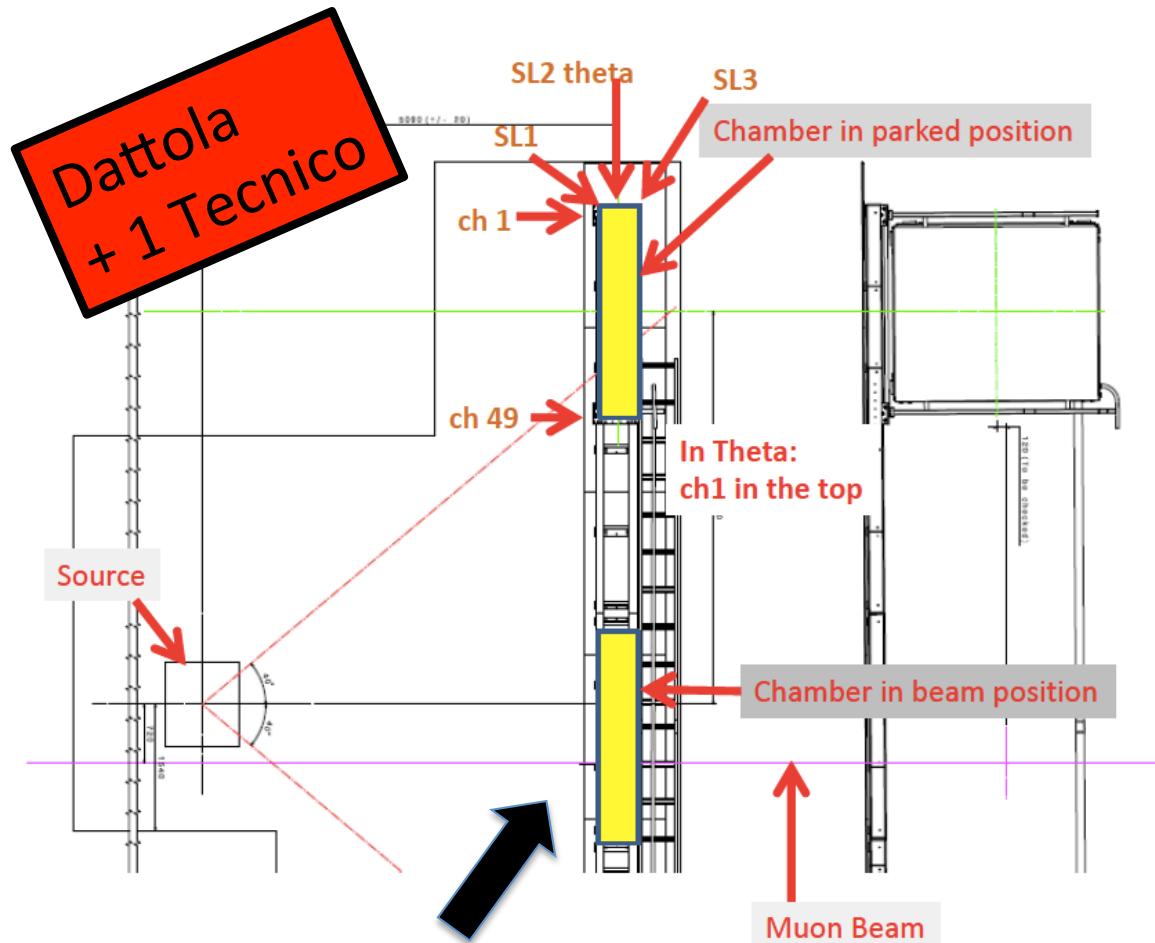
Run I SingleHit Noise:
 ϕ -asymmetry from wheel feet & cavern walls





Barrel Muon Drift Tubes

Longevity studies at GIF++ at CERN



MB1 chamber under test
mounted on a rail at GIF++



DT tubes test of pollutants
generation under radiation



DT Milestones for NEW MiniCrate



2016	2017	2018
dimostrare il multichannel TDC su FPGA e la portabilità degli algoritmi di trigger in asincrono	qualificare la nuova architettura su di una camera intera	validare il track finding strumentando un intero settore (4 camere)

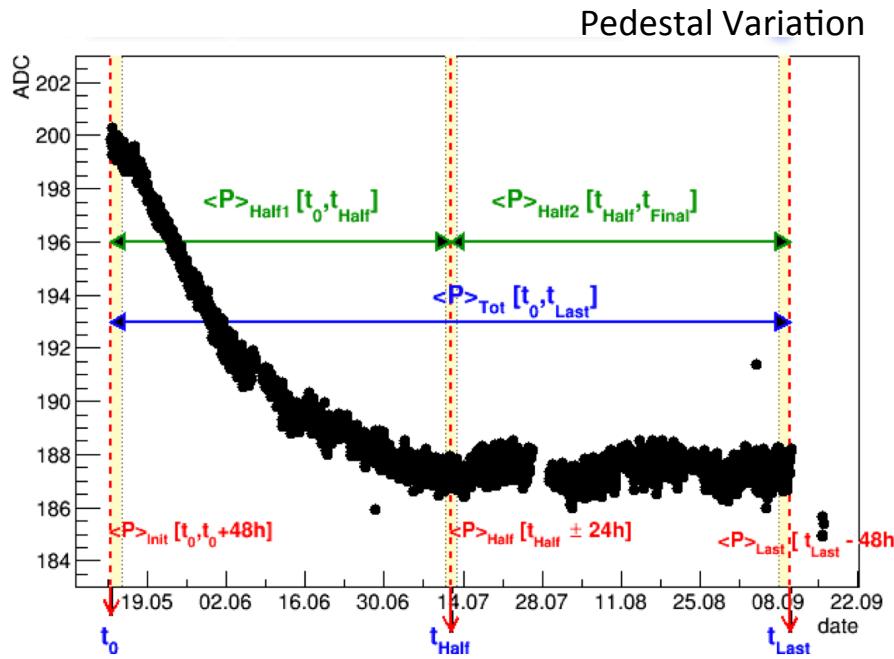
Impegno di Torino

Richieste CMS-DT 2018

Dattola	11 m	Infrastruttura per Studi di Longevita' dei DT alla GIF++/ Schermo protezione per MB4 (DT)
Tecnico Lab. Tecnol.	3 m	Infrastruttura per Studi di Longevita' dei DT alla GIF++
De Remigis	40%	Progetto DT New Minicrate
Rotondo	7 m	Progetto DT New Minicrate

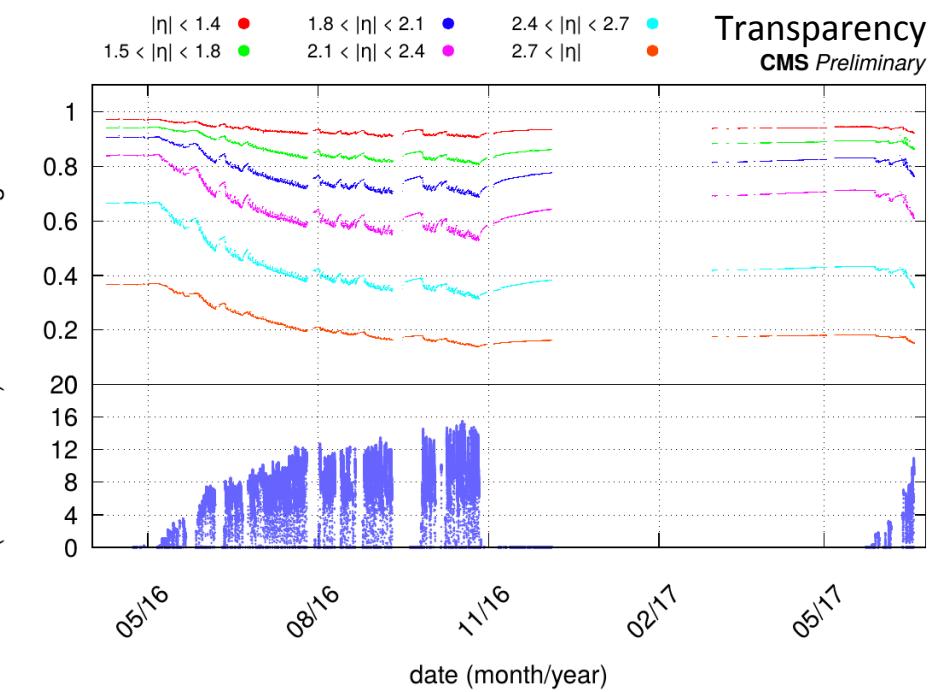
ECAL Past and Present

- In the 2017 data taking the detector is behaving as expected
- Important involvement of italian (To, Mi, Rm) groups to construction, operation, reconstruction, calibration
- The harsher running conditions (pileup) requires **constant monitoring** and fine-tuning in which the Torino group is much involved



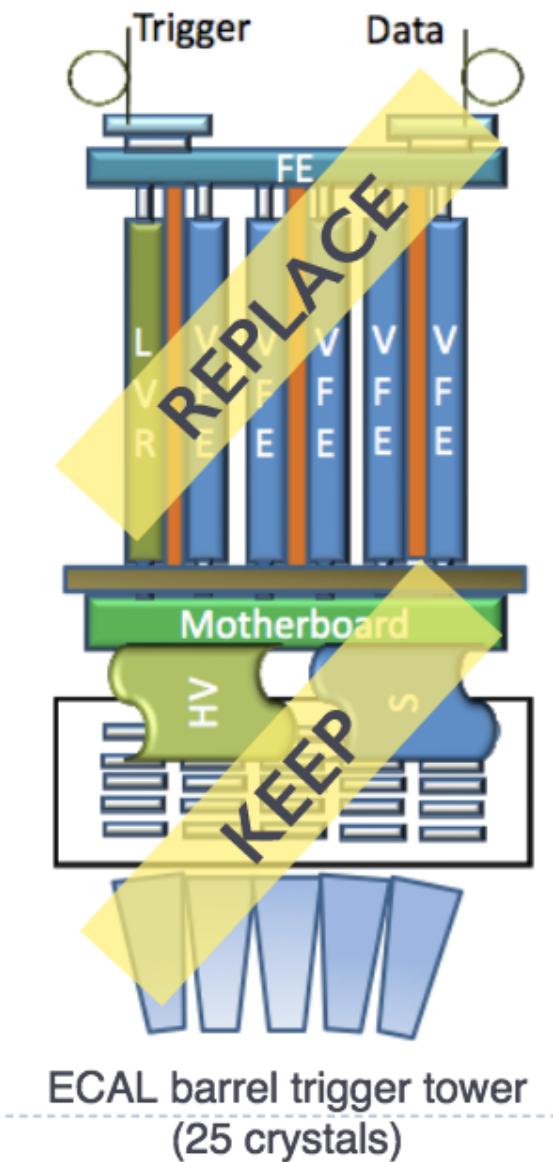
Relative response
to laser light

LHC luminosity
($10^{33} \text{ cm}^{-2} \text{ s}^{-1}$)



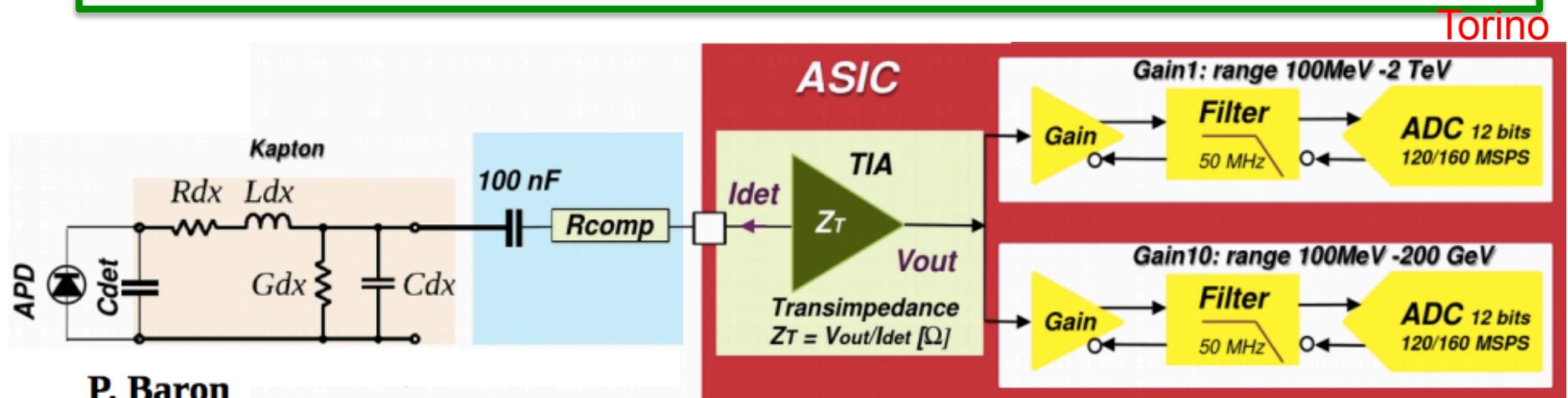
ECAL Future: HL-LHC

- Replace Front-End (FE) and Very-Front-End (VFE) readout
 - To cope with increased Phase II trigger requirements
 - To cope with HL-LHC conditions (APD current noise, pileup, anomalous APD signals).
 - Precise timing measurements for high energy photons.
- Run **colder** to mitigate increase in radiation induced APD dark current
- New off-detector electronics to cope with higher output bandwidth from FE: move trigger off-detector, per-channel granularity



VFE upgrade: Torino contribution

- VFE re-design:
 - Analog readout chip (Saclay/RAL)
 - **ADC and transceiver chip: LiTE-DTU** → **Torino + Lisbon**
 - 160 MHz, 12 bit sampling to allow precise time reconstruction
 - All samples continuously shipped off-detector
 - Lisbon: ADC block, **Torino** : everything else, including executive design, integration, testing of prototypes
 - **Timeline:**
 - First prototype: Q1 2018. Testbed to be developed @TO
 - Second prototype: Q4 2018





CMS-ECAL: Richieste servizi



Elettronica / VLSI

- **6 m.u. microelectronics design**
 - Mazza, Dellacasa, Rolo
- **1 m.u. test-PCB design**
 - Mignone, Rotondo



CT-PPS



2016 set-up:

- Two tracking stations per arm with 10 planes of Totem Si strips
- One timing station per arm with 4 planes of diamond detectors

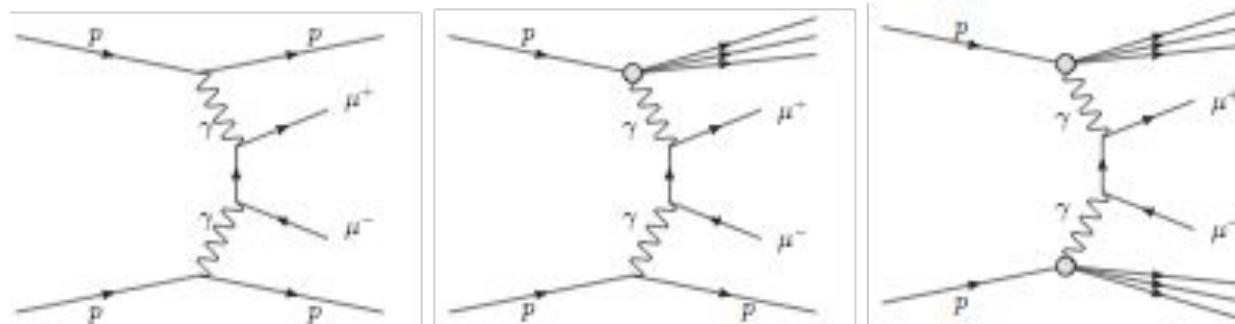
2017 set-up:

- Two tracking stations per arm:
 - 210m pot with 10 planes of Totem Si strips
 - 220m pot with **6 planes of 3D Si pixel sensors with PSI46dig ROCs** (ROC of the new Phase I Pixel Tracker installed during the end-of-the-year shutdown)
- One timing station per arm:
3 planes of diamond detectors and 1 plane of UFSD

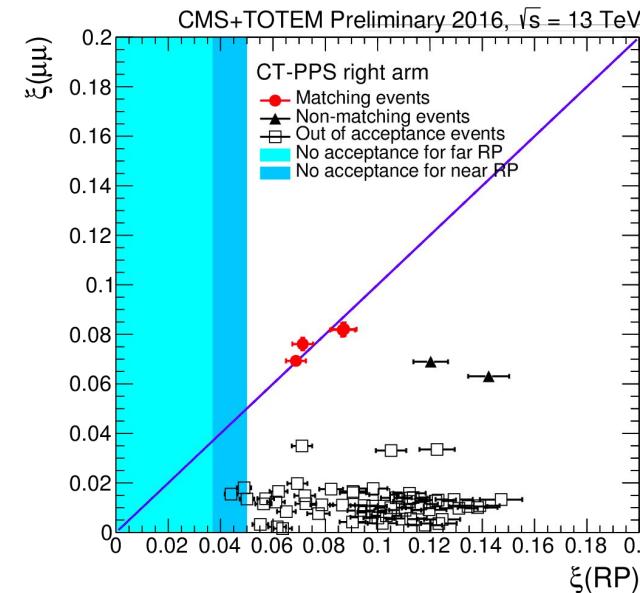
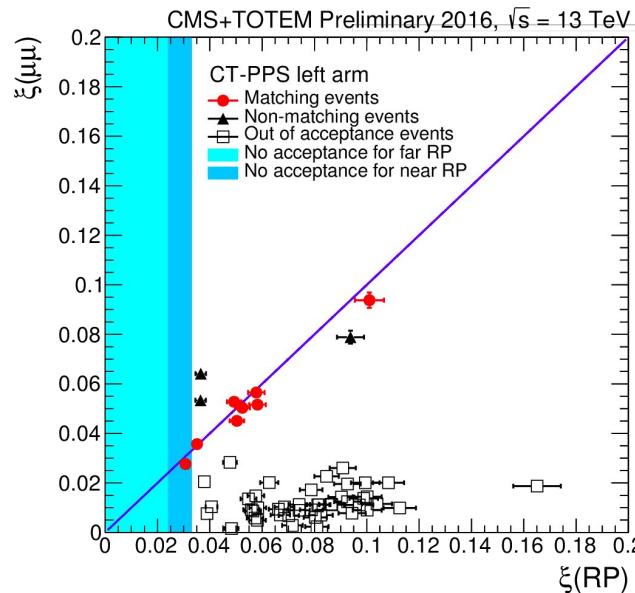
Post-LHCP: First public CT-PPS result

[PPS-17-001](#)

- Evidence for central production of high mass di-muons



- Excellent proof of principle and successful detector operation



$\sim 10 \text{ fb}^{-1}$



CT-PPS: Torino activities in the last year



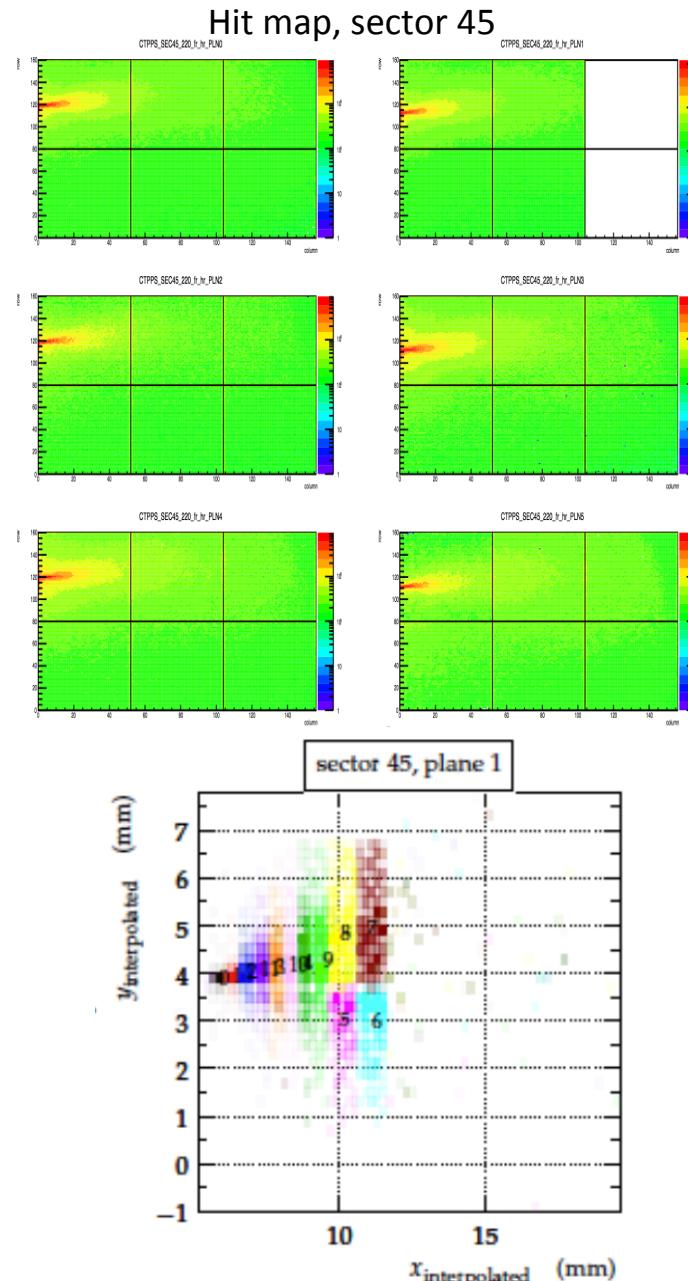
3D pixel tracking detector

- Production of detector modules, assembly, wire-bonding
- Qualification of modules: X-ray test for bump-bonding check, ROC parameters optimization, threshold trimming, calibration
- Beam tests
- Installation and commissioning of two detector stations (6 planes each) in the LHC tunnel

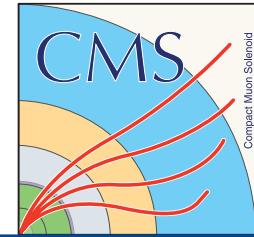
Ultra-Fast Silicon Detector

- Production of sensors at FBK and CNM and their lab characterization
- Design of a custom-made FE electronics for CT-PPS (TOFFEE chip)
- Beam tests
- Installation and commissioning of one UFSD plane in each of the two timing stations

UFSD R&D → ERC of N. Cartiglia



CT-PPS



- The installation and commissioning of the new CT-PPS detectors was successfully achieved. CT-PPS is now using 4 different detector technologies:
 - For tracking: Silicon Strips (from Totem) and new 3D Silicon Pixels
 - For precision timing: scCVD Diamonds and Ultra-Fast Silicon Detectors (first application in a HEP experiment)
- Also, for timing: Two precise clock systems with jitter <1ps (based on RF cables and on optical links) are in operation.
- The detectors are fully integrated in the CMS Central DAQ and run at 100 kHz trigger rate
- The offline software for unpacking of the data of the new detectors (pixels and timing) has been deployed in CMSSW.
- A dedicated run to collect data for RPs alignment and beam optics calibration was done in May. Two crossing angles were tested (150 and 120 urad). The next alignment run (after TS1) should cover the intermediate crossing angles.
- In the low pileup fill in the beginning of June CT-PPS took preliminary data for the timing calibration (protons time vs z-vertex). This calibration aims at using events with two protons in CT-PPS and jets measured in the central detector



CT-PPS



2016 set-up:

- Two tracking stations per arm with 10 planes of Totem Si strips
- One timing station per arm with 4 planes of diamond detectors

2017 set-up:

- Two tracking stations per arm:
 - 210m pot with 10 planes of Totem Si strips
 - 220m pot with **6 planes of 3D Si pixel sensors with PSI46dig ROCs** (ROC of the new Phase I Pixel Tracker installed during the end-of-the-year shutdown)
- One timing station per arm:
3 planes of diamond detectors and **1 plane of UFSD**

Expected actions for 2018:

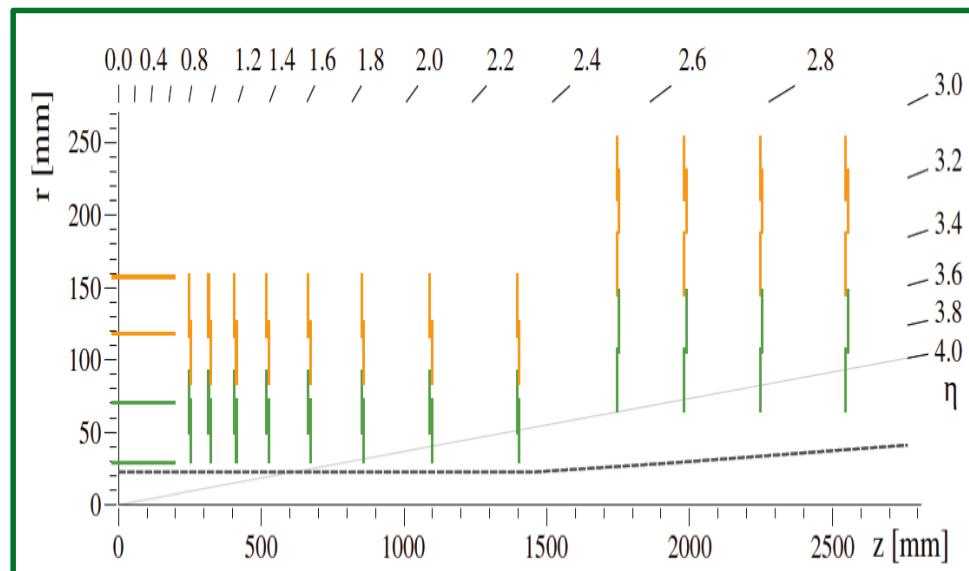
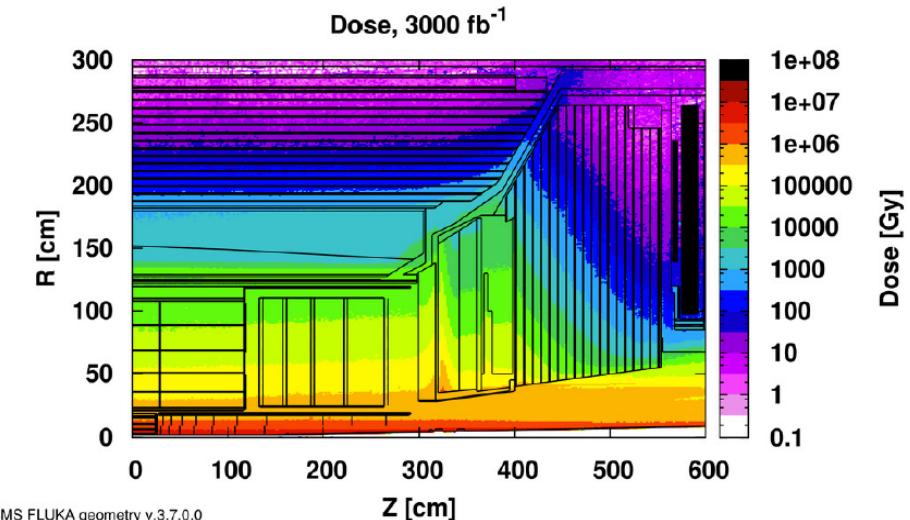
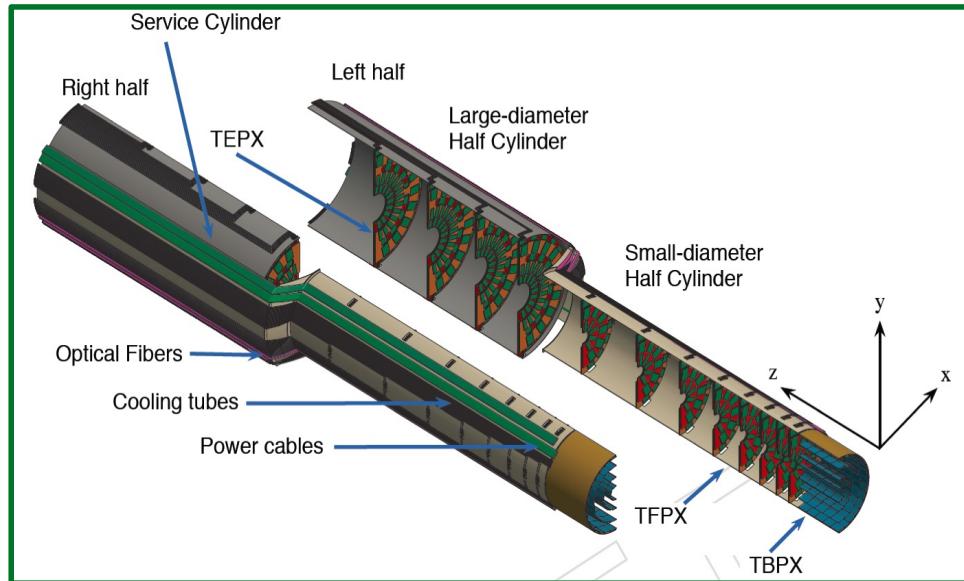
- Replace Si strips with pixels (modules available and ready for TS2 2017)
- Be ready to replace 3D modules when necessary (because of the non uniformity of the radiation damage of the PSI46dig ROC)
→ would like to have 4 extra packages of six planes ready.

Richieste servizi per CT-PPS (insieme a TK):

- Wire-bonding
- Supporto laboratorio elettronico per set-up di laboratorio



CMS Pixel Detector for Phase-2



The most demanding layers are the inner ones, at ~ 3 and 7 cm:

- particle flux
- radiation dose

To maintain same pixel occupancy, a higher granularity is required (x5):

Pixel size NOW is : $100 \times 150 \mu\text{m}^2$

Same occupancy at HL-LHC with $50 \times 50 \mu\text{m}^2$

Torino involvements in Phase-2 Pixel TK

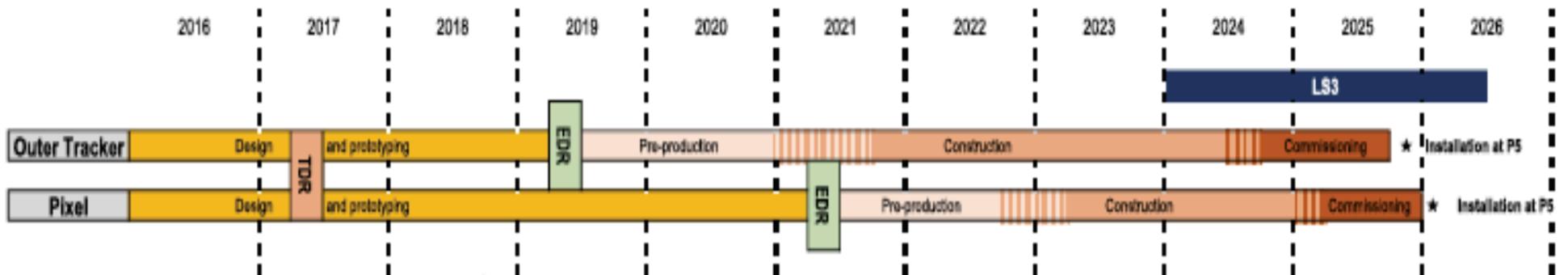
Main research and development activities:

- CMS-Pixel ROC development
- Characterisation of RD53a/CHIPIX65-version2 naked and with sensors (planar/3D). Test beam foreseen.
- Design of Pixel Barrel Mechanics
- R&D on 3D pixel sensors

Construction responsibilities:

Advanced exercise in TDR (presentation to LHCC in September).

- Pixel Readout Chip qualification centre.
- Construction of Barrel mechanics (with Pisa)
- Integration centre of Pixel Barrel layers (TBPIX)





Pixel ROC / Sensor R&D: prototype modules



- **R&D work on Pixel ROC and sensors will be a common effort in 2017**
 - CHIPIX65-demonstrator (version FE0 and FE1), RD53a will be bump-bonded to 3D-sensors and planar sensors
 - Already now first samples of CHIPIX65 arriving after bump-bonding at SLAC with 3D sensors of FBK
 - Experience with CT-PPS 3D sensors is important too
- It is a key-activity to get results in order to help in the final decisions for the CMS-ROC and the sensor choice
 - Irradiation of RD53a / CHIPIX65 wo/with sensors
 - Characterisation in laboratory
 - Test-beams

Test DAQ and pcb/lab setup:	Wheadon; Rotondo/Zampieri
Wire-bonding:	Dumitrache/Pini



ROC development



- Time schedule : **submission of CMS-ROC in Q1-Q2 2019**
 - 1 year to move from prototype to final chip.
- Contributions to RD53a on CMS-side are mainly by Chipix65 groups and by CERN (1-2 fellows + J.Christiansen). INFN groups willing to continue into the design of the final Pixel ROC : **Torino, Bari, Pisa, Bergamo/Pavia**.
- Leading contribution from Torino in Chipix65 and RD53. This needs to be continued for CMS Pixel-ROC
 - vital contribution to RD53a characterisation
 - more than vital contribution to the design of the Pixel ROC.
Analog design and digital Pixel Matrix architecture very promising

- **Design TEAM for Torino**
 - L.Pacher, E.Monteil (tbc) AdR
 - A.Paterno PhD - Politecnico
 - A.Rivetti, M.Rolo, G.Mazza, G.Dellacasa.

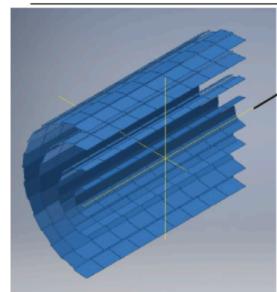


Design of TBPX mechanics



- Joined effort of Pisa and Torino
- Few studies started for TDR, much more work needed in 2018
- A few characteristics:
 - 4 layers
 - CO₂ cooling at -40C

P.Mereu, S.Coli +
Request of 1 year Borsa Tecnologica

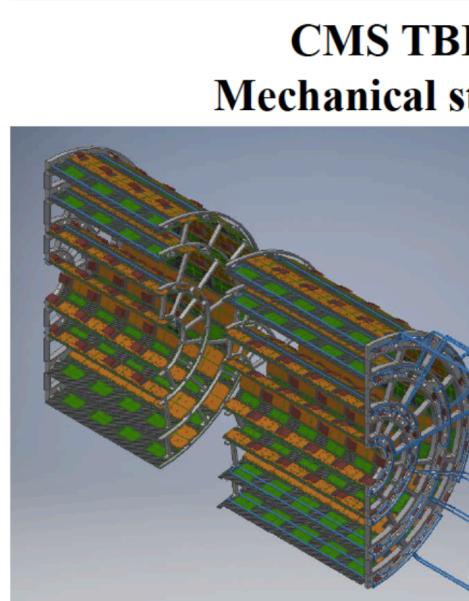


CMS TBPX phase_2

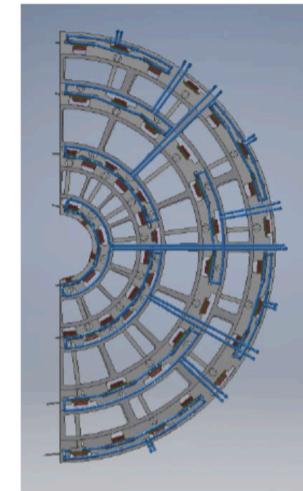
Sensor Geometry:



	R in [mm]	R out [mm]	Z+ / Z- [mm]	N. rod int.	N. rod ext.	N. mod along Z	N. Mod. Tot.
Layer_1	27,5	30,5	+199,7/-199,7	6	6	9	108
Layer_2	68,646	71,646	+199,7/-199,7	14	14	9	252
Layer_3	116,253	119,253	+199,7/-199,7	12	12	9	216
Layer_4	155,888	158,888	+199,7/-199,7	16	16	9	288
							360+504



CMS TBPX phase_2
Mechanical structure vers.0:





CMS TK + PSS overall requests



- Meccanica Barrel Pixel :
 - S.Coli 20%, P.Mereu 20%
 - Borsa tecnologica - 1 anno (2018)
- Progettazione ROC:
 - G.Mazza (20%), A.Rivetti (10%), M.Rolo (10%), G.Dellacasa (7m)
- Pcb / setup di laboratorio:
 - F.Rotondo (2m); A.Zampieri (1m)
- Wire-bonding:
 - F.Dumitrache / B.Pini (2m)
- Test-DAQ:
 - R.Wheadon (20%)



CMS DT + ECAL



DT

Dattola	11 m	Infrastruttura per Studi di Longevita' dei DT alla GIF++/ Schermo protezione per MB4 (DT)
Tecnico Lab. Tecnol.	3 m	Infrastruttura per Studi di Longevita' dei DT alla GIF++
De Remigis	40%	Progetto DT New Minicrate
Rotondo	7 m	Progetto DT New Minicrate

ECAL

Elettronica / VLSI

- **6 m.u. microelectronics design**
 - Mazza, Dellacasa, Rolo
- **1 m.u. test-PCB design**
 - Mignone, Rotondo



Richieste CMS 2018 - Lab. Tecnologico



Dattola	11 m	Infrastruttura per Studi di Longevita' dei DT alla GIF++/ Schermo protezione per MB4 (DT)
Tecnico Lab. Tecnol.	3 m	Infrastruttura per Studi di Longevita' dei DT alla GIF++
Coli	20%	Progettazione meccanica Barrel Pixel
Mereu	20%	Progettazione meccanica Barrel Pixel



Richieste CMS 2018 - Lab. di Elettronica



Mazza	20%	Progettazione ROC
Rivetti	10%	
Rolo	10%	
Dellacasa	7 m	
Wheadon	20%	Test DAQ per prototipi ROC
De Remigis	40%	Progetto DT nuovo Minicrate
Rotondo	7 m	Progetto DT nuovo Minicrate
Rotondo/Mignone	1 m	Disegno PCB per test prototipi ECAL
Mazza/Dellacasa/Rolo	6 m	ADC/Transceiver ASIC
Rotondo	2 m	Disegno PCB per test prototipi ROC
Zampieri	1 m	Supporto per setup di test
Pini/Dumitrache	2 m	Wire-bonding rivelatori CT-PPS e Pixel Fase 2



Backup

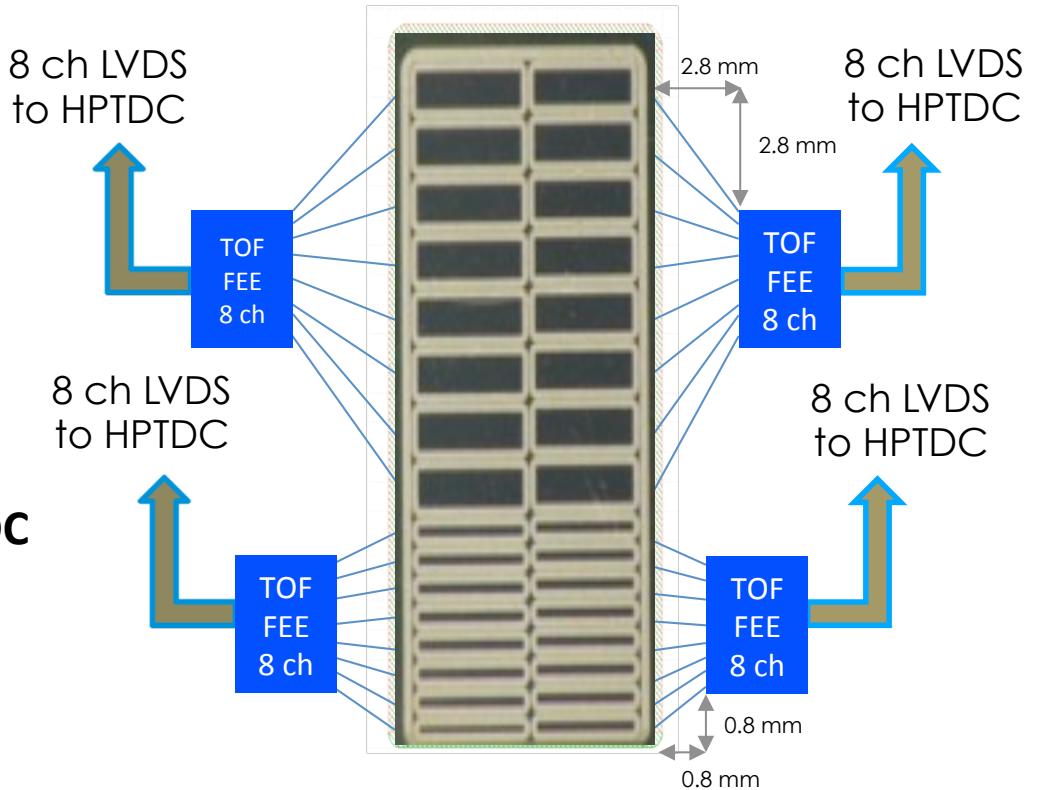




UFSD for CT-PPS



- Sensor production at FBK and CNM.
50 um sensors with CT-PPS design
- Electronics: two possible options
1) Baseline solution:
 UFSD + pre-amp + NINO + HPTDC
2) Advanced solution:
UFSD + custom ASIC (TOFFEE) + HPTDC



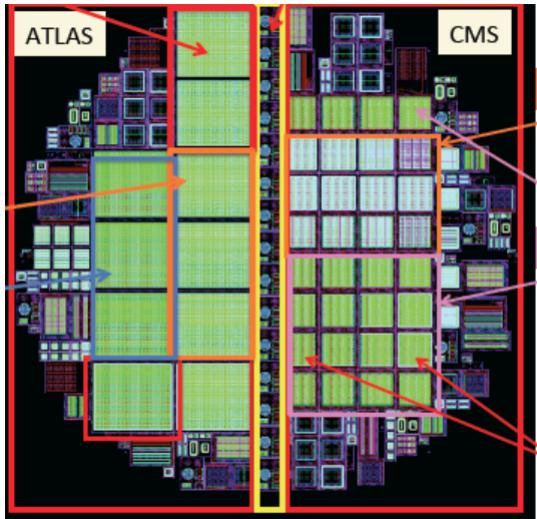


TK R&D on pixel sensors



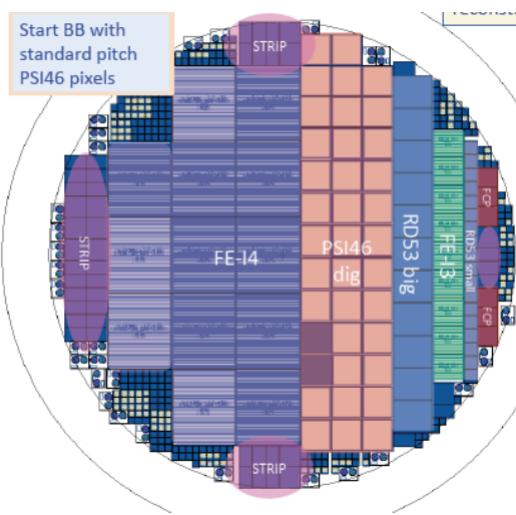
Several submissions ongoing to select technologies and configurations

Finished:



FBK Planar Active Edge

Sensors delivered
Bump-bonding in preparation



FBK 3D

Detectors went to test beam

Soon:

INFN

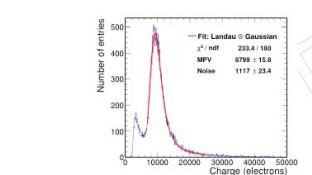
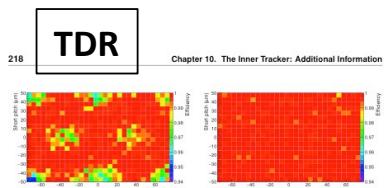
- FBK Planar Active Edge
- FBK 3D Active Edge

CMS

- HPK Planar



Beam test: Charge Collected in 130 μ m 3D Compared to Planar



for intellectual property); pixel chip architectures; and simulation framework for evaluation and optimization. A large number of test circuits have been submitted in the chosen 65 nm technology and these have been extensively tested and verified for performance and required functionality. Two small scale pixel chips have been prototyped and have been undergoing extensive verification and testing programs. A large scale pixel chip demonstrator, referred to as RD53A, is in the process of being finalized for submission in June 2017.

In the following paragraphs a short overview of each of these activities along with the respective status is given. Section 10.2.1 describes the radiation hardness of the technology, including simulations and results obtained from the irradiation of a dedicated test chip. The prototyping of four different analogue frontends is described in Section 10.2.2.2, along with first results of different pixel chip designs developed and tested. The digital part is treated in Section 10.2.3, while Section 10.2.4 describes the digital chip architecture and its simula-

Planar and 3D prototypes
on the same beam test
session at FTBF

I risultati INFN R&D sono parte
integrante del TDR

Anni 2015-16-17

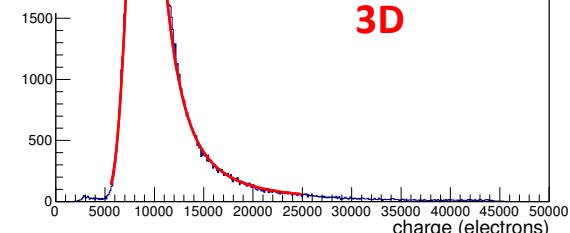
2 campagne irraggiamento con
neutroni e protoni
4 TB FNAL, 1 TB CERN

Standard pixel prototypes 100x150 μ m, 130 μ m active thickness

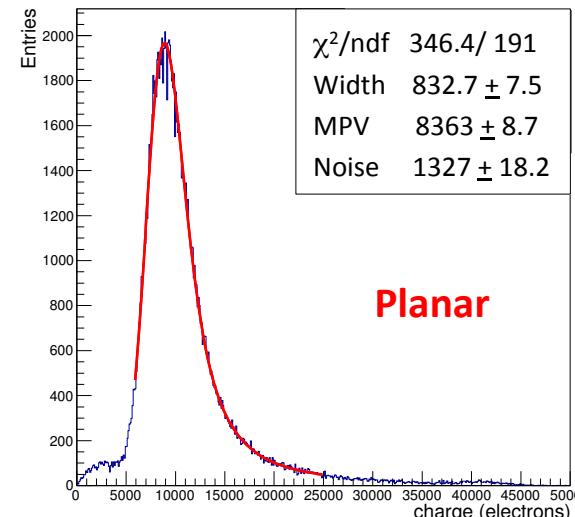
Bump pad not on column

χ^2/ndf	644.5 / 191
Width	715.5 ± 4.3
MPV	8449 ± 5.6
Noise	906.5 ± 8.4

3D



Planari assottigliati fino a 180 μ m !



- Charge collection performance on 3D columnar prototypes is comparable to planar ones (@ higher V_{bias})