R&D Program on Microelectronics for the DarkSide Project
Status and Outlook for 2018

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Overall Review Process and Status of Darkside

- 2015/12: DS-20k Proposal Submitted
- 2016/04: Successful joint INFN and NSF merit review (excellent for "Intellectual Merit" and "Broader Impact")
- 2016/10: LNGS and first CTS review
- 2017/04: INFN-CSN2 and LNGS-SC approval:

  ... the CSN2 has highly appreciated the scientific potential of DS and has unanimously approved the project for a total budget of 5 M EUR (investment) in the years 2017-2020, with the goal of having the experiment built and running at the end of 2020.
- 2017/06: NSF budget review ongoing
- 2017/06: second CTS review
- 2017/06: New collaboration agreement with Canada Institutes (Carleton, TRIUMF, Laurentian, Alberta, Queen's, SNOLAB) for a global argon program - capital funding request submitted
- **14 INFN Sections** participating to the Darkside Program

VLSI design for DarkSide: scope and plans

- Dual TPC DS-20K baseline solution based on cold discrete electronics, 5210 SiPM (analogue differential) readout channels per TPC
- **Strong interest from Collaboration** to pursue an R&D on cryogenic CMOS IC readout electronics for fast sensors

↪ **INFN Torino invited** to join the Darkside Collaboration (June 2016)

- Research Line 1: system-level study for a distributed sensor network for multi-ton direct dark matter detectors
  - aggressive pixelisation of SiPM tiles to allow binary mode readout (photon counting) on S1 and S2?
  - deploy a smart sensor network with data-in/data-out capability **or** use stand-alone multi-channel ASICs and a cold data concentrator?

  ↪ validation of a time-based readout architecture, needed to disentangle critical light statistics, sensor and electronics design parameters

- Research Line 2: design and characterisation of cryogenic CMOS mixed-signal circuits for SiPM readout

  "Typically it requires three times as many resources and development time to design microelectronic circuits for cryogenic temperature than for room temperature" - G De Geronimo

  ↪ Need for a first silicon to evaluate CMOS UMC110AE at cryogenic operation
  - should feature test structures for parameter extraction (g_m, V_{th},...)
  - noise performance of MOSFETs down to 77K
  - VFE compatible with DS-20K SiPM tiles (24 SiPMs, 1x1 cm^2)
  - debug probing of analogue front-end (noise, signal slew-rate, bias and DC drift at 77K)
  - digital timing criticality at low-temperature (timing slacks, multiple clock domains)

Plans for a first multi-channel ASIC prototype

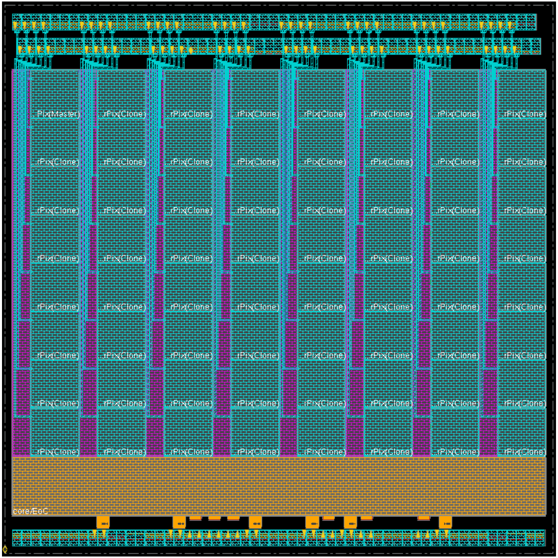
- **Kick-off: multi-channel mixed-signal IC for SiPM readout**
  - testbench for low-temperature noise operation of DSM CMOS technology (110nm node)
  - need for a system-grade ASIC to test SiPM tiles and DAQ
  - focus on a time-based binary readout with time-over-threshold
- Pixel architecture based on leading-edge discriminators and low-power analogue TDCs based on time interpolation
  - sub-ns time stamp on rising and fall edge of fast discriminator output
  - on-chip clock up to 320 MHz (defines TDC binning and data rate)
    - Problems with logic at low temperature (timing slacks, propagation speed)?
      ↪ Run slower, the Wilkinson-based TDC would still cope with the event rate
    - Problems with the analogue TDC at low temperature?
      ↪ Don't use it, generate a coarse time only (time bin = T_{clk})
  - pixel generates event data: time-of-arrival and time-over-threshold
- Fully digital LVDS data and SPI configuration IO
- 64-pixel prototype: maximum matrix size on a (minimum slot) 5x5 mm^2 UMC110AE MPW
- turn-off capability (power-hungry analogue) of unused pixels, masking of screamer pixels
- Design target: 10-15 mW per Pixel (1 cm^2 SiPM)

↪ low-temperature aware design of a VFE for SiPM readout started

↪ chip floorplanning and top integration started

↪ use INFN-Torino silicon-proven IP (discriminators, TDCs, IO drivers, power management)

Plans for the first multi-channel ASIC prototype - Floorplan



- 64 mixed signal pixel matrix, organised in 8 columns
- Pixel hosts SiPM VFE, leading-edge discriminator, 4 TDCs, digital control and interface
- Time-stamp data (Leading edge, ToT) generated on-pixel is propagated along the column
- Distributed bias and power management blocks
- End-of-Column collects data, serialises and manages data links, SPI and column/pixel configuration
- Up to 4 LVDS TX data links, SPI IO, digital power
- VFE input, analogue power, debug for VFE and device characterisation

↪ First ASIC Prototype MPW submission: target Q4 2017

- System-grade design at room temperature
- Testbench for CMOS VFE at cryogenic temperature

↪ Electrical Characterisation and Laser tests with SiPMs at Room Temperature - Torino

↪ System-level Performance Assessment with **ReD** - Napoli

- an experiment to sense **RE**coil **D**irectionality in LAr
- **ReD** TPC instrumented with Darkside R&D SiPM tiles
- privileged test bench for an integrated cold mixed-signal electronics
- success of the **ReD** experiment could have crucial impact on the broader program for Darkside!

↪ Chip design activities on 2018 - design revision towards a second submission during 2019

Requests: Servizio Elettronica

- **Marco Mignone** - 3 mesi test board design (1.5 months contingency cryogenic operation)
- **Giulio Dellacasa** - 5 mesi, chip design
- **Richard Wheadon** - 25%, test setup development (FW/SW)
- **Manuel Rolo** - 40%, chip design

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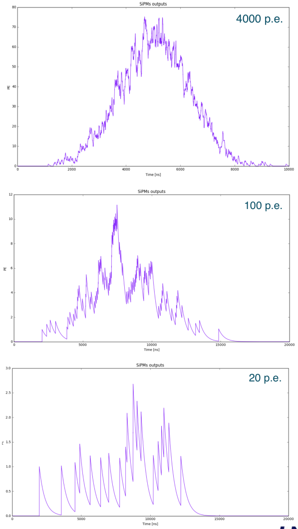
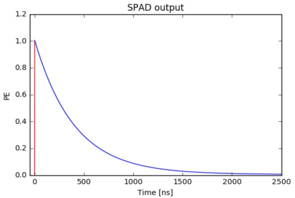
Thank You!

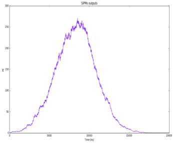
Backup Slides

Towards a binary cold FEE readout: premises

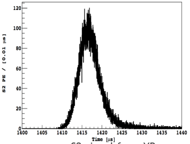
- Readout of 25 cm^2 SiPM tiles is a big challenge for the cold FEE - noise, dynamic range
- Warm electronics for signal digitisation (S2), good engineering and cold optical transceiver can preserve signal integrity. Scalable solution?
- An integrated electronics targeting the same readout discipline would be a **very. big. challenge.**
- Ongoing R&D on cold electronics (FE+ADC ASICs) for LAr TPCs in dark matter experiments or neutrinoless double beta decay (nEXO), also using SiPMs (BNL)
    - *amplification, sampling, digitisation, charge calibration, good energy resolution*
    - *triggered data transfer - energy deposition threshold in the center of the TPC*
- **Can we change paradigm?**
    - is there a pixelisation of the TPC SiPM tiles such that the amount (and time distribution) of photons in S1 and S2 can allow a binary readout?
    - can this be achieved with a relatively low amount of power?
    - how could we read this enormous amount of channels?



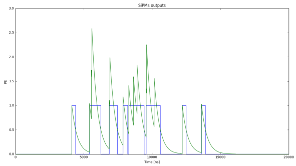




S2 signal generated in python



S2 signal from YB



- Generate with Python a high-Rq single SPAD p.e. signal ("old" $R_q = 40M\Omega$), normalised amplitude
- From TPC simulation results (1 cm^2 pixels), generate a normal distribution to map the mean arrival time of the photons
- Monte-Carlo results do not include QE and FF of the SiPM
- Consider the maximum number of p.e. of S2 signal in the SiPM that sees most light (ongoing studies including simulation results with adjacent pixels)
- Set a threshold to 0.5 p.e. on an ideal discriminator
- Evaluate efficiency of a binary readout
- Evaluate efficiency of time-based readout scheme (time stamp + ToT)

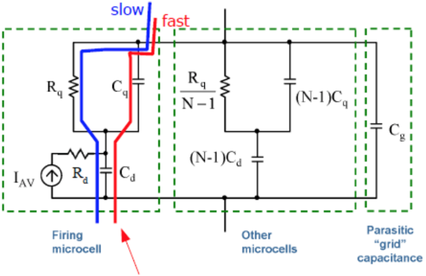
SiPM equivalent circuit (small signal model) and pulse shape

Single cell model → $(R_d||C_d)+(R_q||C_q)$
SiPM + load → $(||Z_{cell})||C_{grid} + Z_{load}$

Signal = slow pulse ($\tau_{d\,(rise)}, \tau_{slow\,(fall)}$) +
+ fast pulse ($\tau_{d\,(rise)}, \tau_{fast\,(fall)}$)

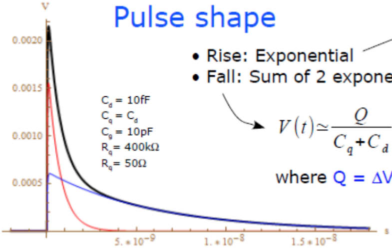
- $\tau_{d\,(rise)} \sim R_d(C_q+C_d)$
- $\tau_{fast\,(fall)} = R_{load}\ C_{tot}$ (fast; parasitic spike)
- $\tau_{slow\,(fall)} = R_q\,(C_q+C_d)$ (slow; cell recovery)

F.Corsi, et al. NIM A572 (2007) 416
S.Seifert et al. IEEE TNS 56 (2009) 3726



Cq → fast current supply path in the beginning of avalanche

Pulse shape



- Rise: Exponential → Sp.Charge Rd x Cd,q filtered by parasitic inductance, stray C, ... (Low Pass)
- Fall: Sum of 2 exponentials

$$V(t) \simeq \frac{Q}{C_q+C_d}\left(\frac{C_q}{C_{tot}} e^{\frac{-t}{\tau_{FAST}}} + \frac{R_{load}}{R_q}\frac{C_d}{C_q+C_d} e^{\frac{-t}{\tau_{SLOW}}}\right) \quad \text{for } R_{load} << Rq$$

where $Q = \Delta V\,(C_q+C_d)$ is the total charge released by the cell

→ 'prompt' charge on C_{tot} is $Q_{fast} = Q\ C_q/(C_q+C_d)$

(slide taken from presentation of G. Collazuol at PD-2012)

Yu. Musienko, INSTR-17, Novosibirsk 5