CHIPIX65

Web-site: http://chipix65.to.infn.it

CALL Project CSN5 approved in October 2013

Development of an innovative **CHIP** for a **PIX**el detector, using a CMOS **65**nm technology for the first time in HEP community, for experiments with extreme particle rates and radiation at future High Energy Physics colliders.
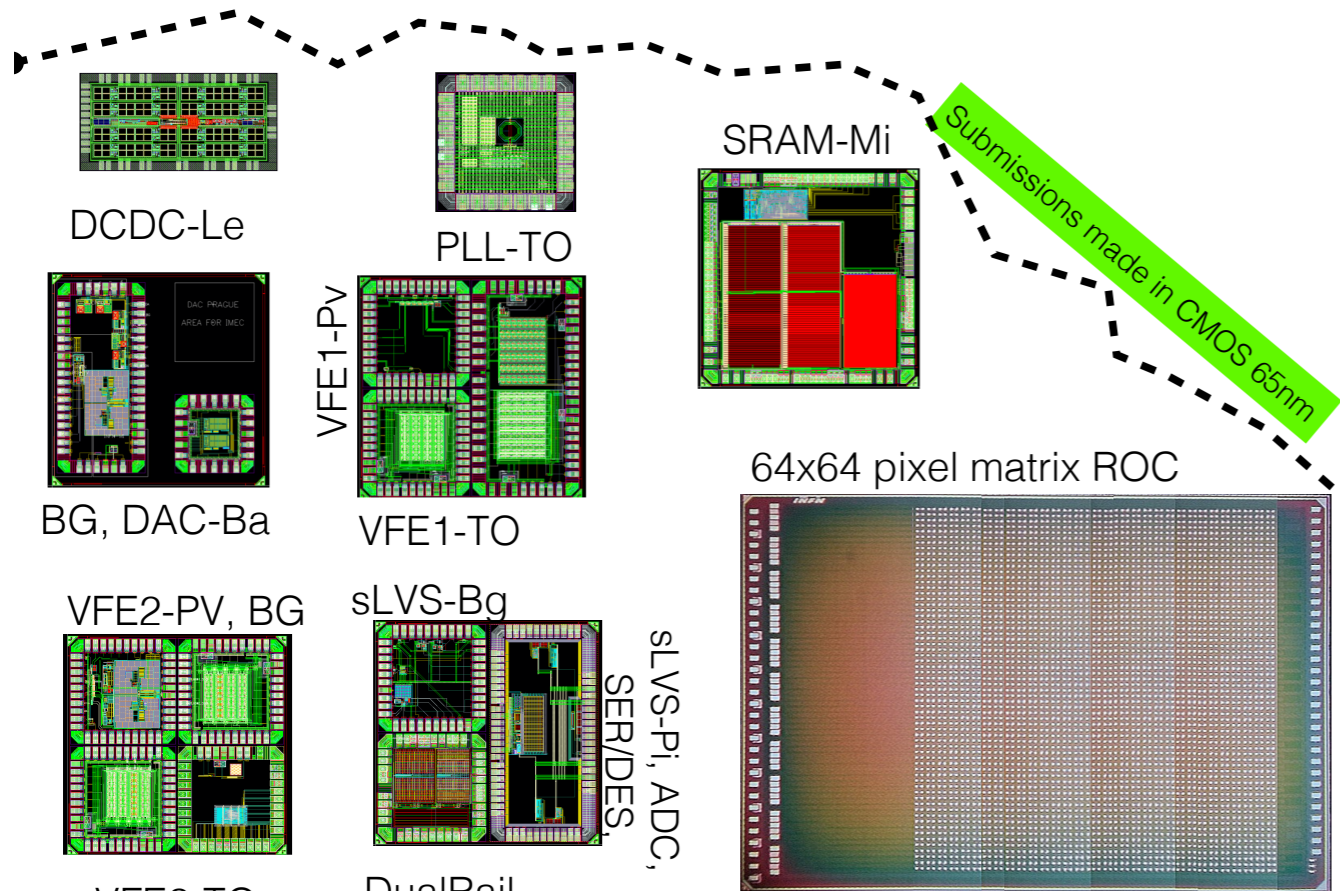
Principal Investigator : Natale Demaria - INFN/Torino

Institutes:
Bari, Lecce, Milano, Padova, Pavia, Perugia, Pisa, Torino

Funding members of RD53 Collaboration

People (~40 of which 50% ASIC designers; 12.4 FTE)**:**   (Torino: 9 people; 3.4 FTE)

DCDC-Le

PLL-TO

SRAM-Mi

VFE1-Pv

BG, DAC-Ba

VFE1-TO

64x64 pixel matrix ROC

VFE2-PV, BG

sLVS-Bg

sLVS-Pi, ADC, SER/DES

VFE2-TO

DualRail

Submissions made in CMOS 65nm

Work Packages:

Radiation Hardness – A.Paccagnella (Padova)
Digital Electronics   – R.Beccherle (Pisa)
Analog Electronics   - A.Rivetti (Torino)
Chip Integration   - V.Re (Pavia/Bergamo),
                                              V.Liberali (Milano)

Papers / talks / thesis
- 33 talks at International conferences
- 3 degree theses, 5 PhD thesis
- 30 papers on international journals

L.Demaria   — CHIPIX65 —   CdS, 30/06/2017 Torino   1

CHIPIX65: groups and people

- **TORINO**

  N.Demaria, E.Monteil, L.Pacher, A.Paterno', R. Wheadon, S.Panati, G.Dellacasa, G.Mazza, A.Rivetti, M.D.Da Rocha Rolo

- **BARI**

  F.Ciciriello, F.Corsi, C.Marzocca, G.De Robertis, F.Loddo, C.Tamma

- **PADOVA**

  M.Bagatin, D.Bisello, S.Gerardin, S.Mattiazzo, L.Ding, P.Giubilato, A.Paccagnella

- **BERGAMO / PAVIA**

  F.De Canio, L.Gaioni, M.Manghisoni, V.Re, G.Traversi, E.Riceputi, L.Ratti, C.Vacchi

- **PISA**

  R.Beccherle, G.Magazzu, M.Minuti, F.Morsani, F.Palla

- **MILANO**

  V.Liberali , S.Shojaii , A.Stabile

- **PERUGIA**

  G.M.Bilei , M.Menichelli , E.Conti , S.Marconi, D.Passeri , P.Placidi,

- **LECCE**

  S.D'Amico, C.Veri, A.Donno.

~40 of which 50% ASIC designers; 12.4 FTE

CHIPIX65-FE0 demonstrator

5,15 mm (vertical left axis)

3,46 mm (horizontal bottom axis)

Labels on chip: 1a, 1b, 2, 3, 4, 5
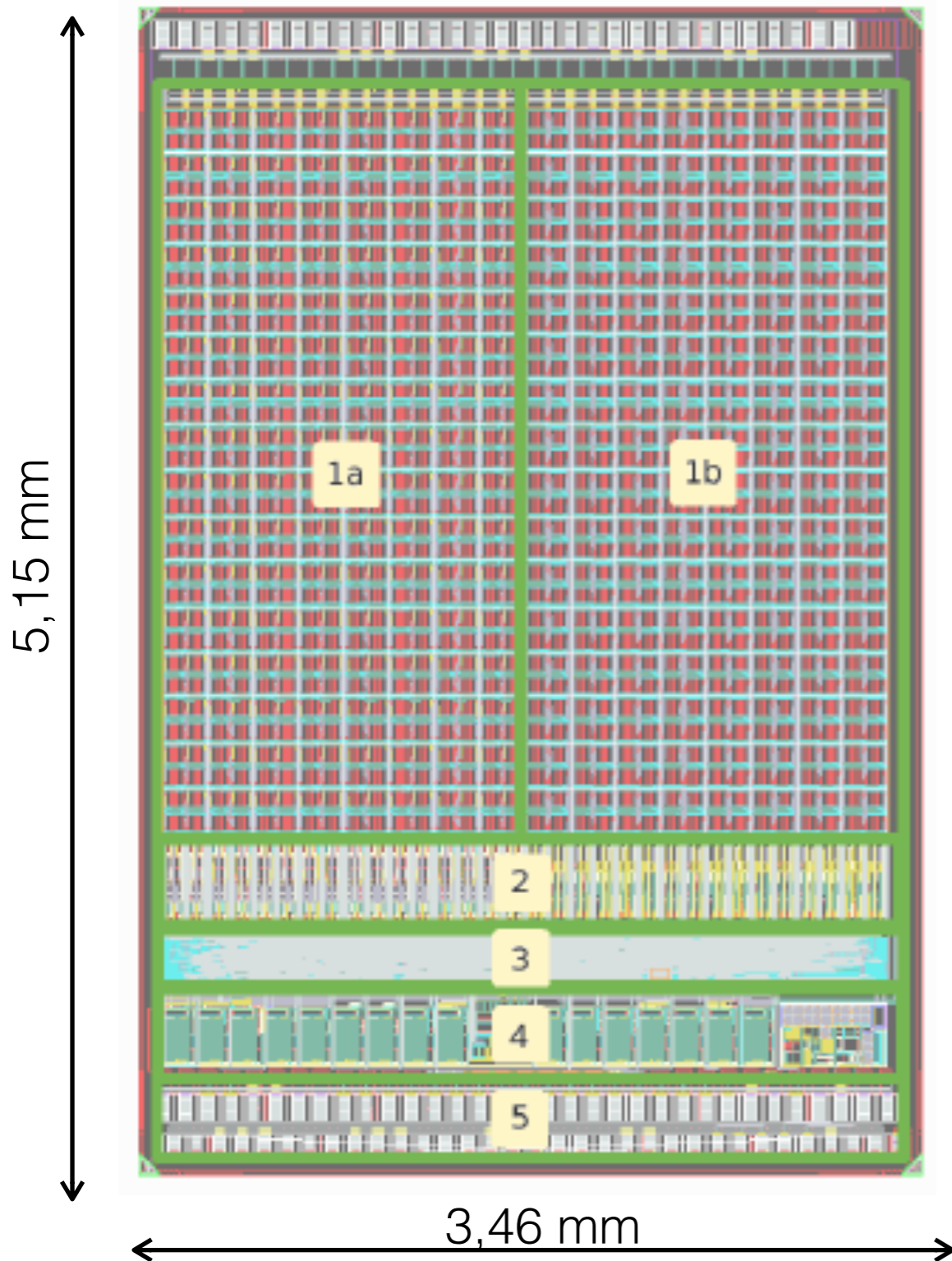
64x64 pixel matrix - 50x50 um²
Organised into (4x4) Pixel Region

HL_HLC flux rates: 3 GHz/cm²
Trigger latency : 12,5 us
In-time threshold : 1200 e-
Noise ~100e- @50fF input capacitance

Dimensions: 3,463 mm x 5,148 mm
~3M of digital standard cells

Full INFN development (about 1 year work):
- Two Analog Very Front Ends
- IP-block
  (DAC,ADC, I/O, BandGap, sLVS-TX/Rx, Serialiser)
- Digital design, digital-on-top, chip integration

~15 Millions of transistors

submitted: 5/7/2016
Arrived: 26/9/2016

CHIPIX65-FE0 Design Team

CHIPIX Integration and Floor Planning

L.Pacher(*)

Digital

A.Paterno(*), L.Pacher (*)

Analog Front Ends

E.Monteil(*), L.Gaioni(*), L.Ratti

IP-Blocks

F.De Canio(*), G.Traversi, F.Loddo(*), G.Magazzu, C.Marzocca, **F.Liciulli, F.Ciciriello**

Analog Bias and Monitoring

F.Loddo

Architecture Simulation and Verification

S.Marconi(*), E.Conti(*), G.Mazza, G.Dellacasa

Young researchers
are strongly contributing
(in bold).

(*) : also part of RD53A
design team

PSI46 (150um x 100um)
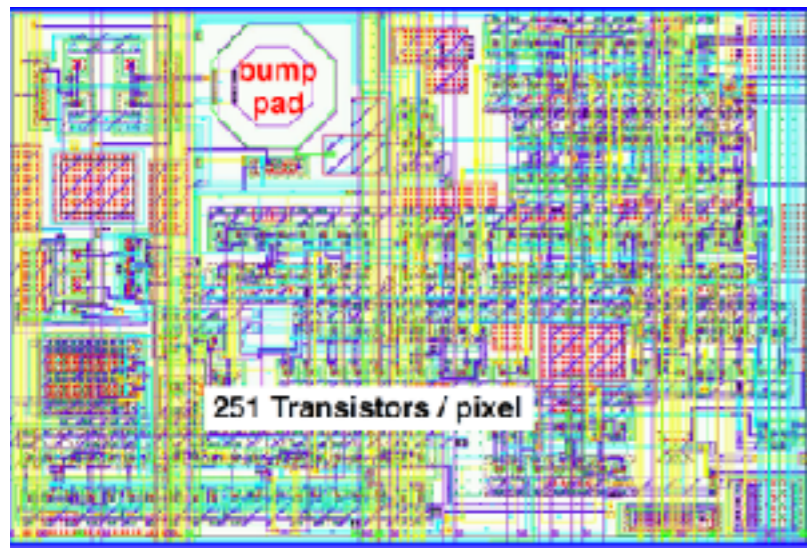
- 250nm CMOS tech
- **251** transistors/pix

FEI4 (50um x 250um)

- 130nm CMOS techn
- ~**2500** transistors/pix
- ~0,5 trans/um^2

YES !

65nm technology allows to design a smaller pixel capable to sustain extreme particle fluxes and long latencies
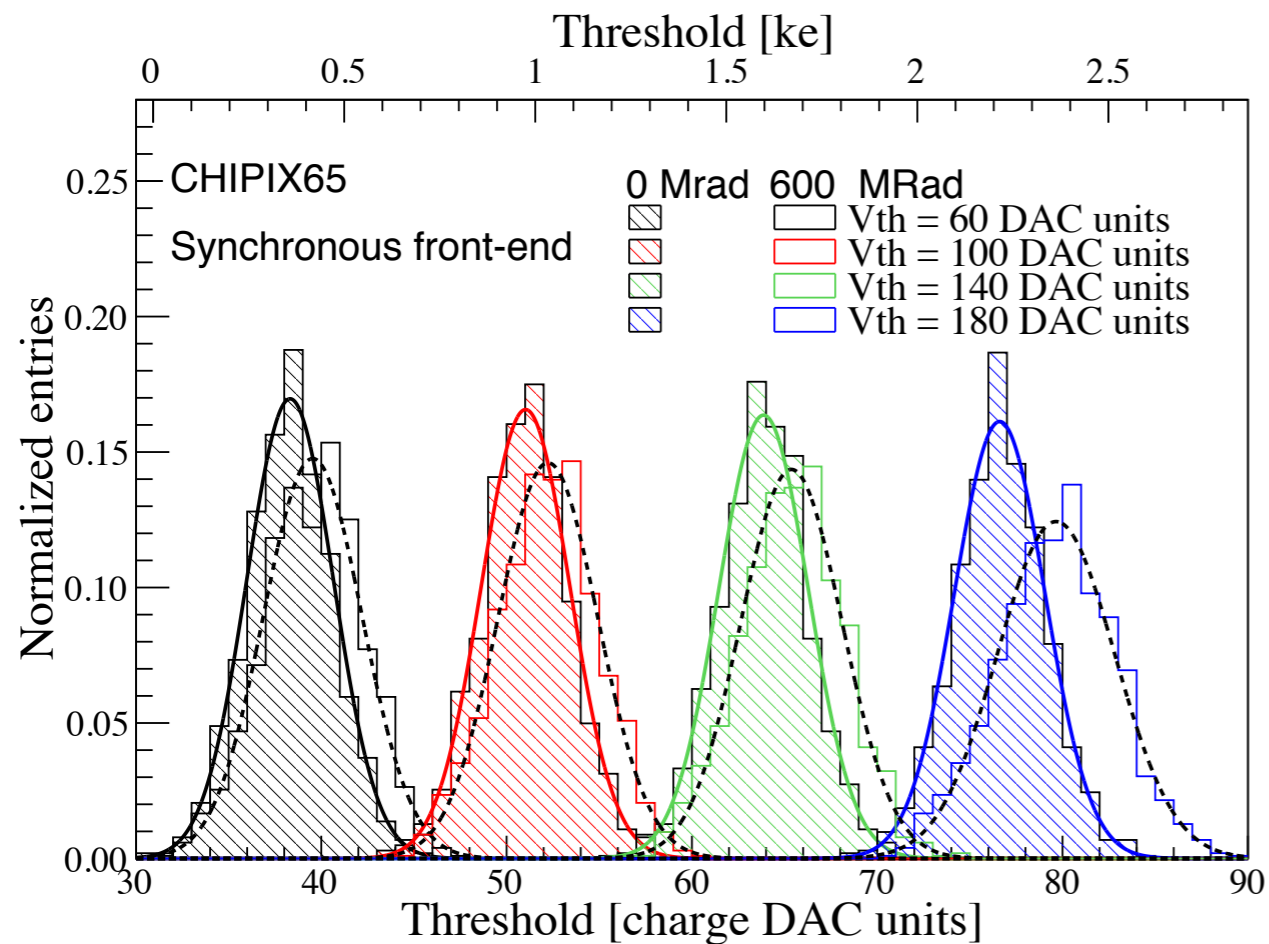
RD53 / CHIPIX65
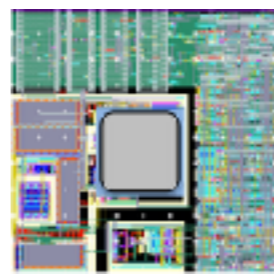
(50um x 50um)

- 65nm CMOS tech
- ~**2500** transistors/pix
- ~2 trans/um^2

50% of area to digital

VFE-TO: threshold and Noise

- **Low threshold < 500e⁻ for all pixels**
  Dispersion~90e- with no need of trimming (auto-zero technique)

- **Noise ~100 e⁻**

- Irradiation test - TID = 600 Mad @ -20C
  - **chip is still fully operational**
  - increase of the dispersion is below 10%
 - ENC shows around 10% increase

VFE-TO: Linear, Fast-ToT

32 counts=100ns

Charge res= 200e-

injected charge in DAC units
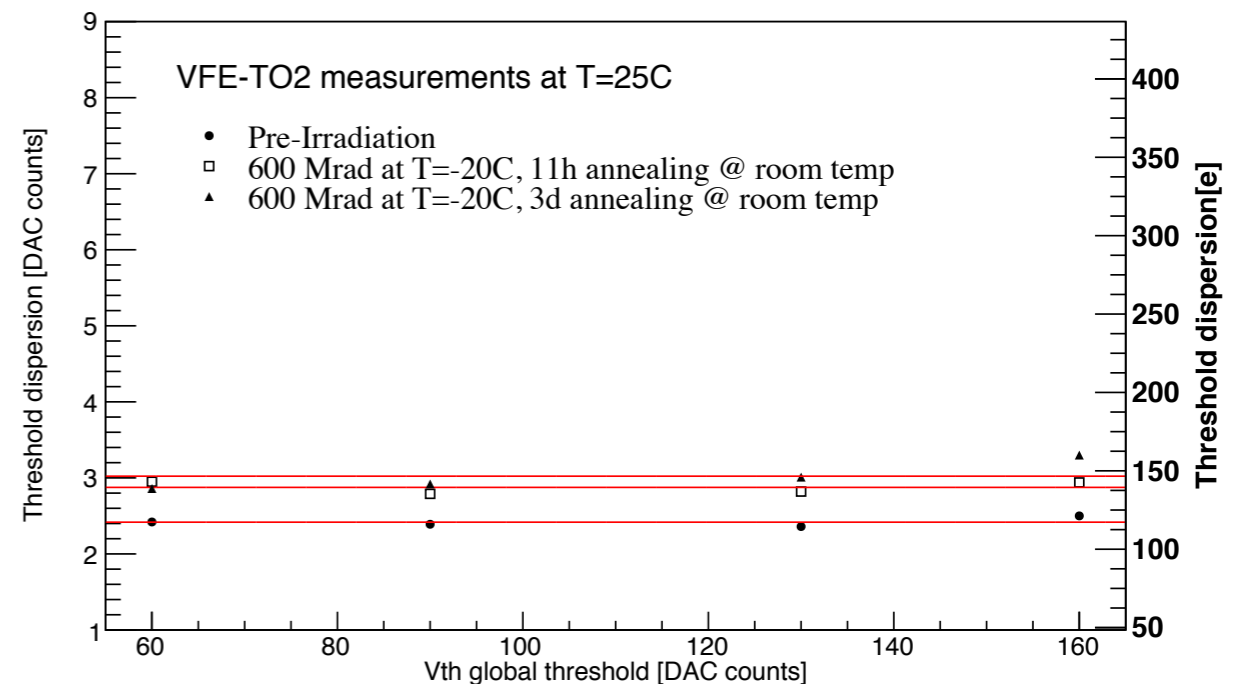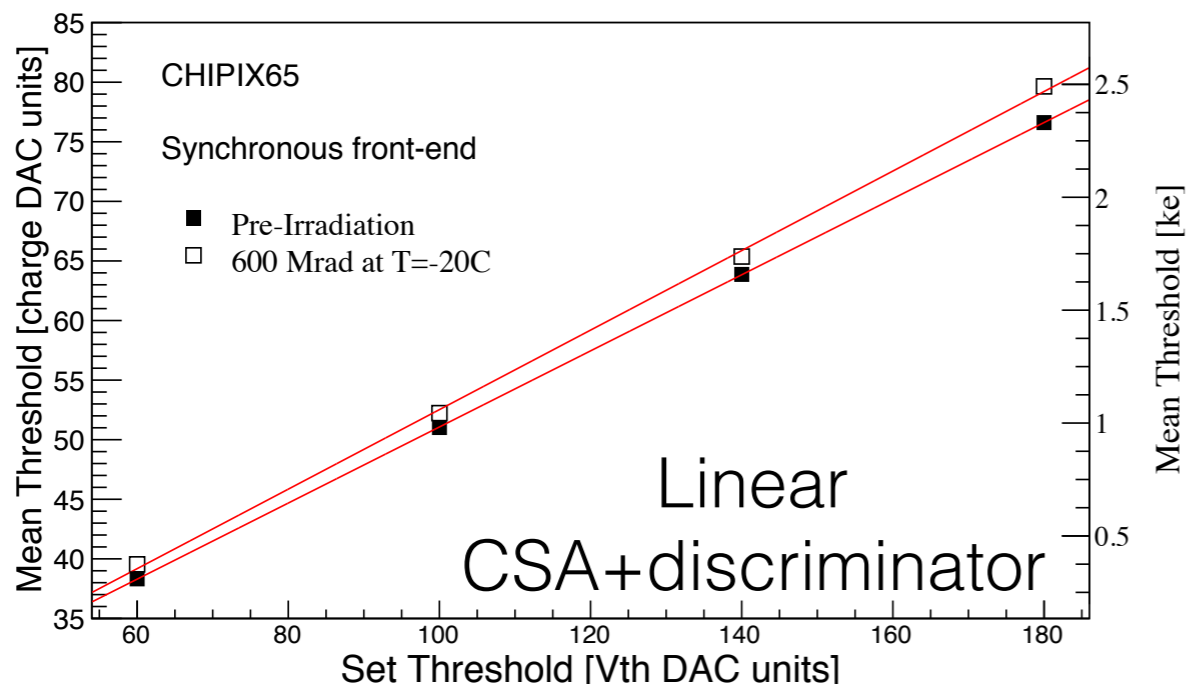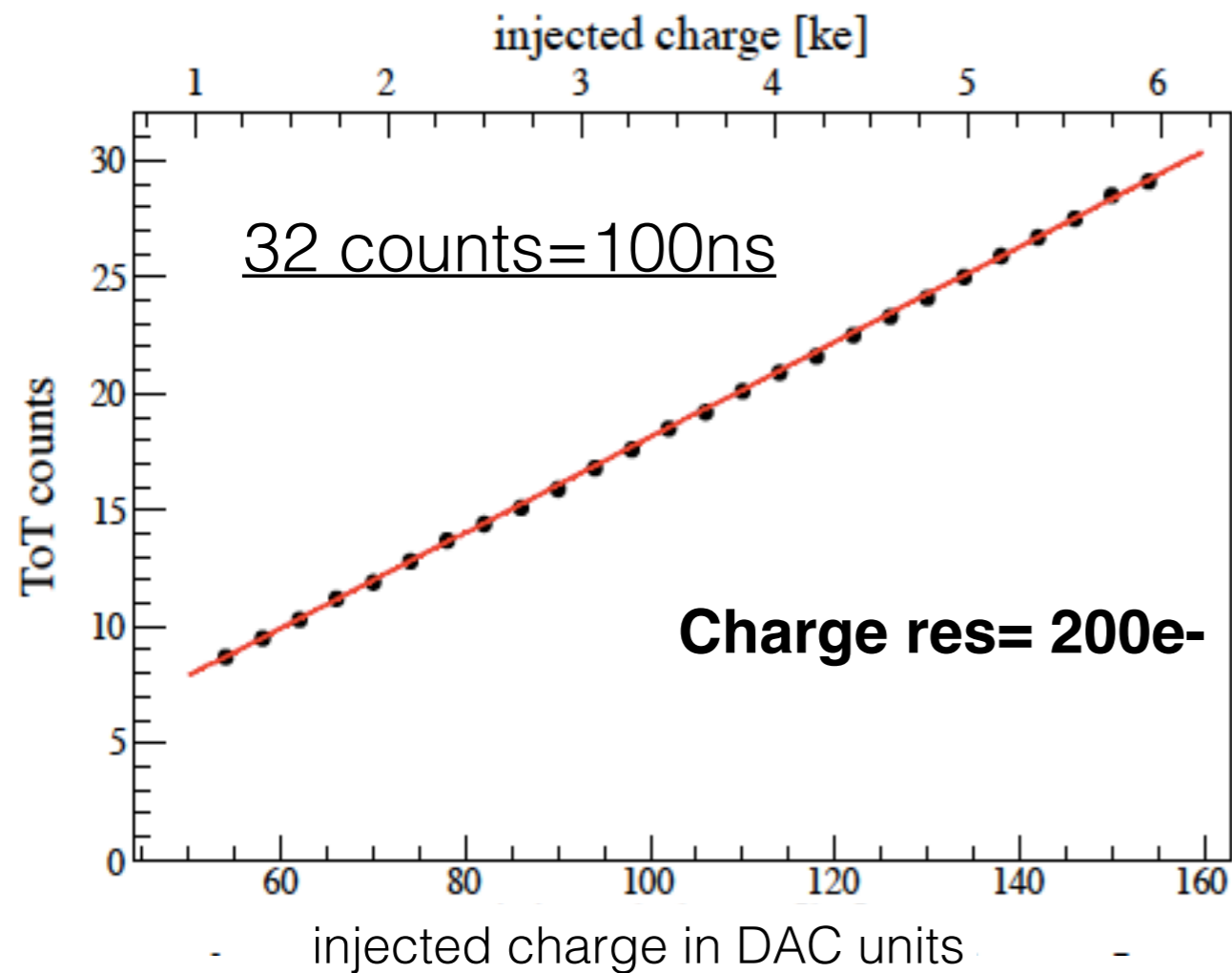
- Good ToT Linearity - **5 bit ToT**
- Gain dispersion ~12% (good)
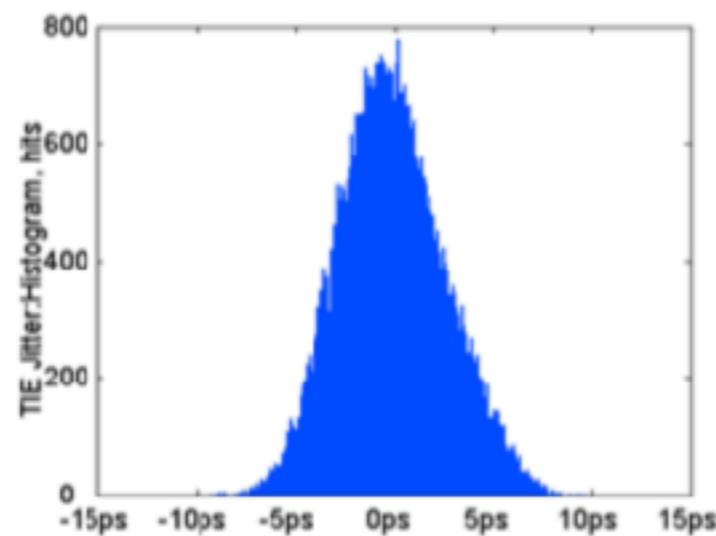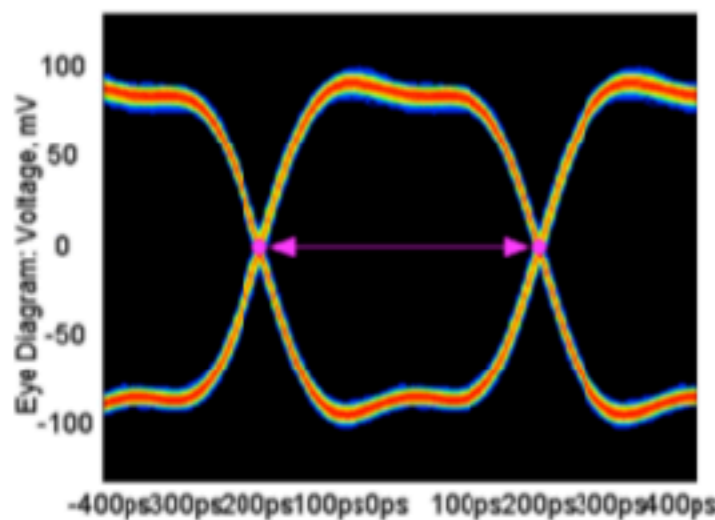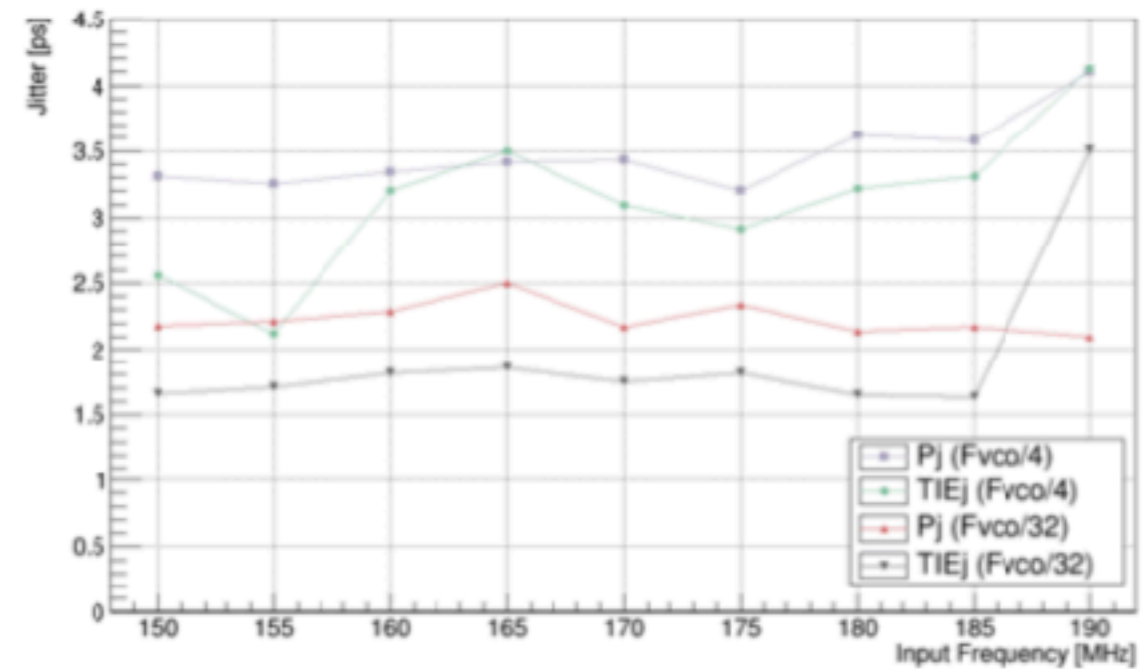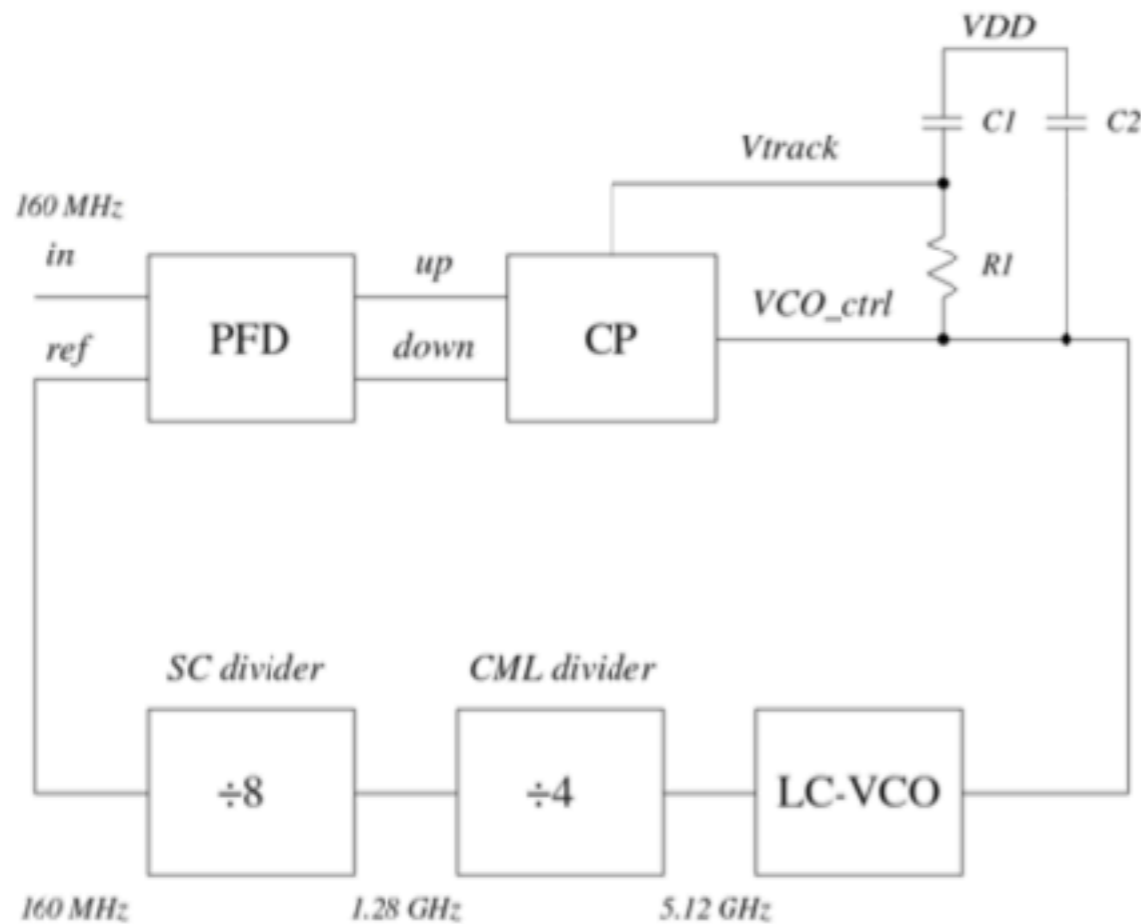- digitisation is less then 100ns (low impact in analog pile-up inefficiency)

- Measurement with **320MHz** Fast ToT
- Little decrease after irradiation but can be tuned back to value before irradiation
- dead-time ~ 0.2% for m.i.p.
- almost no increase in power
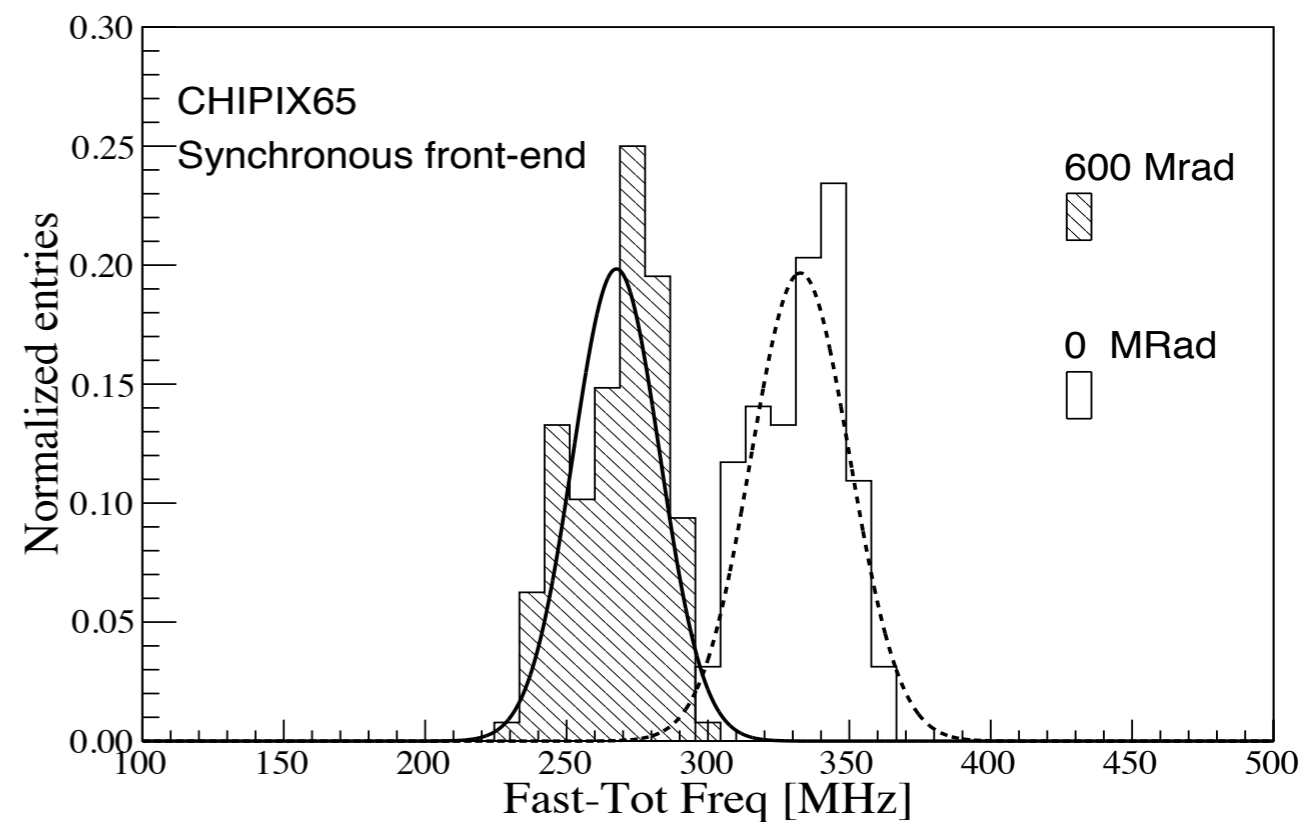
5.12 GHz CP-PLL

Sezione di Torino

* Input frequency : 160 MHz

* LC-based oscillator

* Oscillator frequency : 5.12 GHz

* Output frequencies : 1.28-2.56 GHz

* Technology : CMOS 65 nm

G.Mazza

RD53A (1)

RD53A is a chip-of-chips with 3 analog front-ends
(output of the cores is the same for each)

Synchronous

synchronous discriminator can be used for a fast ToT counter

~Chipix65 demonstrator~

Linear

single amplification stage for minimal power consumption

Differential

differential threshold reduces coherent noise

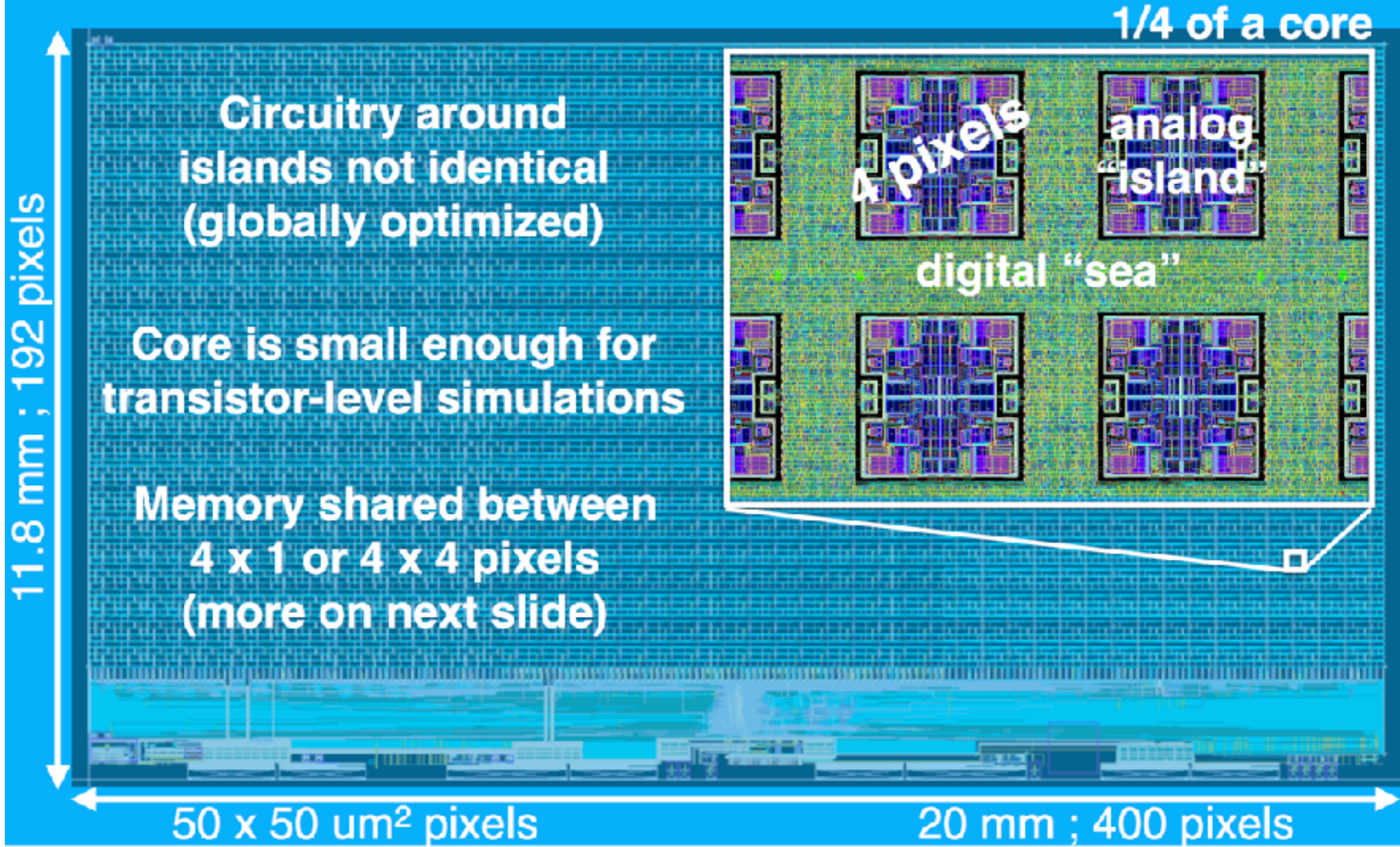*~FE65P2 demonstrator~*

11.8 mm ; 192 pixels

50 x 50 um² pixels

20 mm ; 400 pixels

The pixel matrix is organized into 8 x 8 pixel cores

1/4 of a core

Circuitry around islands not identical (globally optimized)

Core is small enough for transistor-level simulations

Memory shared between 4 x 1 or 4 x 4 pixels (more on next slide)

4 pixels

analog "island"

digital "sea"

11.8 mm ; 192 pixels

50 x 50 um² pixels

20 mm ; 400 pixels

RD53A essentials

Analog VFE	Building Blocks	Digital Blocks	Integration/ Verification
FE-Lin	10b-Current DAC	(2x2) DBA Pixel Region	DRC verification
FE-Sync	12b-voltage DAC	(4x4) CBA Pixel Region	LVS Verification
FE-Diff	Band Gap reference 1.2V	Pixel Configuration	Virtuoso Integration
	BandGasp Reference 2V	Command Decoder	Innovus Integration
	ShLDO voltage regulator	Data Concentrator	Voltus
	Power On Reset	Aurora 64b/66b	Tempus
	Command Data Recovery + PLL	JTAG	VEPIX53 (SystemVERILOG)
	Serialiser	DFT	ADE-XL
	SLVS Driver	Data Compression	RTL
	SLVS Receiver	Global Configuration	Verilog
	CML driver	Ch-Sync	HSIM
	12b-Monitoring ADC		Verilog AMS
	Analog Buffer	4b-Latch	
	Ring Oscillator	DICE-Latch	
	Radiation Sensor		
	Temp Sensor		

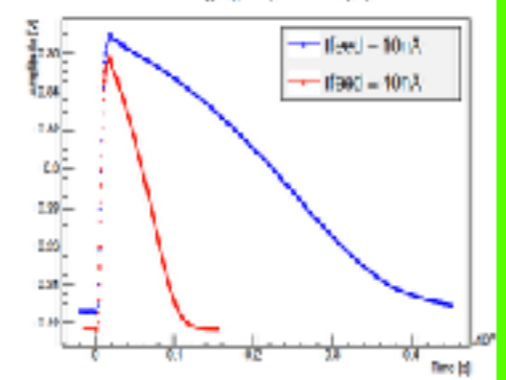Almost ALL of these are Intellectual properties ! INFN ~50%
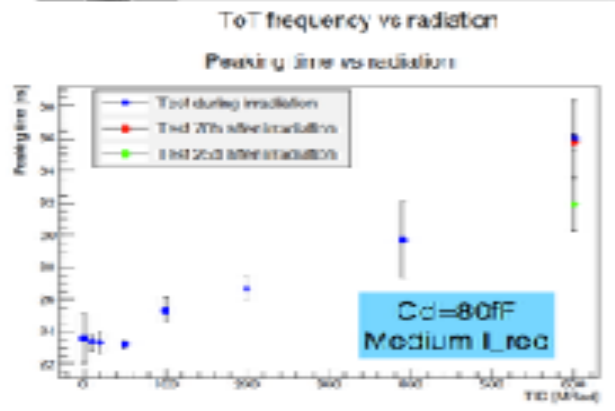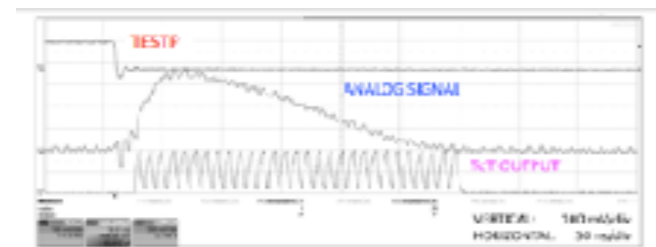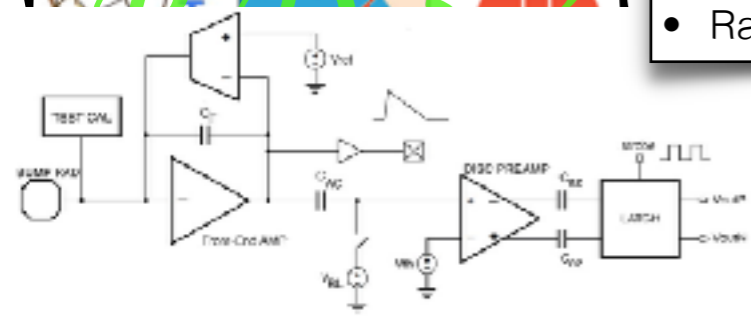
Conclusion

- The use of CMOS 65nm technology in Front End ASIC is know well established in INFN thanks to CHIPIX65. IP-blocksand VFE-analog chain, digital architecture have been designed, tested and most have been characterised for radiation hardness.

- A demonstrator was build consists of 64x64 pixels, with dimension of $50\times50um^2$ and integrating 'final' IP-blocks and two VFE. Lots of lessons have been learnt and solutions found. It is fully working with performance as required by HL_LHC

- CHIPIX65 is strongly contributing to RD53a, with blocks, ideas, experience realised for the small demonstrator. Large fraction of the design team is from CHIPIX65, including the overall coordination

- RD53a will be submitted soon (this summer); in fall 2017 we will start the testing

- CHIPIX65 project last year is this year.

- Now the INFN will concentrate to the design of HL_LHC Pixel ROC(s) : see more in the CMS presentation !
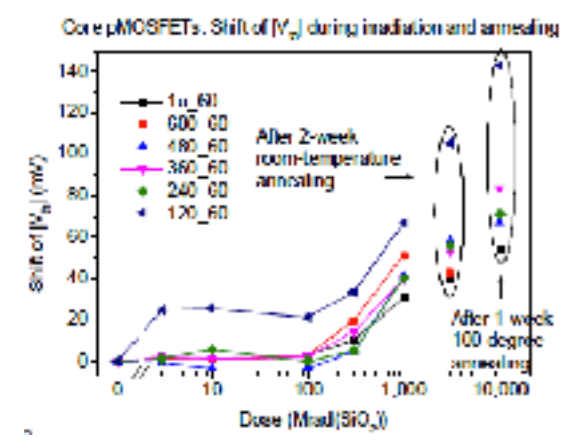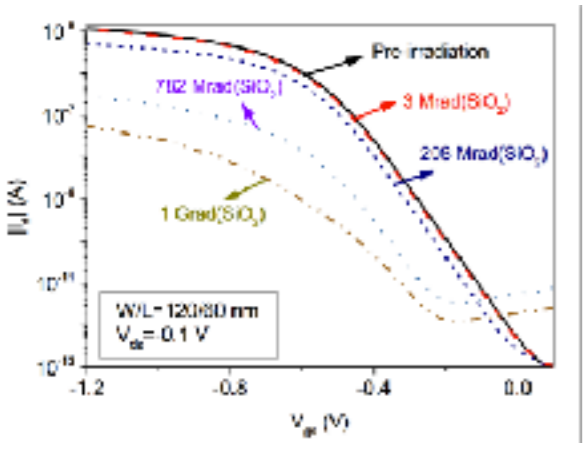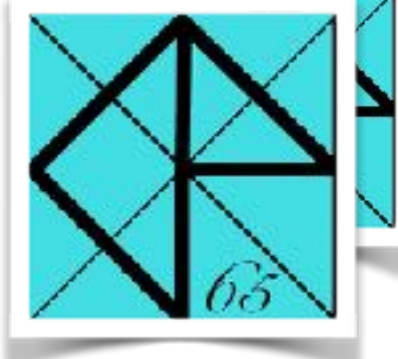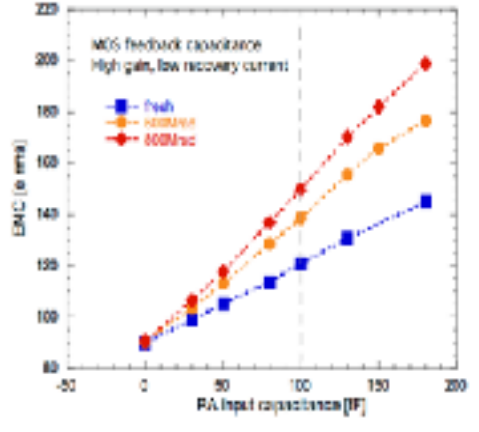
Backup

- Compact: 35x35 um², Low power (<5uW)
- Low Noise (<100e⁻), Fast ToT (~150ns),
- Rad-Hard (6-800 MRad)

Asynchronous designn

ANALOG Very Front ENDs

ToT frequency vs radiation

Peaking time vs radiation

Noise vs Cinput

+7.7%

Pre-irrad

600 Mrad

Cd=80fF
Medium I_rec

Input charge [ke]

IP-Blocks

Measured LSB vs #dac
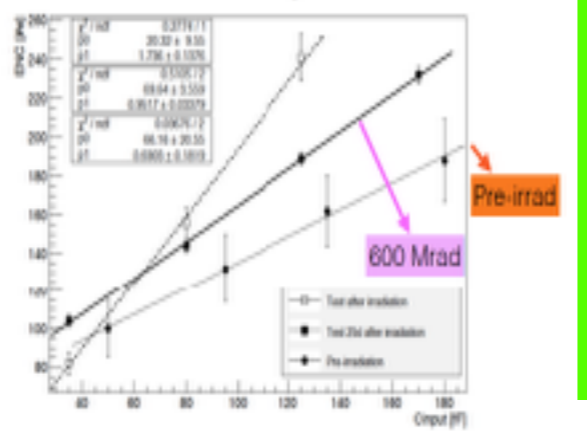
10-bit current steering DAC
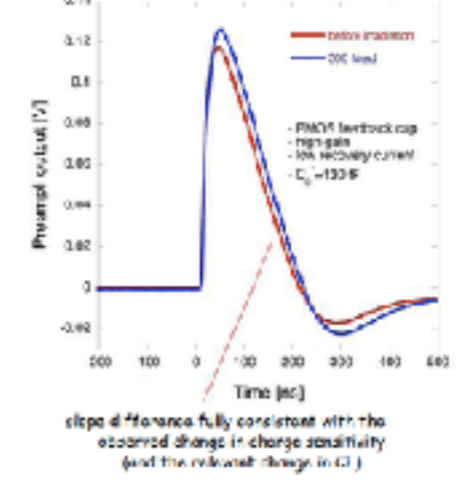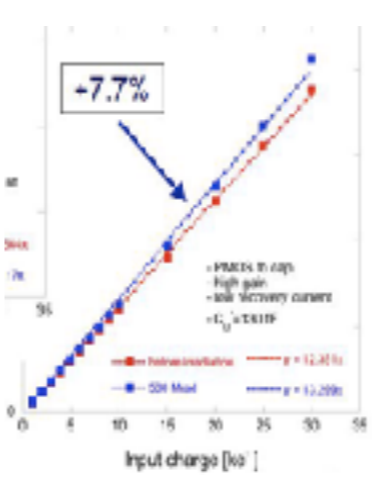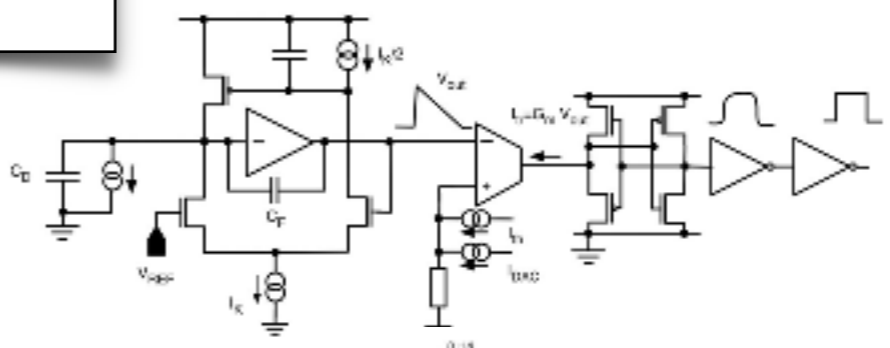
Radiation Characterisation

Eye diagram: SLVS driver@1.2 Gbps
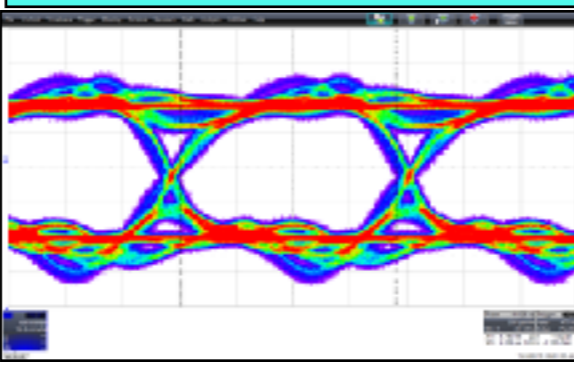
Eye diagram: SLVS receiver@1.2 Gbps

Band Gap for VRef
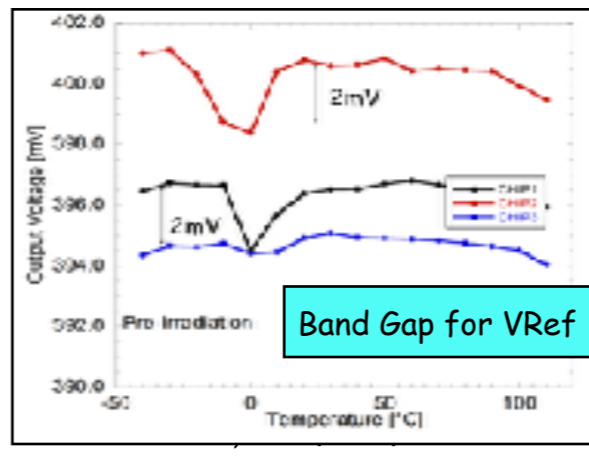
List of CHIPIX65 IP-blocks

- Band Gap   : Pavia
- DAC   :Bari
- SLVDS driver   : Pavia, Pisa
- SLVDS receiver   : Pavia,Pisa
- PLL   : Tor,Padova
- SER   : Pisa
- DES   : Pisa
- Monitoring ADC: Bari
- SRAM EOC   : Milano
- Dual Digital Cell : Milano
- DC-DC   : Lecce