Hybrid and monolithic pixel detectors for X-ray imaging at FELs and synchrotron light sources

XDET

Programma di attività e preventivo di spesa
Sezione di Pavia

Resp. Naz.: Lodovico Ratti

Resp. Loc.: Massimo Manghisoni

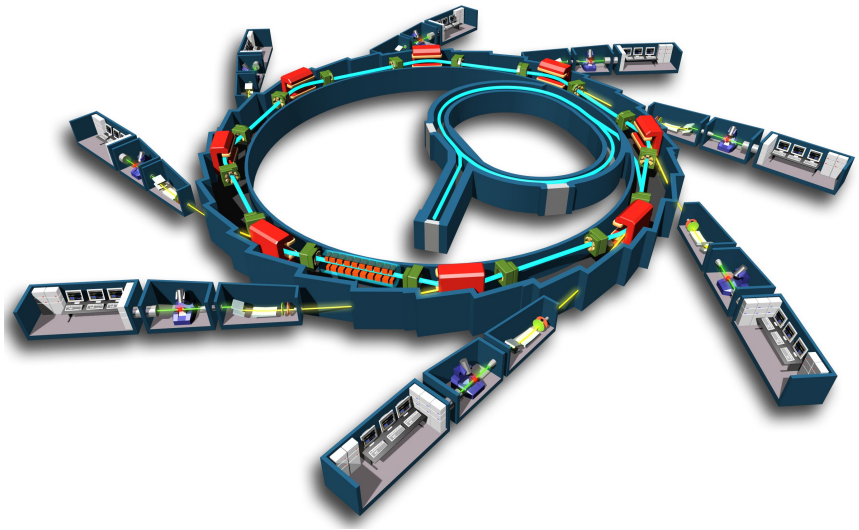
INFN Pavia, Consiglio di Sezione, 6 luglio 2017

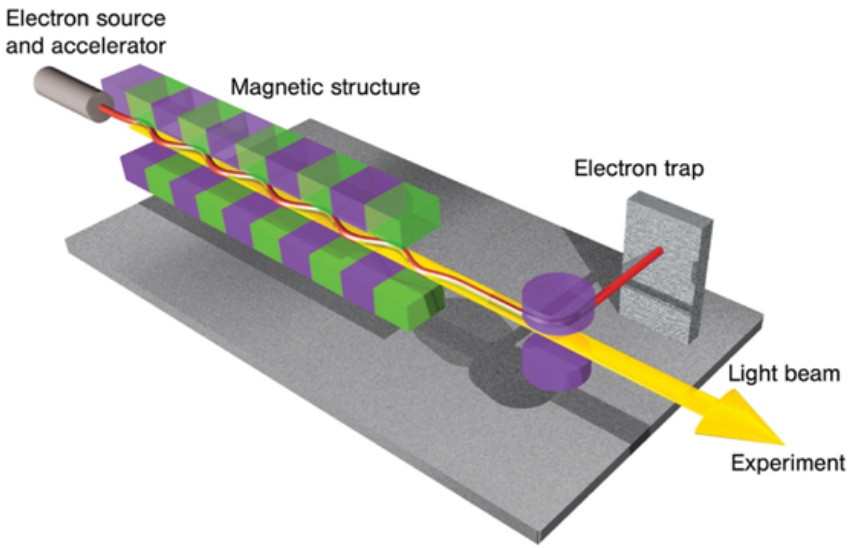
XDET project

- Goal of the project: develop the building blocks for hybrid and monolithic detectors for X-ray imaging at FELs and synchrotron light sources; build a demonstrator based on a 2-tier structure, including the sensor with integrated analog electronics in one layer and digital circuits (memory, readout) in the other
- Duration: 3 years
- Participating INFN groups:
  - INFN Pavia
  - INFN Pisa (DTZ5)
  - TIFPA Trento
  - INFN Torino (DTZ5)

FELs and synchrotron light sources

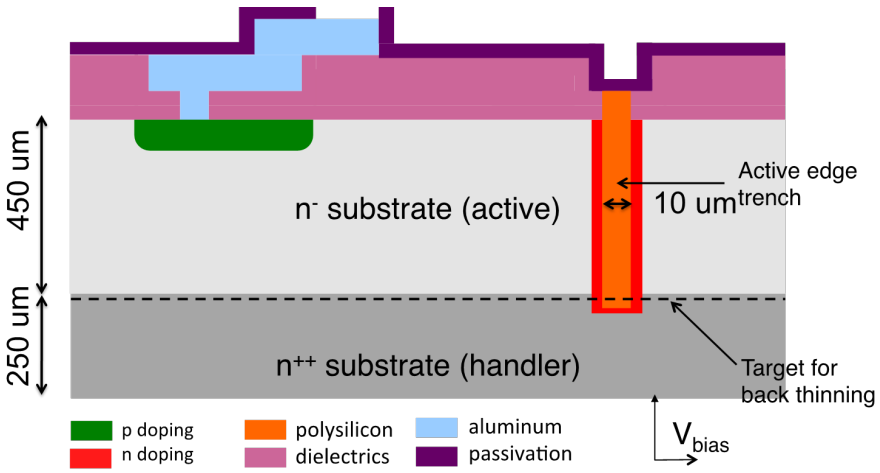
- Powerful tools for exploring the world at the atomic scale and characterizing fast microscopic processes
- Synchrotron light sources
  - widespread, with several experimental beam lines
  - upgrade in progress in many facilities (e.g., ESRF Upgrade Programme)





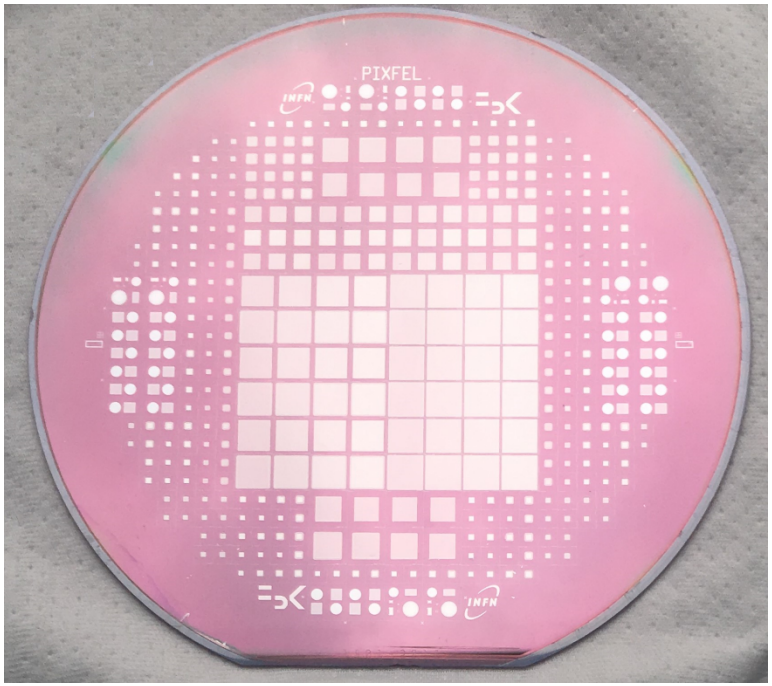
- Free electron lasers
  - increasing in number
  - extremely brilliant beams, orders of magnitude more brilliant than at synchrotron light sources
  - very short pulses, down to femtosecond duration

Starting point: the PixFEL project



Active-edge sensor production run fabricated at FBK on 450+250 um SiSi DWB, 6" wafers. Structures included:

- Diodes and strips
- Arrays
- Test structures for process characterization



Starting point: the PixFEL project

charge preamplifier

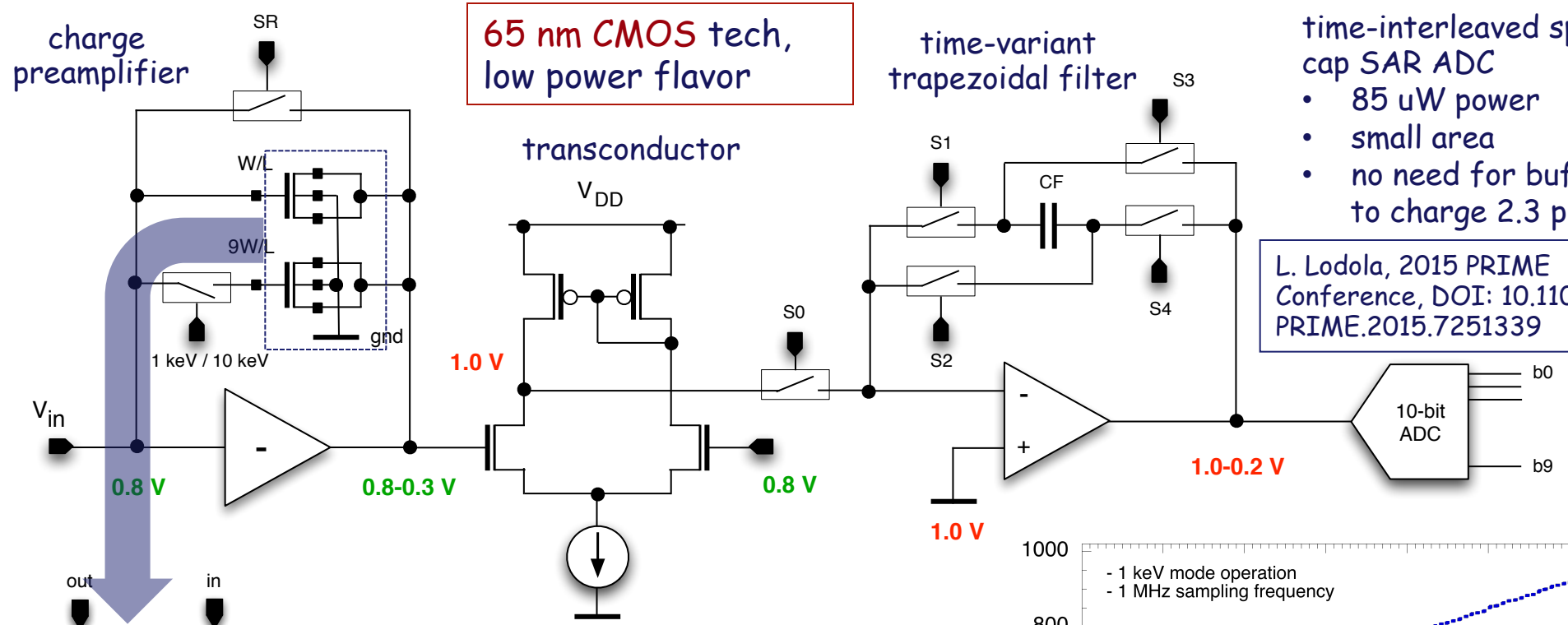
65 nm CMOS tech, low power flavor

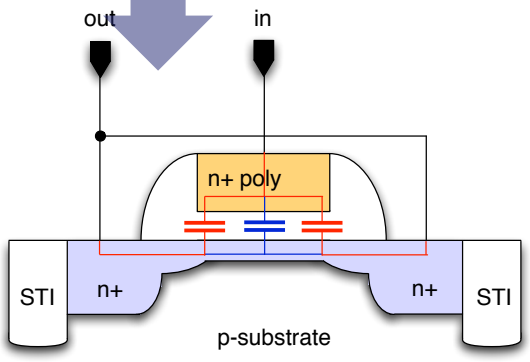
transconductor

time-variant trapezoidal filter

time-interleaved split-cap SAR ADC
- 85 uW power
- small area
- no need for buffer to charge 2.3 pF

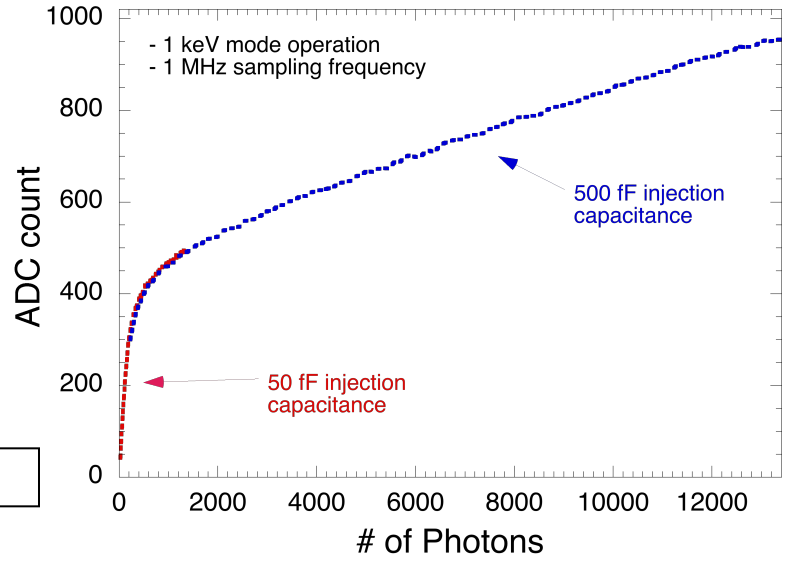
L. Lodola, 2015 PRIME Conference, DOI: 10.1109/PRIME.2015.7251339





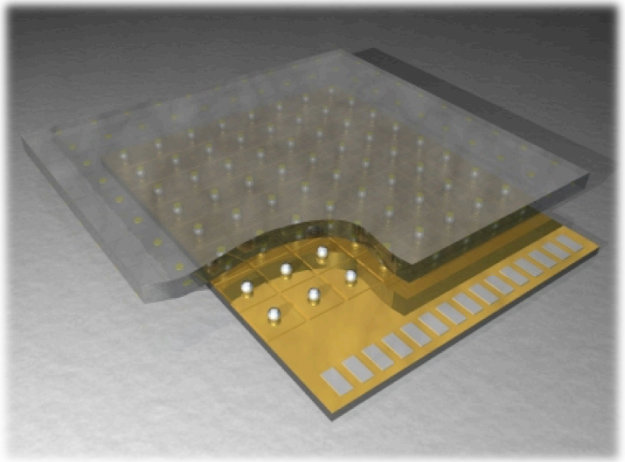
MOS cap in inversion mode for signal dynamic compression

$$\int_0^{Q_{in}} dq = Q_{in} = \int_0^{V_{out}} C(v)\,dv$$



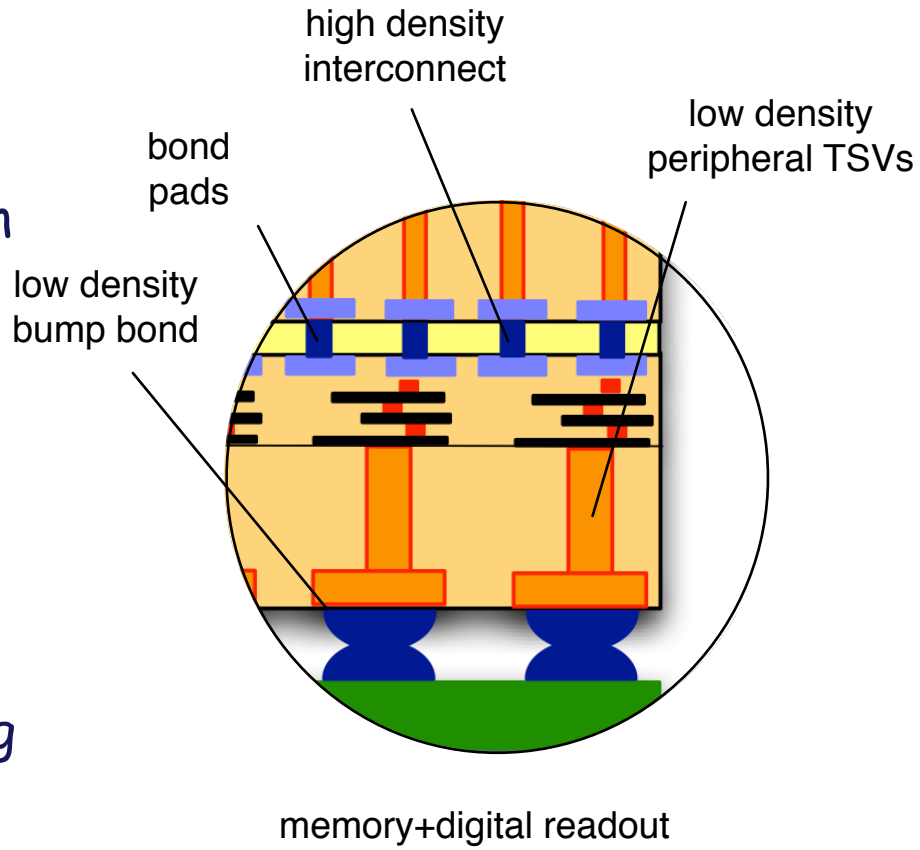
M. Manghisoni et al., IEEE TNS vol. 62, no. 5, pp. 2318-2326, Oct 2015

Activity in progress



- 10 chips + sensors to be bump bonded by IZM

- Working on the design of a new version of the 32x32 channel array for post-processing with peripheral TSVs (wafers needed)
  - participation in an engineering run organized by RD53 and MPA groups at CERN
  - wafers available for post-processing



Summary of the proposed activity

MONOLITHIC PIXEL

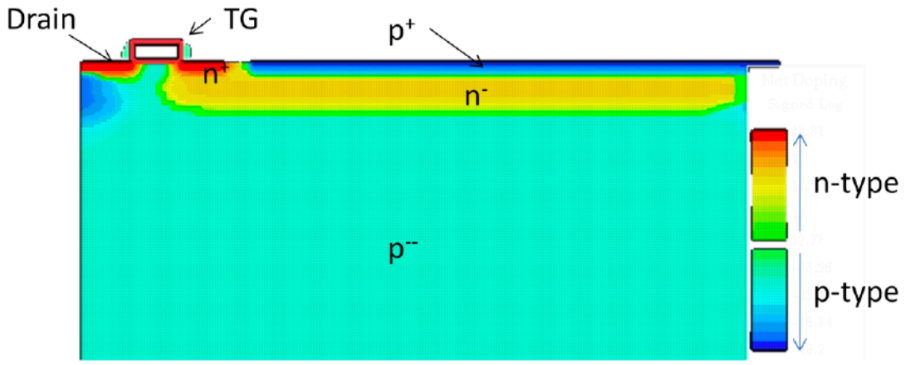
- Develop a detector based on monolithic technologies with high resistivity substrate (suitable for full depletion)
  - faster charge collection and more efficient detection as compared to present monolithic detectors at FEL
  - cheaper solution

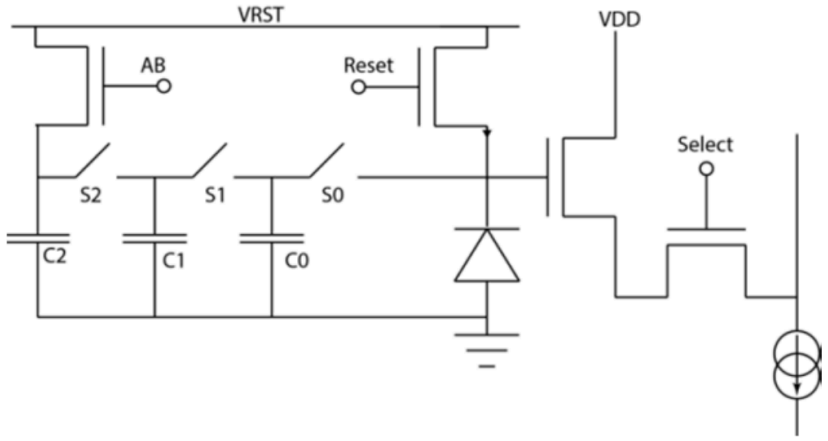
HYBRID AND MONOLITHIC PIXEL

- Develop second tier for memory and digital readout
  - 65 nm CMOS, compatible with both hybrid (PixFEL) and monolithic solutions
- Vertical integration
- Peripheral through silicon vias towards buttability

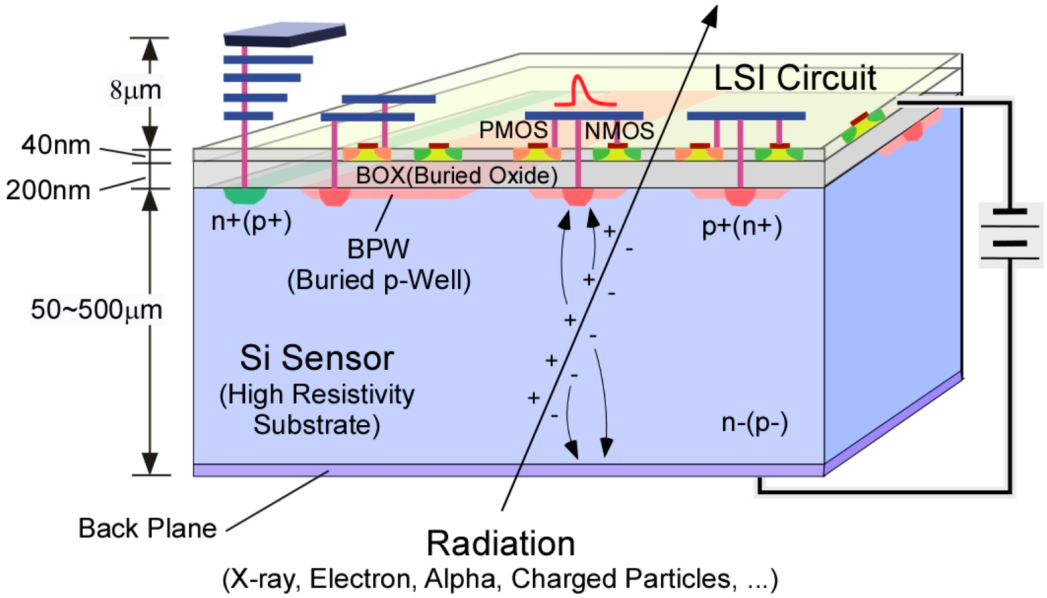
Summary of the proposed activity

- CMOS with HR epi-layer
  - max energy limited to a few keV





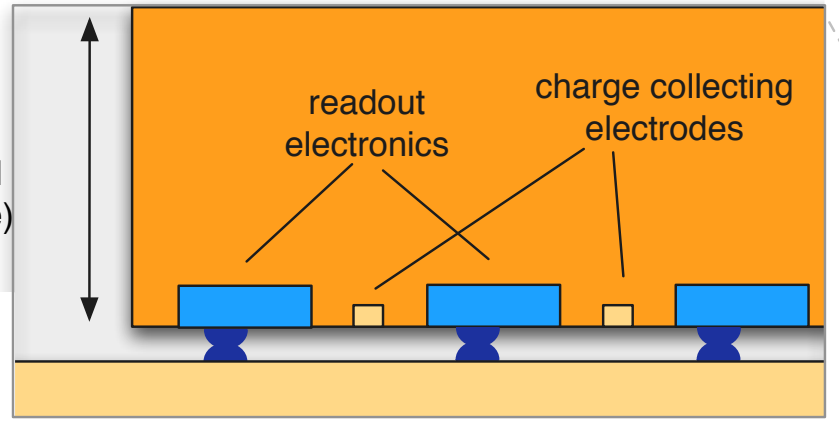
- SOI + HR support wafer

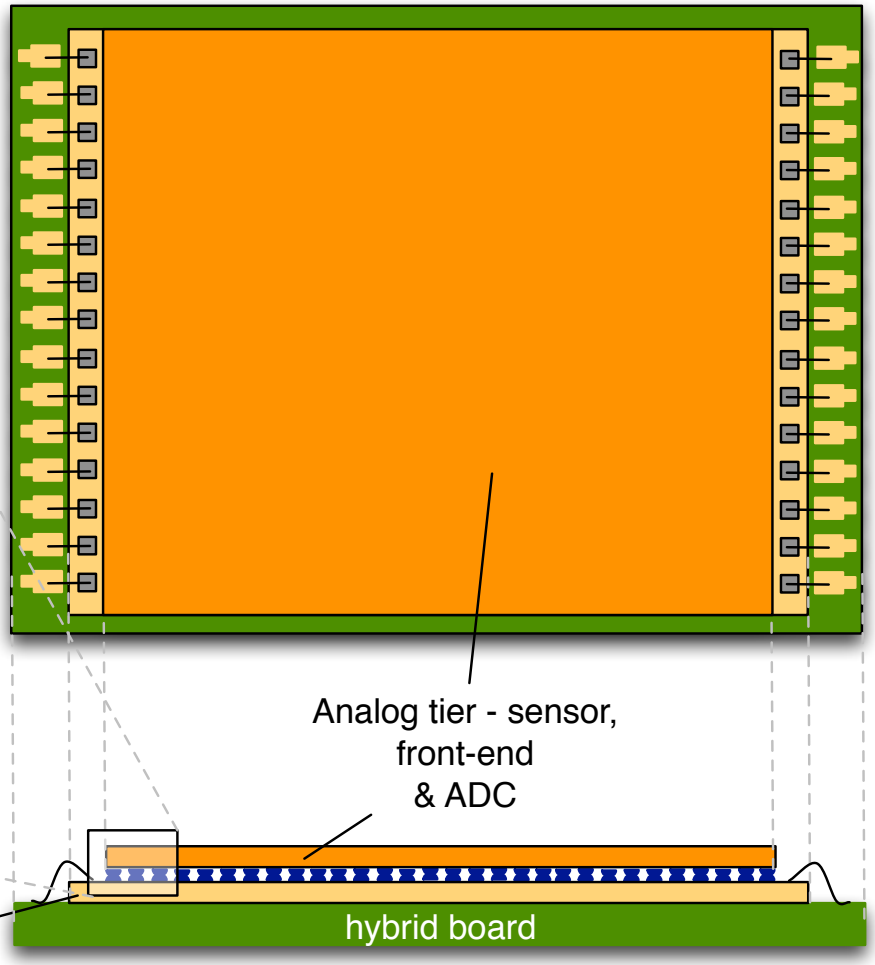


- In general:
  - low noise
  - small pitch
  - slow readout (ADCs serving large chip regions) → limited frame rate

Monolithic sensor demonstrator

- Two-tier detector
  - analog layer – sensor, front-end and ADC
  - digital layer – memory and fast readout





- Low noise + high frame readout rate
- Small pitch bump bonding with IZM
- Development required on sensor (trenches for slim edge design, backside processing for low energy photons)

Activity plan

- First year
  - investigation on technologies for monolithic sensors (towerjazz, XFAB, LFoundry, ESPROS – SEED experiment is successfully developing a fully depleted monolithic sensor in 110 nm CMOS technology by LFoundry)
  - design and simulation of analog front-end for monolithic sensor, TCAD simulations on sensor (taking into account the final test on a synchrotron source beam)
  - production of a test chip for monolithic process characterization from the standpoint of the sensor
  - characterization of chips from the engineering run and hybrid sensor (pixel detector in fully depleted technology connected to front-end chip – from PixFEL), including radiation hardness tests

Activity plan

- Second year
  - monolithic sensor fabrication
  - digital layer fabrication
  - exploration of peripheral TSV options (LFoundry is developing a proprietary TSV process)
  - prototype characterization (including radiation tolerance tests)

- Third year
  - interconnection of monolithic sensor layer with the digital layer
  - characterization of the two-tier demonstrator
  - test of the demonstrator at a synchrotron light source experiment

Workpackages

- WP1 – Sensors (simulation, design and characterization of monolithic and pixel sensors) - TIFPA
- WP2 – Analog front-end (simulation and design of analog front-end for monolithic pixels) – INFN Pavia
- WP3 – Memories, digital readout and chip integration (simulation and design of the digital layer) – INFN Torino
- WP4 – Testing (prototype characterization, including experiment on X-ray beam) – INFN Pavia

Involved people and groups

- TIFPA: L. Pancheri (resp. loc.) et al., 2 FTE
- INFN PISA: F. Morsani, 0.3 FTE
- INFN Torino: L. Demaria, ~0.7 FTE
- INFN Pavia

Name	Position	Committment
Alessandro Cabrini	RTDB	20%
Paolo Ghigna	PA	30%
Marco Grassi	Assegnista	20%
Piero Malcovati	PA	20%
Massimo Manghisoni (resp. loc.)	PA	20%
Stefano Noli	Ph.D	40%
Lodovico Ratti (resp. naz.)	PA	40%
Valerio Re	PO	10%
Gianluca Traversi	PA	20%
Carla Vacchi	RU	20%
FULL TIME EQUIVALENT		2.4

Three-year budget - Overall

	2018		2019		2020	
Travels	CSN5 meetings	**1 kEuro**	CSN5 meetings	**1 kEuro**	CSN5 meetings	**1 kEuro**
	Joint tests	**4 kEuro**	Joint activity on design	**2 kEuro**	Joint tests	**4 kEuro**
	Contacts with the foundry	**2 kEuro**	Contacts with the foundry	**2 kEuro**	Test beam at ESRF	**4 kEuro**
Consumables	Laboratory material	**10 kEuro**	Analog layer, including sensor (LFoundry 110 nm, 12 mm^2)	**20 kEuro**	Laboratory material	**10 kEuro**
	Test structures (LFoundry 110 nm, 10 mm^2)	**12 kEuro**	Substrates, process tuning (LFoundry)	**50 kEuro**	Bonding with IZM	**30 kEuro**
			Digital layer (CMOS 65 nm, 12 mm^2)	**50 kEuro**		
			Laboratory material	**10 kEuro**		
Investments		**0**		**0**		**0**
	Total	**29 kEuro**	**Total**	**135 kEuro**	**Total**	**49 kEuro**

Three-year budget - Pavia

	2018		2019		2020	
Travels	CSN5 meetings	**1 kEuro**	CSN5 meetings	**1 kEuro**	CSN5 meetings	**1 kEuro**
	Joint tests	**2 kEuro**	Joint activity on design	**1 kEuro**	Joint tests	**2 kEuro**
	Contacts with the foundry	**1 kEuro**	Contacts with the foundry	**1 kEuro**	Test beam at ESRF	**4 kEuro**
Consumables	Laboratory material	**3 kEuro**	Digital layer (CMOS 65 nm, 12 mm^2)	**50 kEuro**	Laboratory material	**3 kEuro**
	Test structures (LFoundry 110 nm, 10 mm^2)	**12 kEuro**	Laboratory material	**3 kEuro**		
Investments		**0**		**0**		**0**
	Total	**16 kEuro**	**Total**	**56 kEuro**	**Total**	**9 kEuro**