ASAP

Array of Silicon Avalanche Pixels

Programma di attività e preventivo di spesa 2018

Sezione di Pavia

Resp. Naz.: Pier Simone Marrocchesi (PI)

Resp. Loc.: Lodovico Ratti

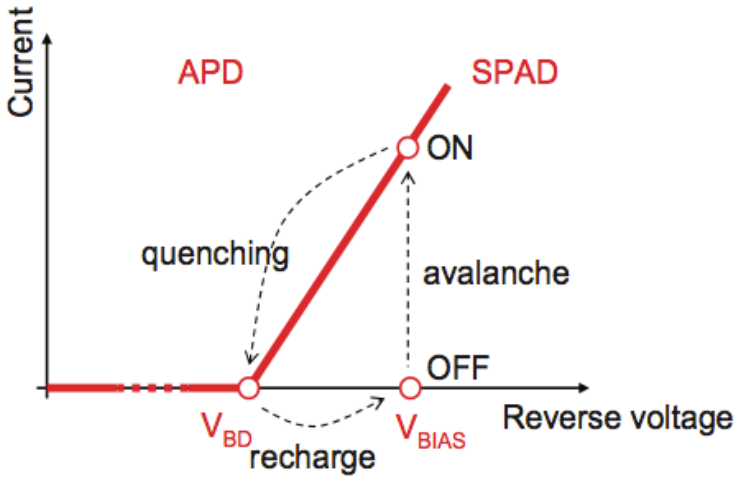
INFN Pavia, Consiglio di Sezione, 6 luglio 2017

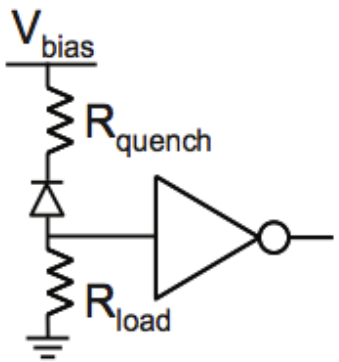
ASAP project

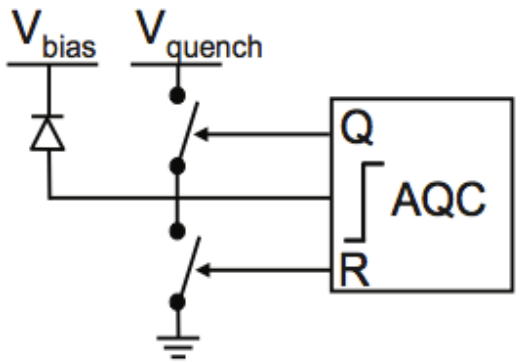
- Goal of the project: develop a new generation of layered avalanche detectors for charged particles (also in medical applications) leveraging process scaling, thinning technologies, process tailoring and through silicon vias for improved efficiency, reduced DCR and buttability to cover large areas
- Duration: 3 years
- Participating INFN groups:
  - INFN Pisa (gruppo collegato di Siena)
  - INFN Pavia
  - TIFPA Trento
  - INFN Padova (DTZ5)

SPADs (single photon avalanche photodiodes)

- Avalanche photodiodes are p-n junction purposely made to operate at high electric fields in order to achieve an internal gain
- A charge carrier accelerated by the field in the depleted region can reach an energy high enough to break a bond when colliding with lattice atoms, thus generating a new e-h pair through impact ionization
- In linear-mode APDs, bias voltage is below breakdown and the generated current is proportional to incident light; in Geiger-mode APDs (or SPADs), the bias voltage exceeds the breakdown voltage, with multiplication factors in the order of 10^6
- To turn the avalanche current off, a proper quenching mechanism has to be used in Geiger-mode APDs







From a single layer to a dual tier SPAD

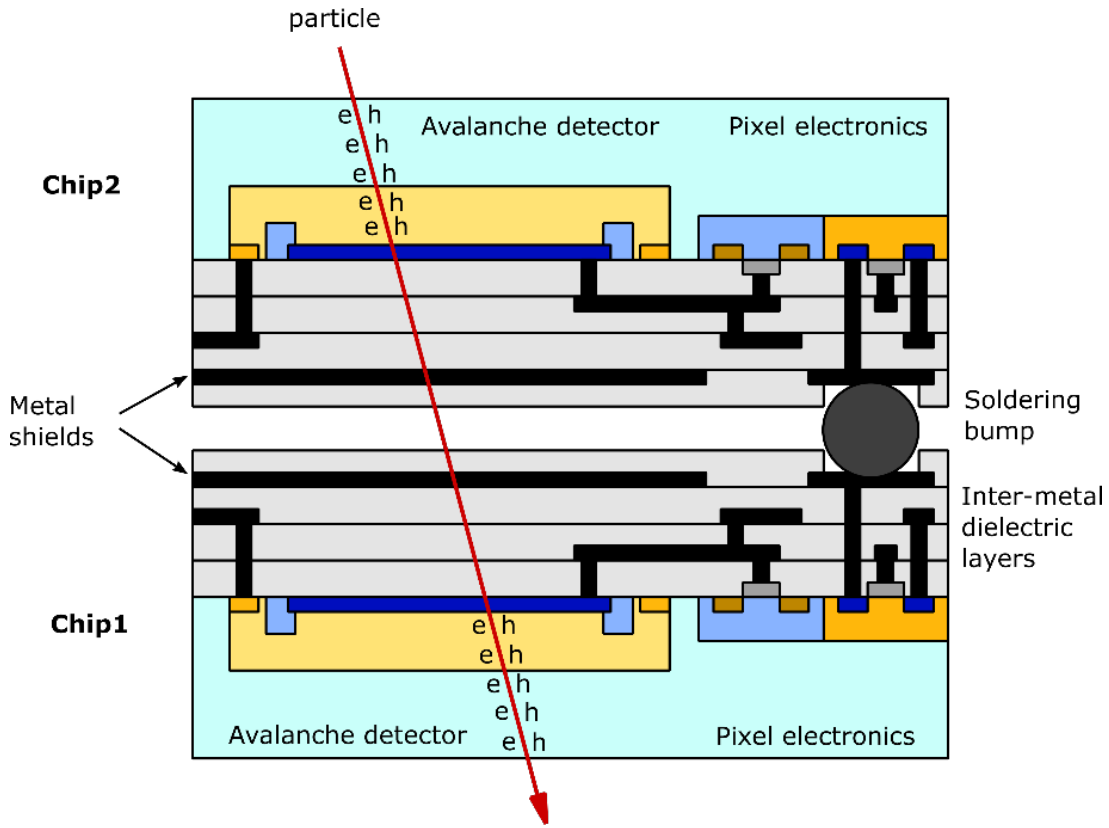
- The basic element of the **ASAP** detector is an avalanche detector, based on a standard CMOS process and operated in the quenched Geiger mode
  - a large, intrinsic gain is provided by the detector itself, with no need for preamplification → less power dissipation
  - no amplitude measurement, pure binary information (hit/no hit)
  - the sensitive layer of the device is very thin, limited to the depleted region around the pn junction → virtually no charge loss if the substrate is thinned down
  - readout electronics in the same substrate as the sensor
- An avalanche detector may feature a dark count rate of the order of 10 MHz/cm^2
- The goal is to improve dark rate performance by using the coincidence signal between two overlapping pixels (sensor pairs)
  - dark count rate per unit area R_A for each tier, an elementary square cell with pitch **p** and a coincidence time Δt the dark count rate per unit area for a n-tier detector is

$$n \times R_a^n \times p^2 \times \Delta t^{n-1}$$

  - for R_A=10 MHz/cm^2, Δt=1 ns and p=50 μm, the dark count rate for single cell a dual-tier detector (n=2) is 5 Hz

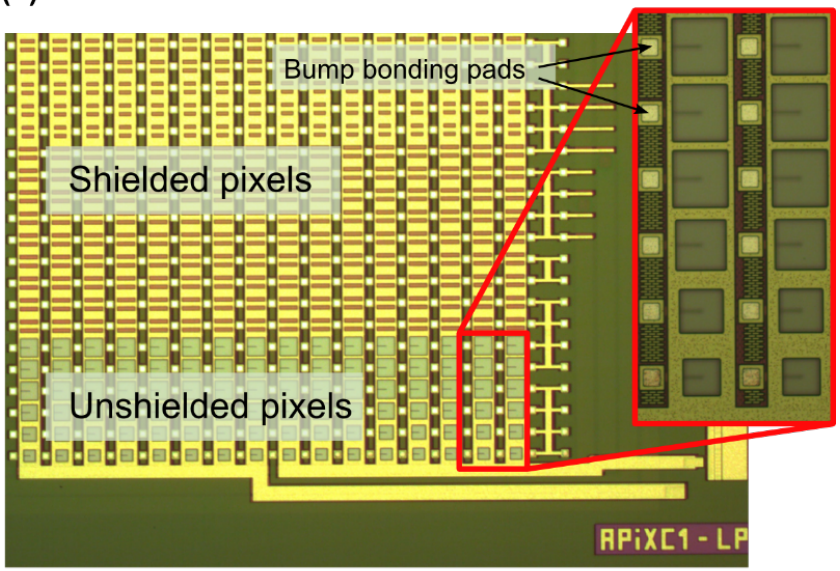
Starting point: the APiX2 detector

- Coincidence pixel composed of two layers (LFoundry 150 nm CMOS) of detectors and electronics, with vertical interconnection to deliver the digitized signal from top to bottom
  - small prototype tested, design of a larger array ready by the end of July

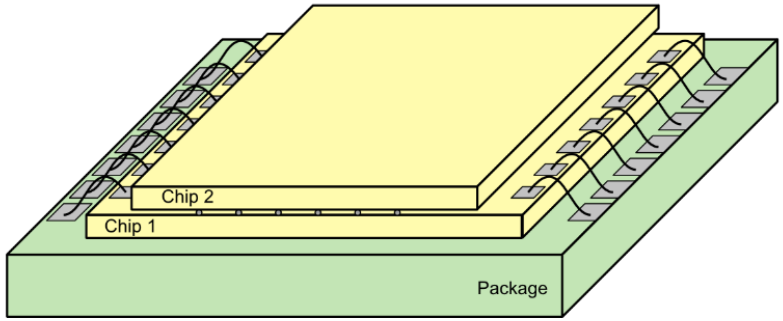


Starting point: the APiX2 detector

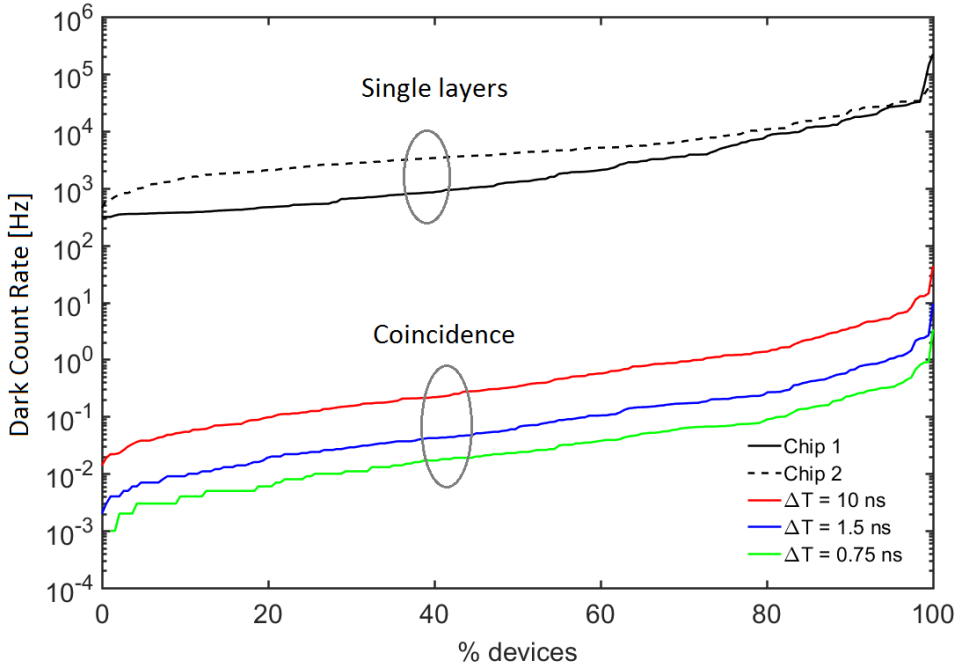
(a)



(b)



- Two interconnected layers of avalanche detectors in LFoundry 150 nm technology
- DCR reduction as expected from theoretical considerations

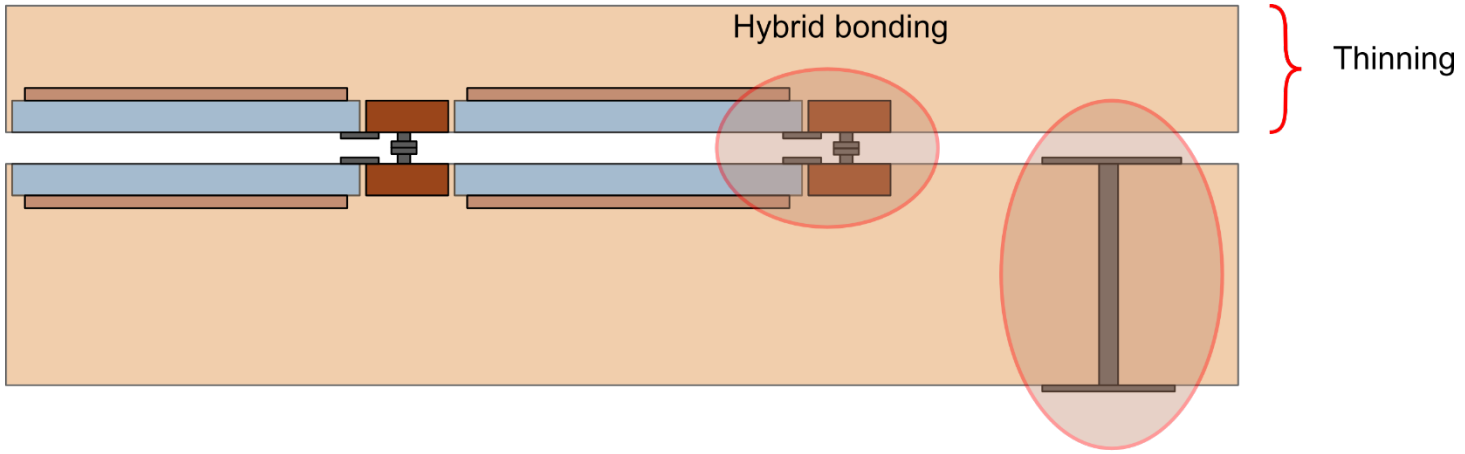


ASAP: a new generation of layered avalanche detectors

- Strategies to improve **efficiency**
  - Process scaling: improved geometrical Fill-Factor
  - Thinning: improved efficiency for low-energy particles
- **Dark count** reduction
  - Reduce DCR of single layer: process tailoring (dedicated implantations)
  - Reduced contaminations (imaging process)
- **Large area**
  - Through-Silicon Vias: buttable modules

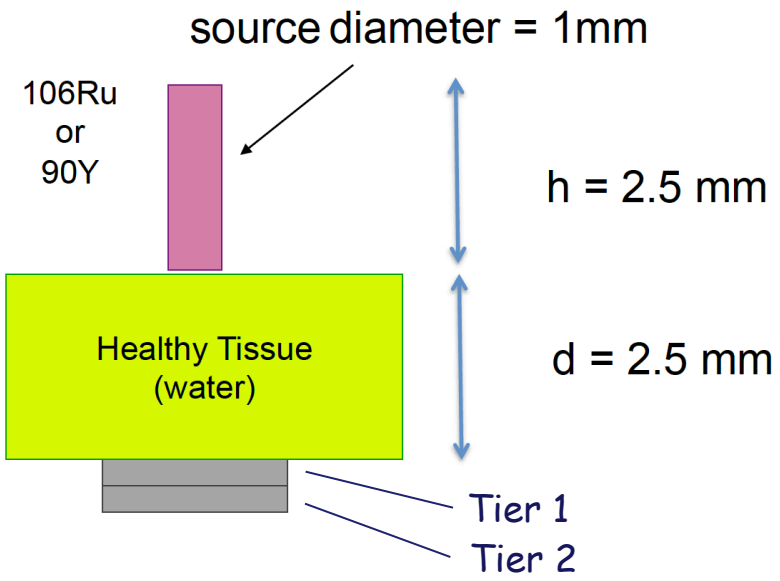
Innovation in process technology

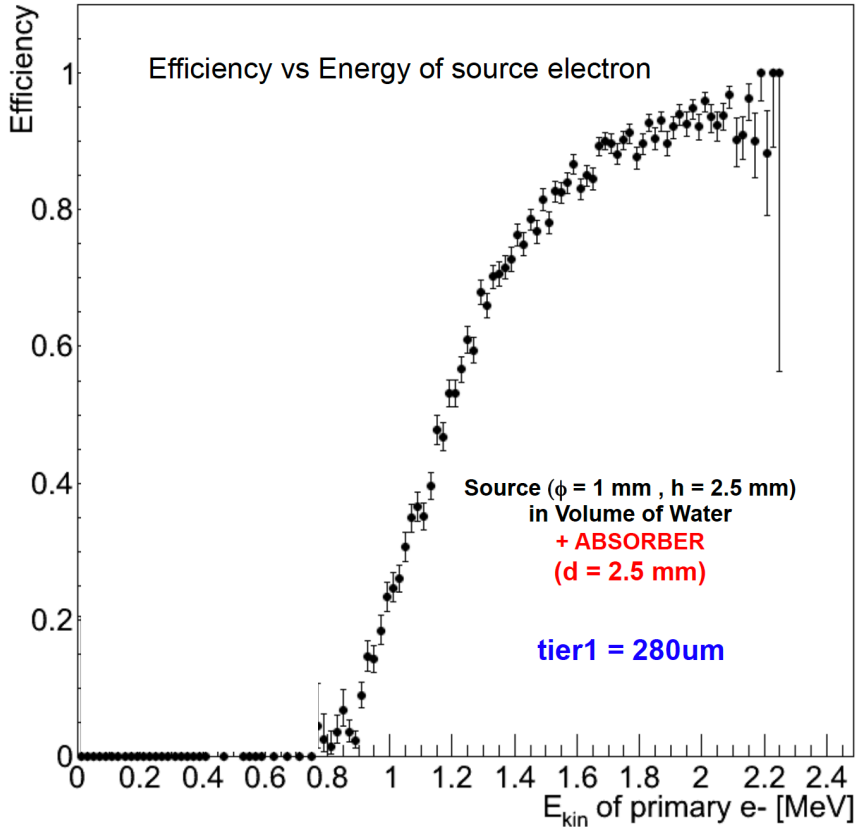
- **Scaled process:** 110 nm (advantages in efficiency, speed and power consumption)
- **Vertical integration** obtained with **hybrid bonding** and handled internally by LFoundry at the wafer level → advantages in terms of cost and yield
- **Thinning** down to a thickness lower than **10um**
- **Perypheral TSVs**



Imaging intraoperative probe

- Take advantage of the high sensitivity and low noise of a layered avalanche detector to design a compact imaging probe for radio-guided surgery with β emitters
- Some simulations have already been performed





- Efficiency also increases as tier 1 thickness decreases

Work plan for 2018

- Design of test structures in LFoundry 110 nm CMOS technology
  - contribution mostly focused on the design of front-end, in-pixel electronics and readout electronics
  - passive and active quenching structures
  - fill factor maximization
  - timing optimization (in view of possible applications for time of flights measurements)
- Test structure characterization

Involved people and groups

- INFN Siena (PI): P.S. Marrocchesi (resp. naz.) et al., ~6 FTE
- TIFPA Trento: L. Pancheri (resp. loc.) G.-F. Dalla Betta et al., ~2 FTE
- INFN Padova: G. Collazuol, ~0.5 FTE
- INFN Pavia

Name	Position	Committment
Marco Musacci	Ph.D	**70%**
Stefano Noli	Ph.D	**60%**
Lodovico Ratti (resp. loc.)	PA	**30%**
Carla Vacchi	RU	**40%**
FULL TIME EQUIVALENT		**2.0**

Budget requests for 2018

Travels	Collaboration meetings	**1.0 kEuro**
	Electrical and electro-optical tests in laboratories of other members of the collaboration	**2.0 kEuro**
Consumables	Test structures in LFoundry 110 nm CMOS technology (12 mm^2)	20 kEuro
	Process development (e.g., dedicated implants for breakdown voltage adjustment)	40 kEuro
	Material for prototype testing	**5 kEuro**
	TOTALE	**68 kEuro**