PIXELS & SHORT STRIPS

SOME THOUGHTS AFTER A PRELIMINARY ANALYSIS…

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CEPC-SppC Study Group Meeting
Beihang University, Beijing, Sept. 2-3, 2016

updated for the

"Future Accelerator" group meeting
Bologna
July 3-4, 2017

Outline:

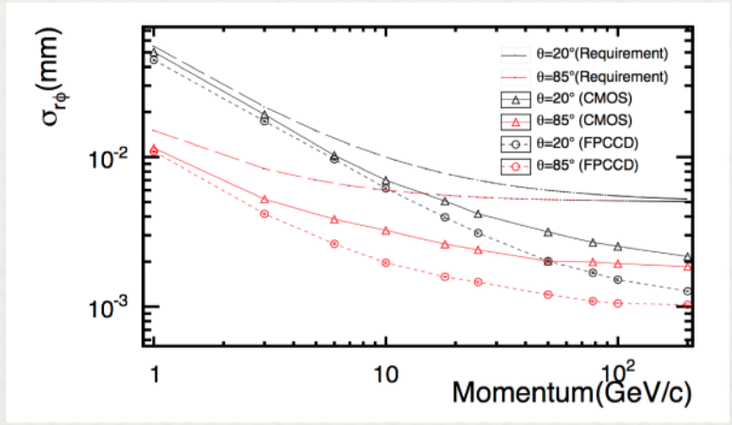
- Boundary Conditions & System Aspects
- Technology
- Architecture
- What's Up in China
- Conclusions

Boundary Conditions & System Aspects

☑ Physics First!

impact parameter resolution

$$\sigma_{ip} = a \oplus \frac{b}{p \cdot \sin^{3/2}\theta}$$



ILD DBD 2012

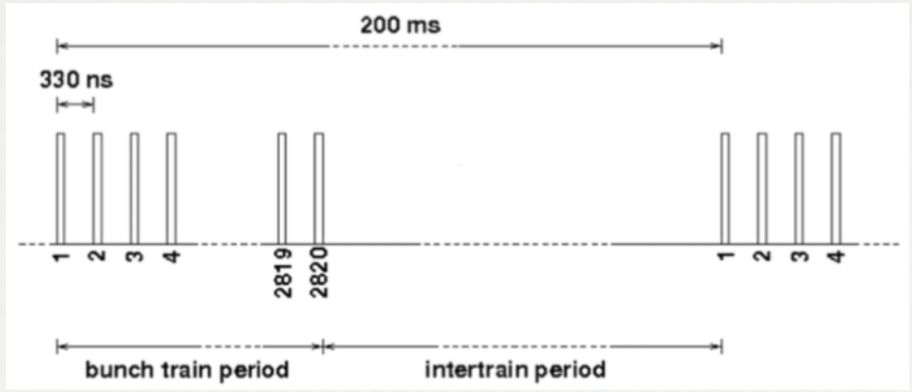
Accelerator	a [μm]	b [μm·GeV/c]
LEP	25	70
SLC	8	33
LHC	12	70
RHIC-II	13	19
ILC	< 5	< 10

ILD LOI 2009

- a depends on the single point resolution and the ratio between the innermost radius and the lever arm:
  => σ_{sp} = 3 μm when R_{in} =16 mm and R_{out} = 60 mm [The ILD and CePC figures]
- b depends on the multiple scattering at the innermost radius:
  => thickness/layer = 0.15% X_0 [X_0 = 9.37 cm for Silicon] [140 μm]

☑ The machine comes next:

what is the time structure of the beams?



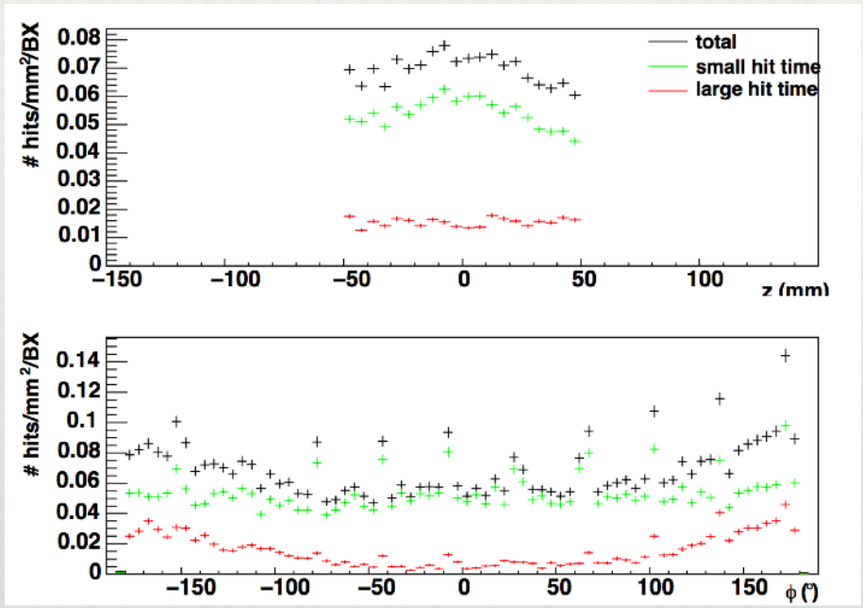
at the ILC, it may look weird but it is very practical since the low duty cycle allows:

- to consider a Power Pulsing scheme
- a relaxed evacuation of time stamped data during the inter-train

What is the expected Beamstrahlung?

hit rate in the first layer of the ILD-VD

occupancy ~10^{-2} /50 μs



DeMasi, Winter, ArXiv: 0902.2707v1

It has an impact on:

- the granularity and the technology (affecting the cluster size)
- Time stamping
- read-out speed ⇢ architecture & power consumption

☑ The machine comes next:

what is the time structure of the beams?

at the CepC, collisions are equally spaced (in time) with a frequency depending on the number of bunches. In one of the configurations reported in Beijing-201609, we have:

- 50 bunches at the Higgs factory energy
- 5000 bunches at the Z factory energy [where I estimated 4 kHz event rate]

for a beam Xing every 5 μs (@Hlggs) to 50 ns (@Zpole) [3.6 μs is the "official" number]

What is the expected Beam-induced background?

there is actually NO solid rock number and estimates have a significant dependence on the machine & final focus parameters (HongBo, June 107).

A rough figure says ≈ 50 hits/cm^2/Xing (I believe @Hlggs energies)

BUT:

- having the spectrum of the bckg particles in important to see if I have "loopers"
- we have to see how it scales with the energy

and what about the expected radiation levels?

Table 1
Comparison of the requirements of various vertex detectors, in terms of read-out speed (σ_t) and radiation tolerance related to the total ionizing dose (TID) and non-ionizing particle fluence.

Experiment-system	σ_t (μs)	TID (MRad)	Fluence (n_{eq}/cm^2)
STAR-PXL	$\lesssim$200	0.150	3×10^{12}
ALICE-ITS	10–30	0.700	10^{13}
CBM-MVD	10–30	$\lesssim$10	$\lesssim 10^{14}$
ILD-VXD	$\lesssim$10	$\mathcal{O}(0.1)$	$\mathcal{O}(10^{11})$
Super B factories	$\lesssim$20	5/yr	5×10^{12}/yr

Here we can possibly relax..
estimated figures do not go beyond 1 Mrad/year

Baudot et al., NIM A732 (2013) 480

☑ Last but not least, the overall detector design:

- is the VD part of a full Silicon Tracker?
- is the experiment running trigger less? [certainly not at the Z pole]

Technology

- epi- less technologies (AMS 350 nm)
- low resistivity epitaxial layer, bulk (large catalogue)
- low resistivity epitaxial layer, OPTO tech (AMS 350 nm)
- low resistivity epitaxial layer, 3 wells (e.g. STm 130 nm)
- low resistivity epitaxial layer, 4 wells (e.g. INMAPS)
- **High Resistivity epitaxial layer, 4 wells (e.g. Tower Jazz 180 nm)**
- SOI on High resistivity Substrate (LAPIS, formerly OKI)
- Vertical integration (e.g. Tezzaron)

* low resistivity: ≈ 10 Ω cm, collection by diffusion
* high resistivity > 1 k Ω cm, collection by drift

Technology

- **High Resistivity epitaxial layer, 4 wells (e.g. Tower Jazz 180 nm)**

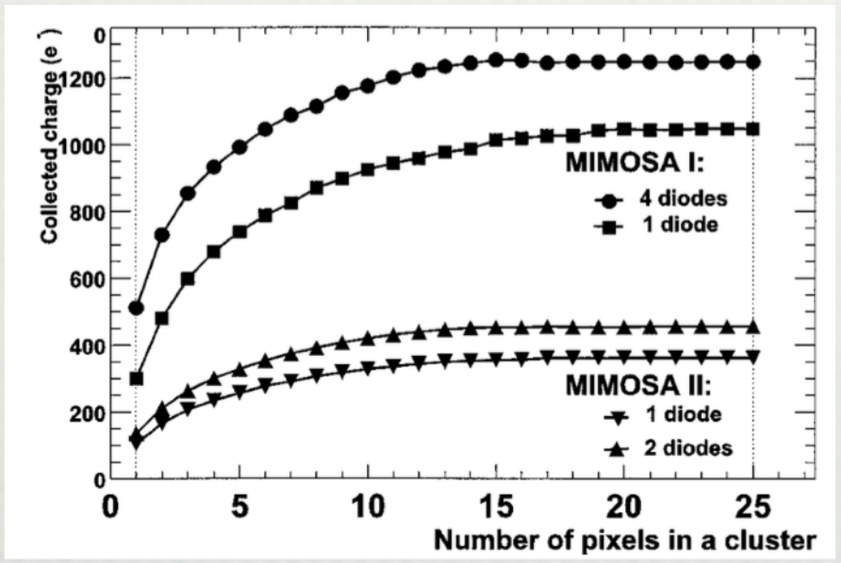
Some of the advantages of this technology:

- 6 metal layers for dense interconnections
- quadruple well
- 18 μm thick epitaxial layer of 1-5 kΩ cm resistivity ⇢ collection by drift

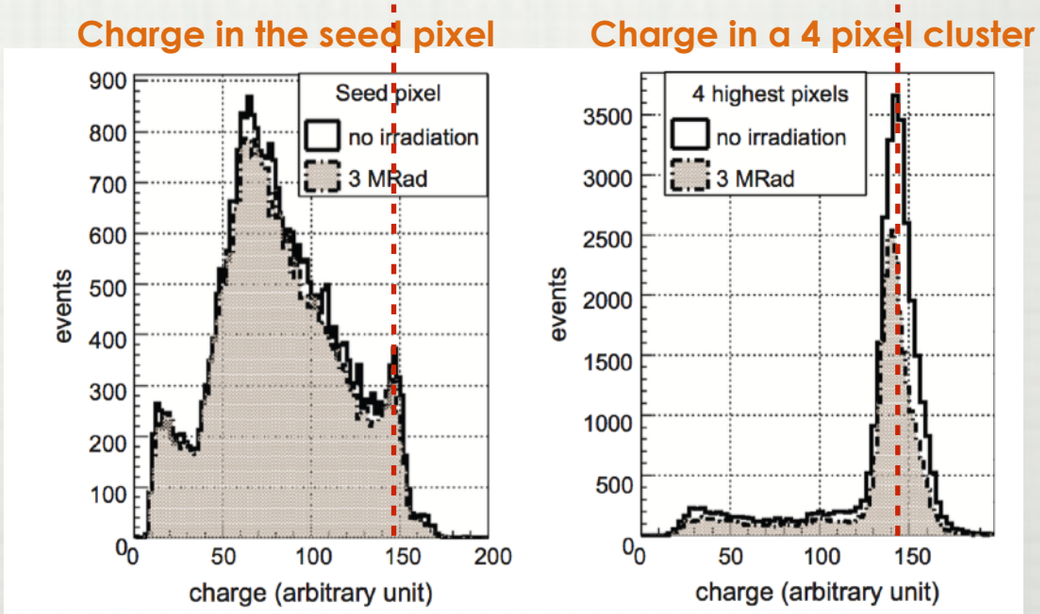
3 good reasons for having high resistivity substrates:

a. smaller charge spread & clustering size

G. Deptuch at al, IEEE-TNS 49 (2002) 601



AMS 0.6 μm technology - 14 μm epitaxial layer - 20 μm pixel pitch

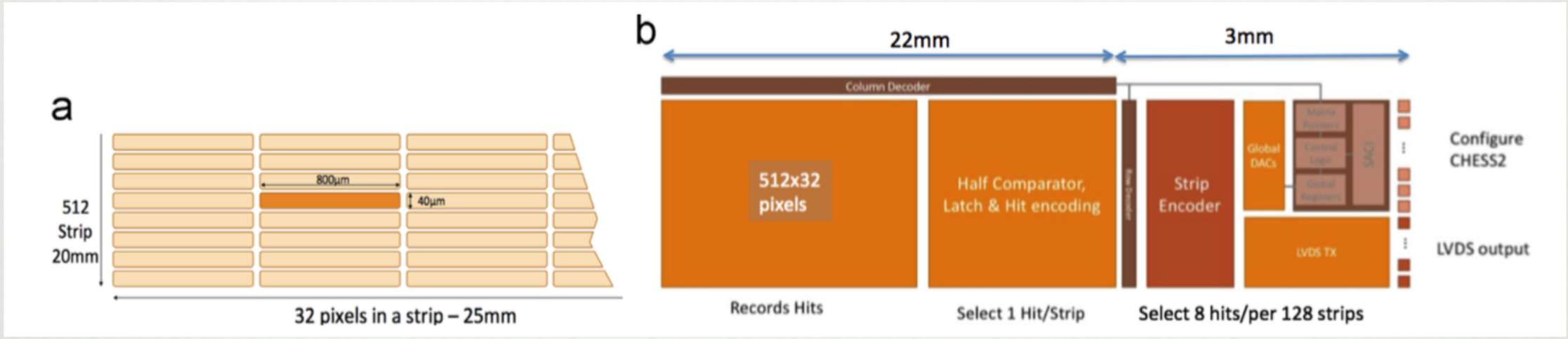


TJ 0.18 μm technology - 18 μm epitaxial layer - 20 μm pixel pitch, illuminated by an 55fe source (5.9 keV X ray, generating 1640 eh pairs

G. Baudot at al, NIM A732 (2013) 480

b.shorter collection time ⇢ reduced trapping probability ⇢ increased radiation tolerance (possibly from 10^{12} n_{eq}/cm^2 to 10^{15} n_{eq}/cm^2 [W. Snoeys, NIM A731 (2013) 125]

c. possibility to design pixels with unusual aspect ratio ⇢ SHORT STRIPS



Z. Liang et al., NIM A (2016) http://dx.doi.org/10.1016/j. nima.2016.05.007

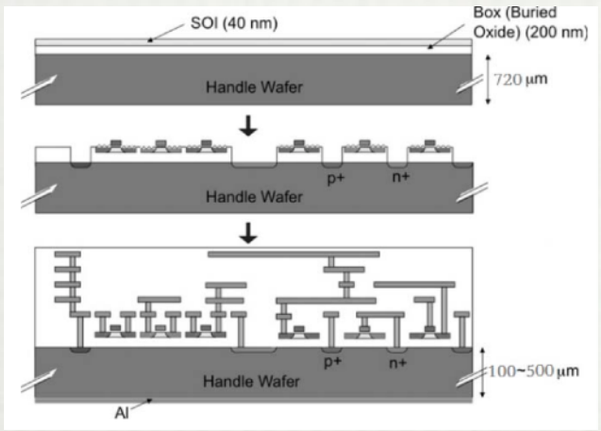
There's a lot of ongoing activity relying on these technologies. Among them, it is worth mentioning:

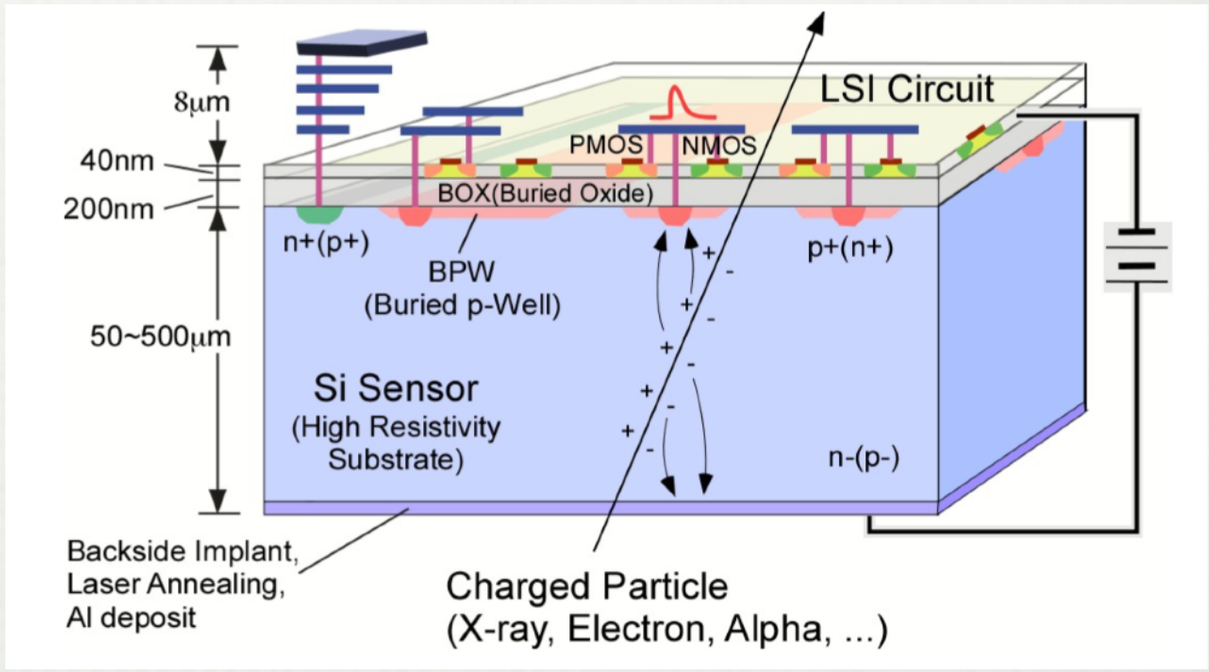
- the papers by Ivan Peric & coworkers (U. Heidelberg), driven by ATLAS
- the activity by A. Andreazza & co. (Uni.Milano) on pixels integrating a first stage amplification capacitively coupled to an LHC compliant RO chip (see poster @IWORID2016 and the oral at the next IEEE-NSS)
- notably the activity on ALPIDE, the sensor for the ALICE ITS system (see below)

Technology

- SOI on High resistivity Substrate (LAPIS, formerly OKI bu TJ seems to be on the track!)
  - H. Lan et al. IEEE sensors journals 15 (2015) 2732 a Review!
  - J. Marczewski, M. Caccia et al., *IEEE Trans. Nucl. Sci.*, 51 (2004)1025
  - M. Jastrzab, M. Caccia et al, NIM A560 (2006) 31

simplified process flow



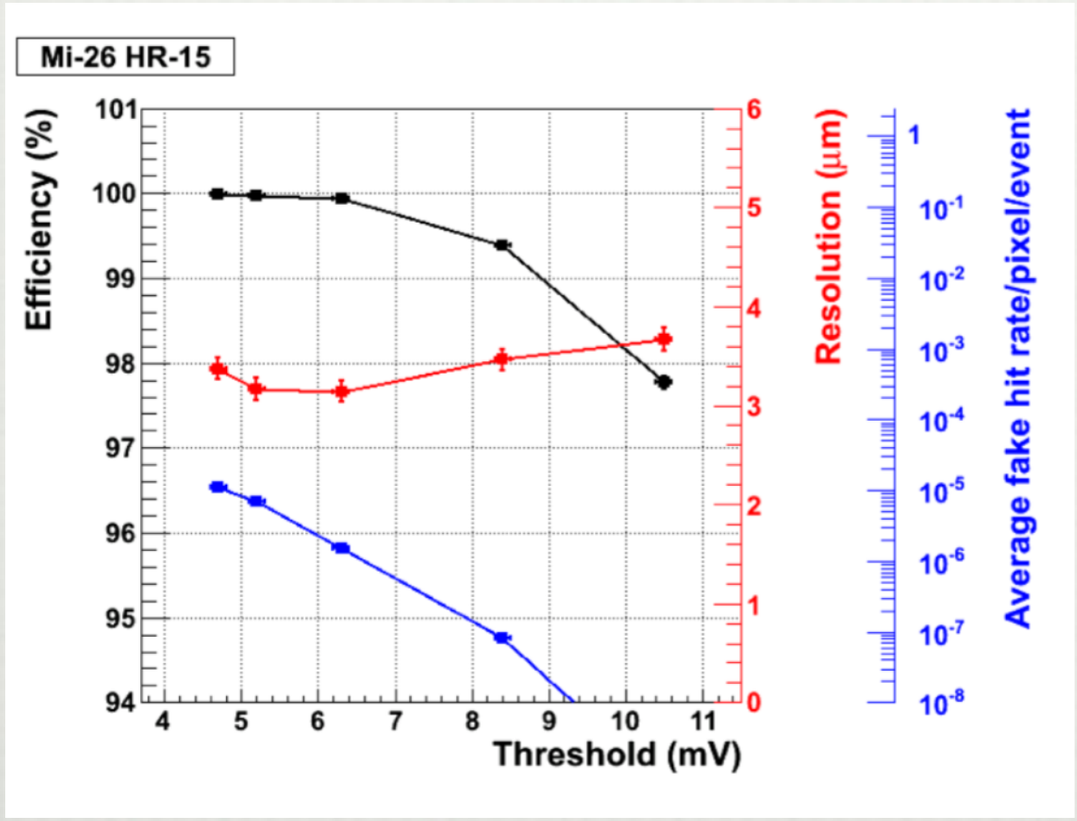


- main advantages:
  - a genuine monolithic approach
  - more flexible wrt CMOS maps (nmos & pmos naturally integrated in the SOI layer)
  - electronics "isolated" from the bulk (fast switching, reduced single event upset) [the motivation for the industrial development of SOI - partially true here]
  - the active layer is a very standard and comfortable high resistivity, fully depleted detector
- main disadvantages:
  - not easy to get SOI wafers on a high resistivity substrate
  - mind the effect of the depletion voltage (back-gate effect)
  - custom process

Architectures

☑ Analog or binary pixels?

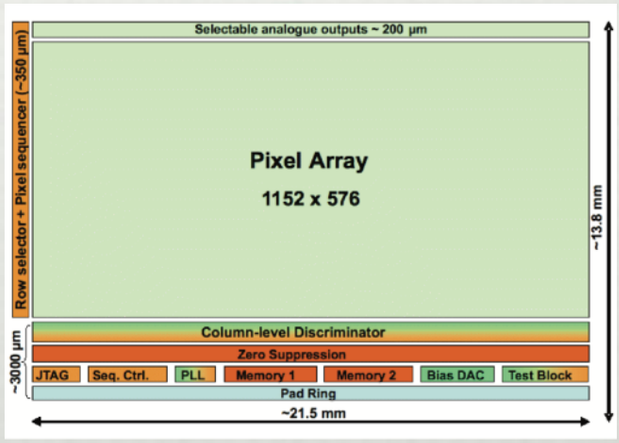
The pitch/√12 rule has been violated in MAPS:



M. Winter et al., arXiv: 1203.3750v1 (2012)

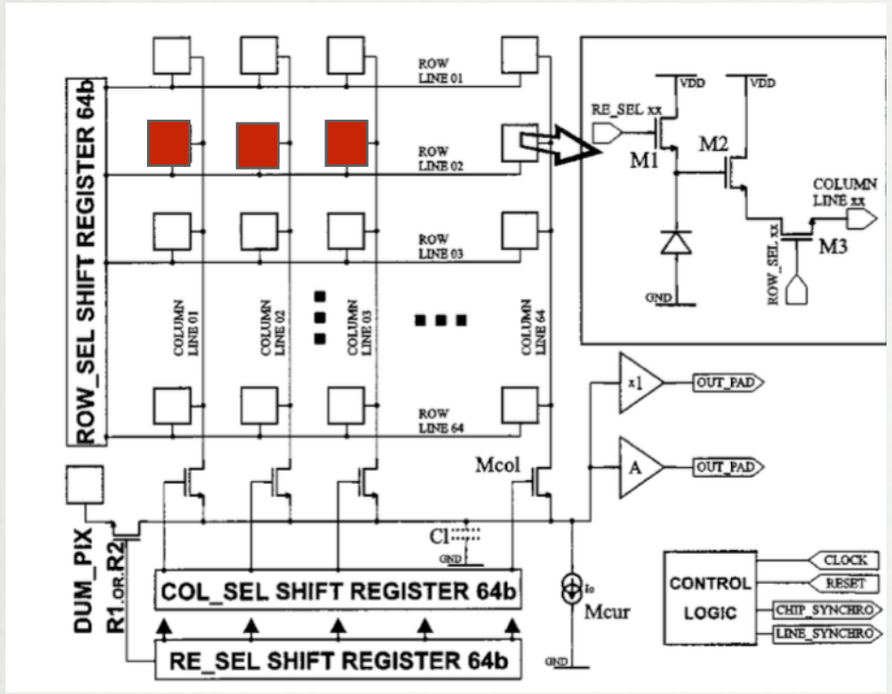
Test beam results for the MIMOSA-26 sensor:

- 18.4 μm pitch (5.3 μm binary resolution)
- rolling shutter & end-of-column zero suppression (200 ns/pixel r.o. time)
- 250 mW/cm^2 power consumption



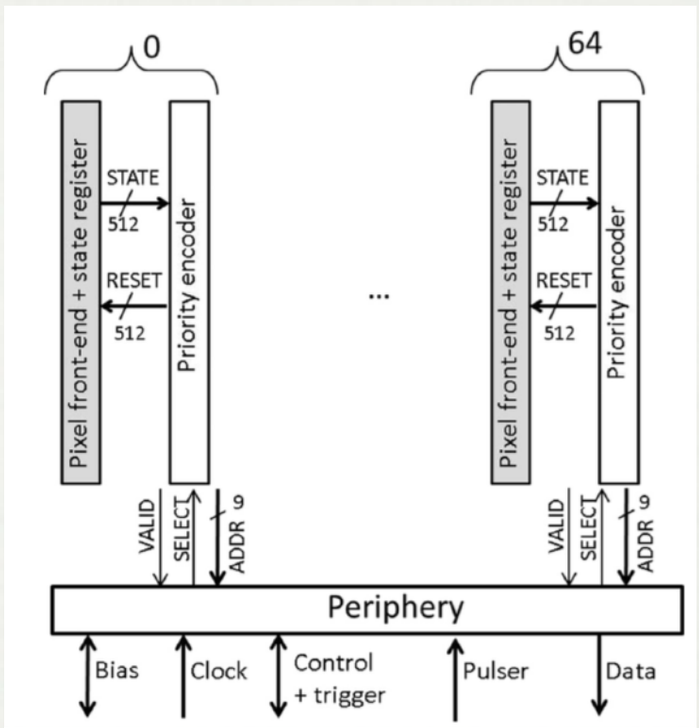
☑ Rolling shutter + end of column zero suppression or on-pixel sparsification?

Rolling Shutter



- 1 discriminator/column
  ⇢ analog info travels to the end-of-column logic
- the integration time is determined by the read-out (r.o.) time
- the r.o. time is independent from the pixel occupancy
- current power consumption at the level of 150 mW/cm^2 (MIMOSA -28)

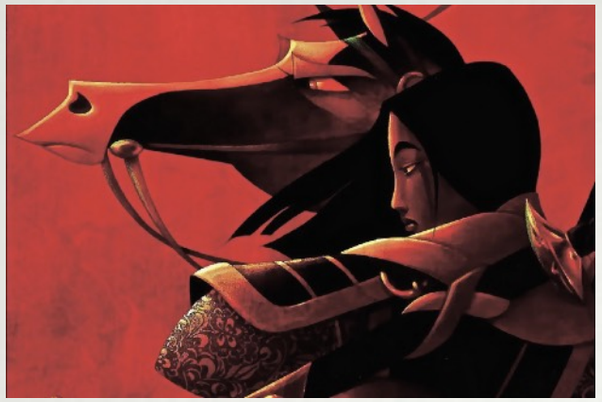
On-pixel sparsification



- 1 discriminator/pixel + 1bit memory cell
  ⇢ analog info locally processed
- the integration time is independent from read-out (r.o.) time
- the r.o. time is dependent from the pixel occupancy
- current power consumption at the level of 50 mW/cm^2 (ALPIDE)

-NIM A 765 (2014) 177 + A 785 (2015) 61
-pixel 2014 proceedings published on JINST
(doi:10.1088/1748-0221/10/03/C03030)

made possible by the quadruple well tech.

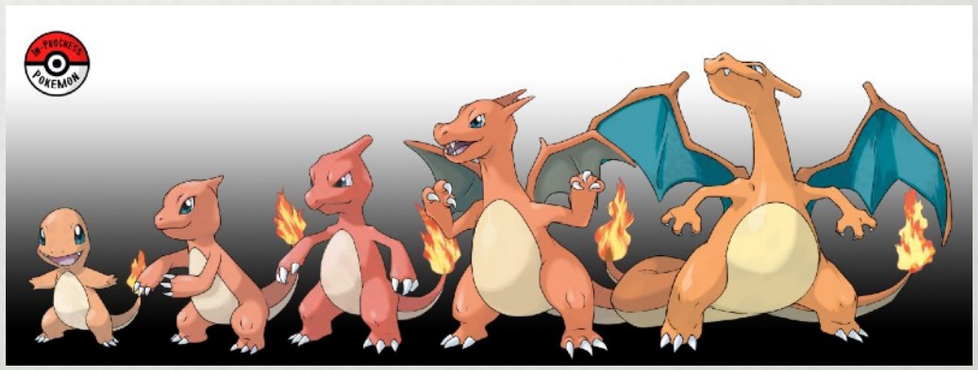


Anything specific on going in China?

excerpt from the HK207 report by Ping Yang, Central China Normal University

- a study of the effect of the epitaxial layer characteristics (technology)
- optimisation of the pixel & pre-amplifier layout ⇒ squeeze the pixel size & gain on the power dissipation by the analog cell
- optimisation of the readout architecture ⇒ decrease the power consumption

Evolutions from the ALPIDE



⇒ Effects of the epitaxial layer characteristics (simulation)

(Y. Zhang et al., NIM A831 (2016) 99-104)

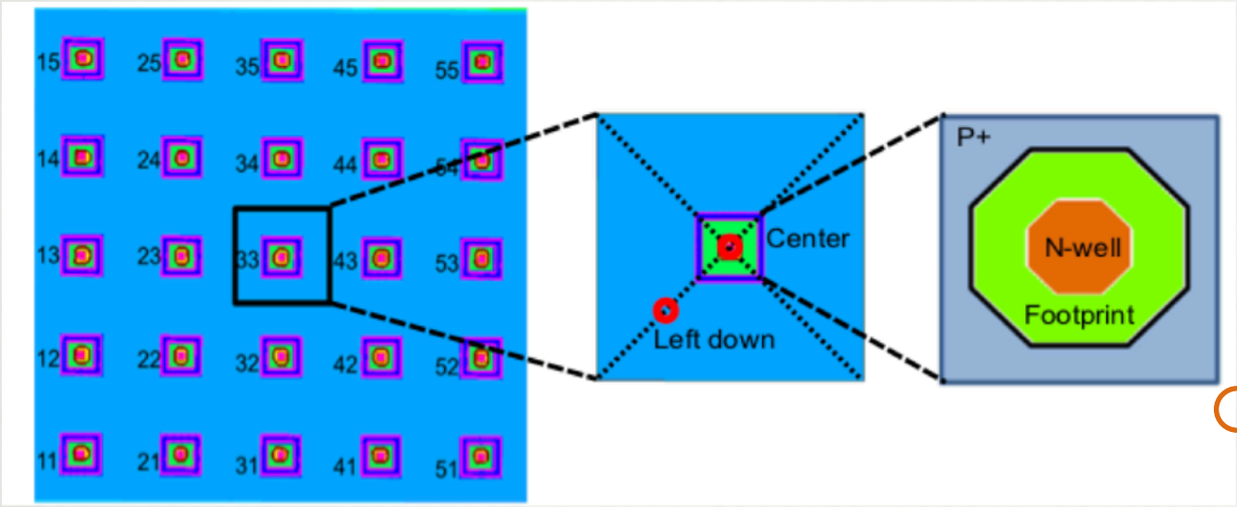
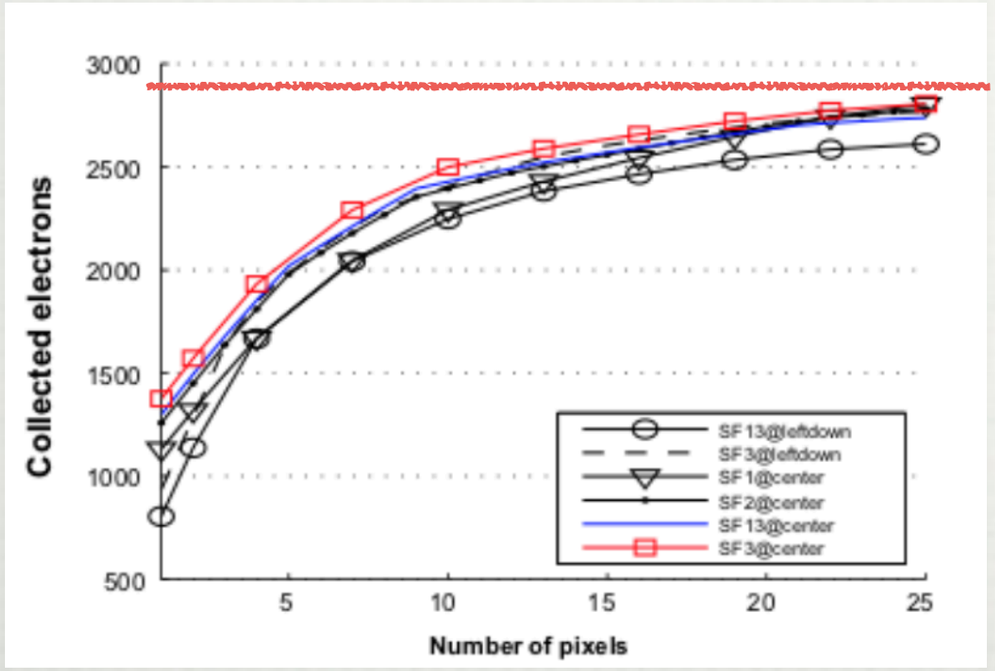


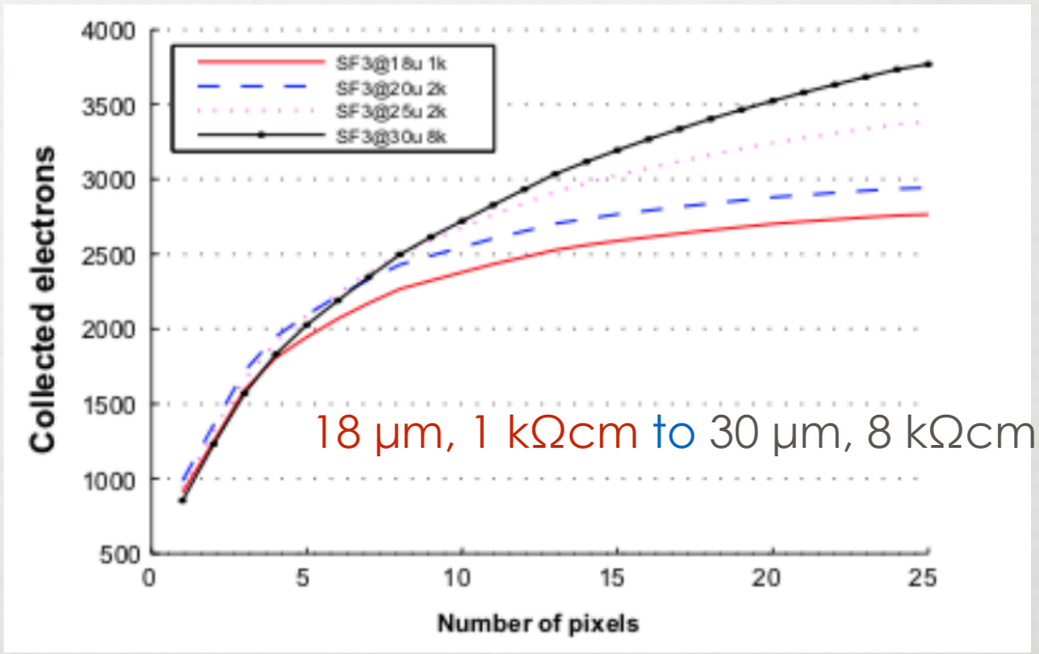
Table 1
Diode geometries implemented in simulation.

Structure	N-well (μm^2)	Footprint (μm^2)	C_{in} (fF)	Circuits
SF1	3	20	4.5	NMOS
SF2	4	20	5.1	NMOS
SF3	8	20	6.8	NMOS
SF13	8	20	6.8	PMOS



the asymptotic value seems to exceed the 1440 e-h paris expected in 18 µm ⇒ possible contribution from the charges diffusing on from the substrate

SF3 design

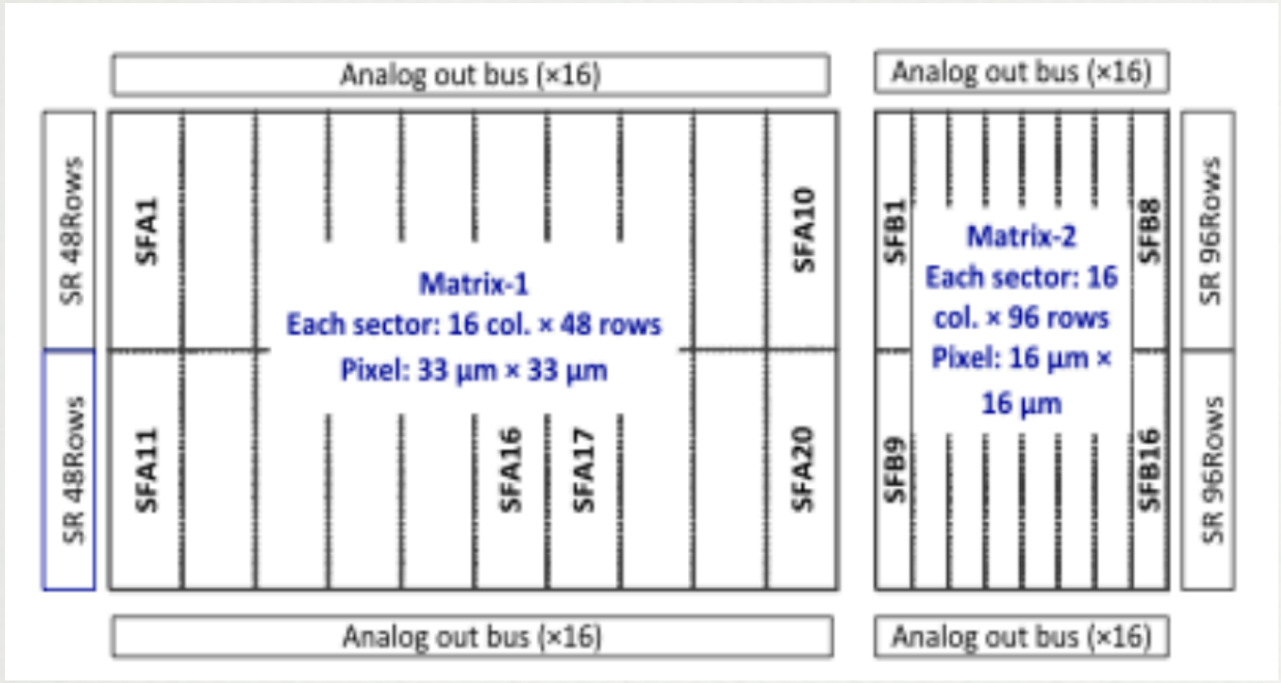


collected charge vs no. pixels

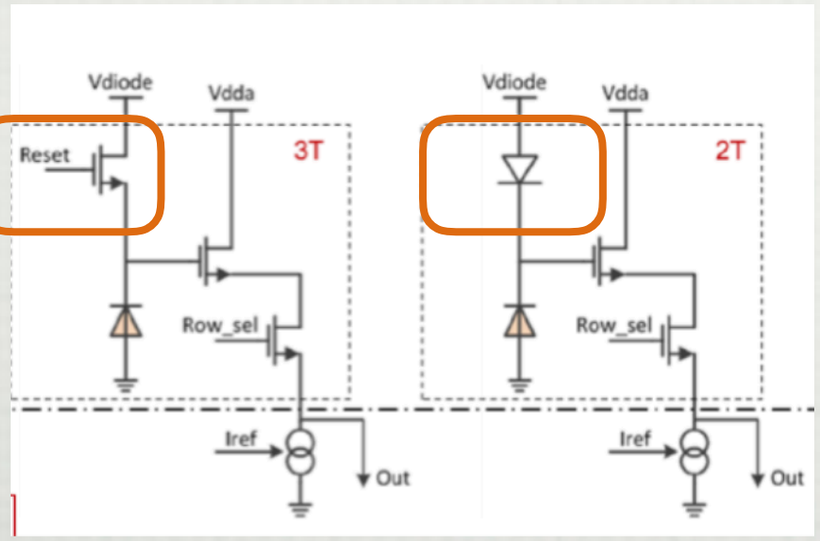
for various eps thickness and resistivity

⇒ Study of the pixel cell

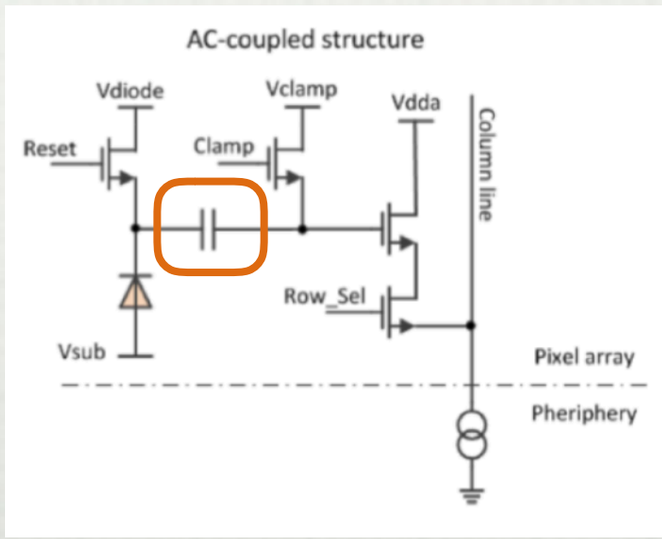
(Y. Zhang et al., NIM A831 (2016) 99-104 + Ping Yang's talk)



3T + 2T (x 2, nmos & pros), DC coupled



AC coupled



A Si STRIP DETECTOR WITH INTEGRATED COUPLING CAPACITORS

M. CACCIA & al.

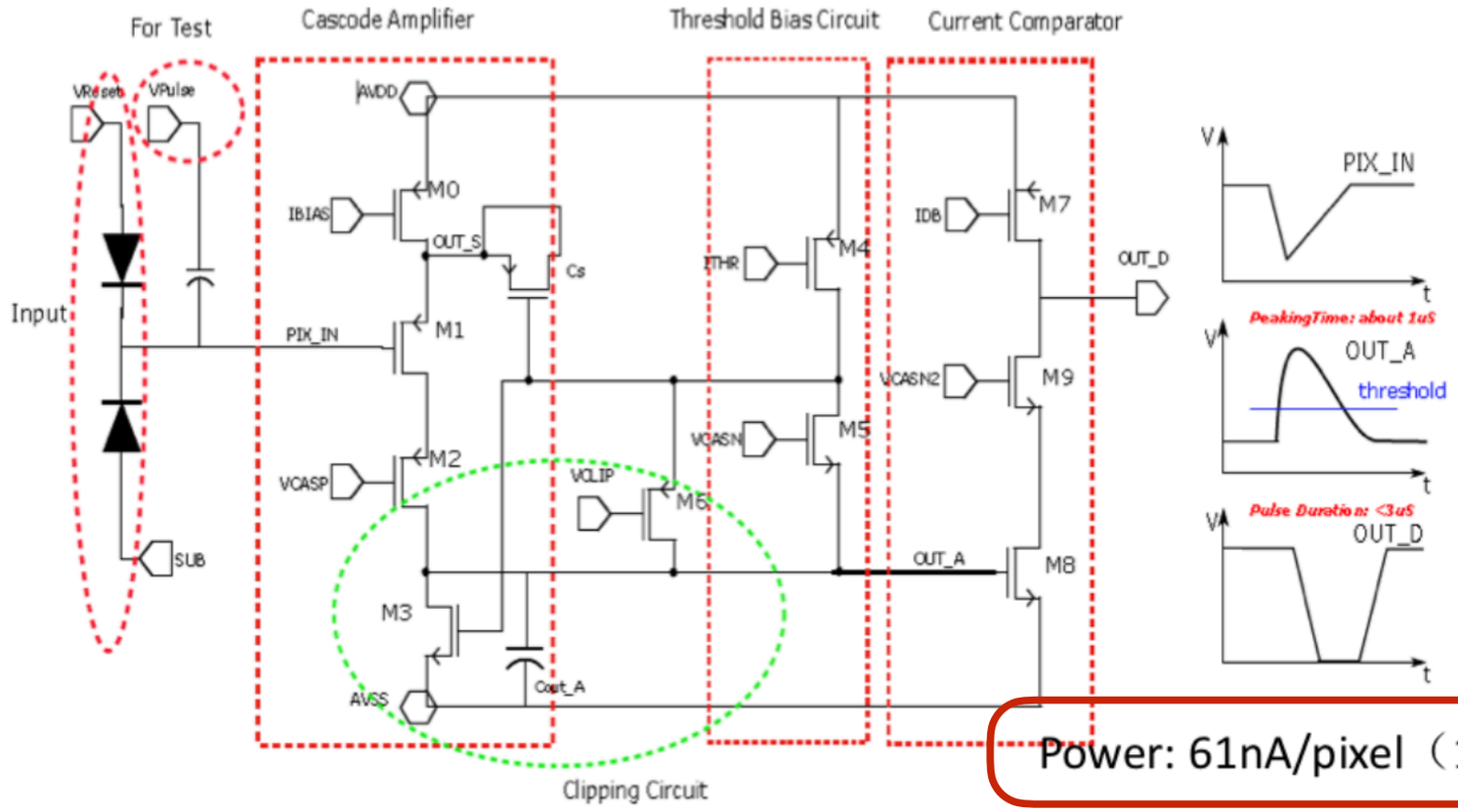
Dipartimento di Fisica dell'Università and Sezione INFN, Milano, Italy

NIM A260 (1987) 124-131

⇒ Digital read-out machine (after Ping Yang's talk)

A series of "machines" have been designed, including a "low power" version of the ALPIDE

MIC4 Front-end : similar to ALPIDE



Power: 61nA/pixel（17.6mW/cm^{-2}）

- Signal charge creates negative voltage step ΔV_{PIX_IN} at input node(PIX_IN). M1 acts as a follower and force source to follow gate.
- Threshold 140 e- : from OUT_A baseline voltage to point where discriminated output OUT_D flips when $I_{M8} > I_{DB}$.

$$\Delta V_{OUT\_A} \approx \frac{C_s \bullet \Delta V_{PIX\_IN}}{C_{OUT\_A}} = \frac{C_s}{C_{OUT\_A}} \bullet \frac{Q_{in}}{C_{PIX\_IN}}$$

Peaking time< 1 µs, duration < 3 µs, ENC < 8 e- (including amp noise ~5 e- and mismatch ~2 e-)

possibly not good for the GigaZ - and the clock is not known (to me)

Conclusions:

- The new technologies certainly offer unprecedented opportunities
- I believe the running conditions at the Z shall be carefully considered in designing the detector
- the real CHALLENGE, to me, will be designing an architecture providing the required data evacuation rate with the MINIMUM power dissipation, resulting by an optimisation of the ANALOG CELL, the digital architecture, the clock distribution
- **Having DESIGNERS on our side**, and considered the current level of activities , I see 3 options:
  - **be conservative**, start by the ALPIDE design and join the Chinese effort (actually Ping Yang is in ALICE)
  - **be smart**, exploit what we did in the past (e.g. the STm130nm design by the UNIPV-UNIBG teams) and what is being done (e.g. SEED (Sensor with Embedded Electronics Development)- Pd (Piero Giubilato), TO (Angelo Rivetti, PI), TIFPA (Claudio Piemonte))
  - **be brave**, start with something NEW (e.g. the mini-strips)

Thank you very much!