L'upgrade di CMS per HL-LHC

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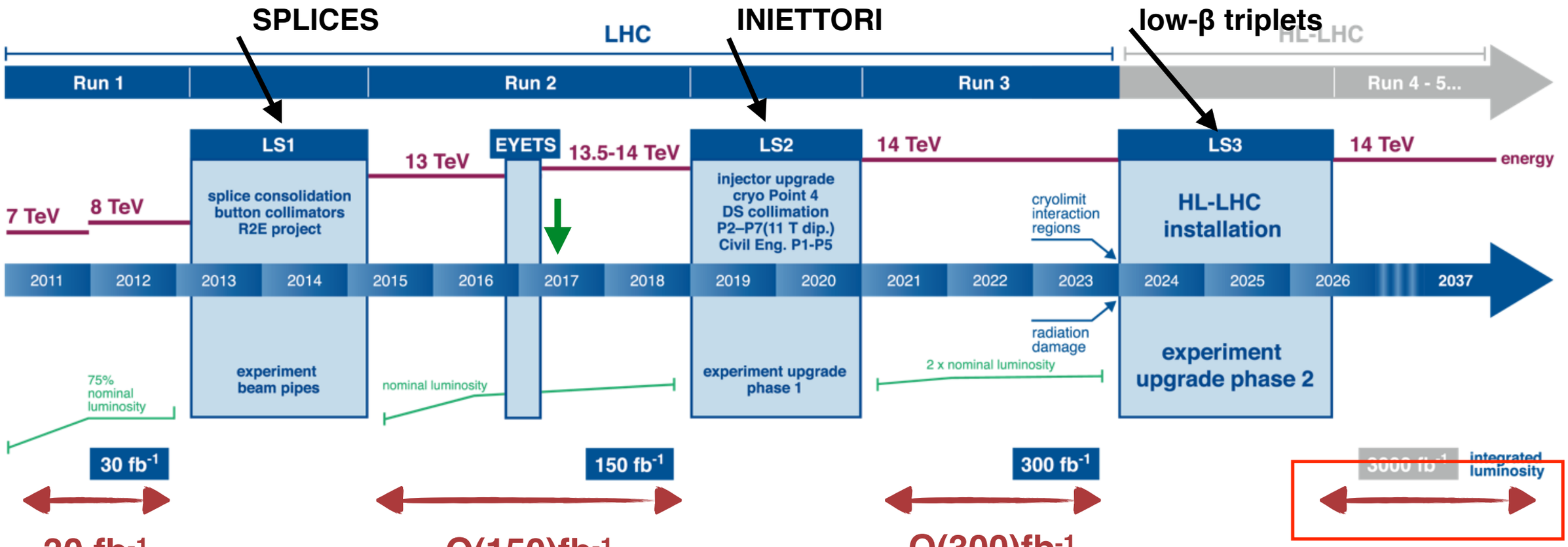
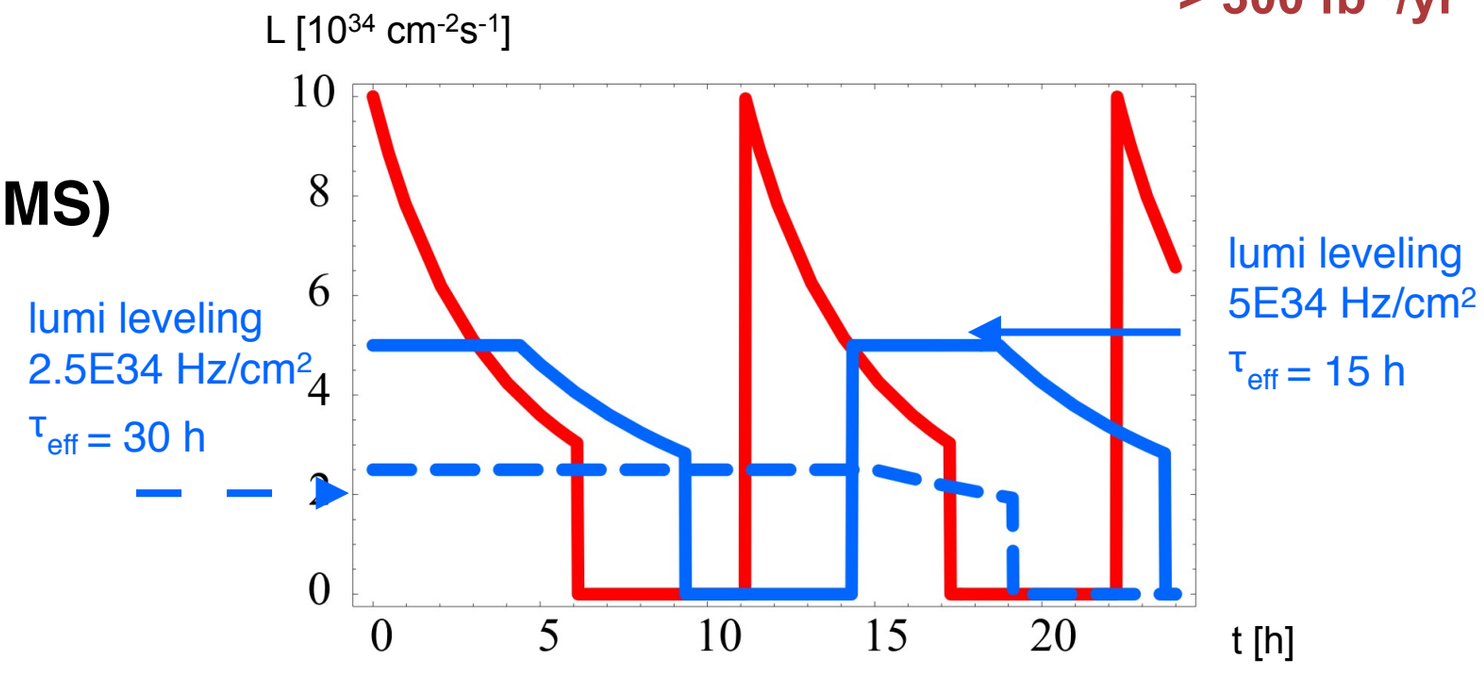
seminario Consiglio di Sezione
30 maggio 2017

LHC / HL-LHC Plan



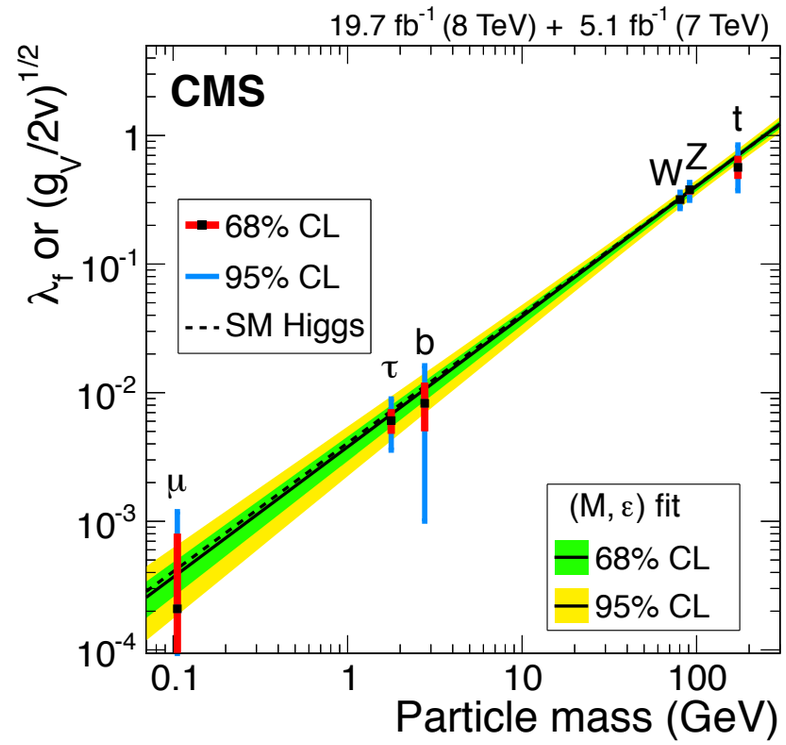
Rates di riferimento (ATLAS/CMS) per HL-LHC:

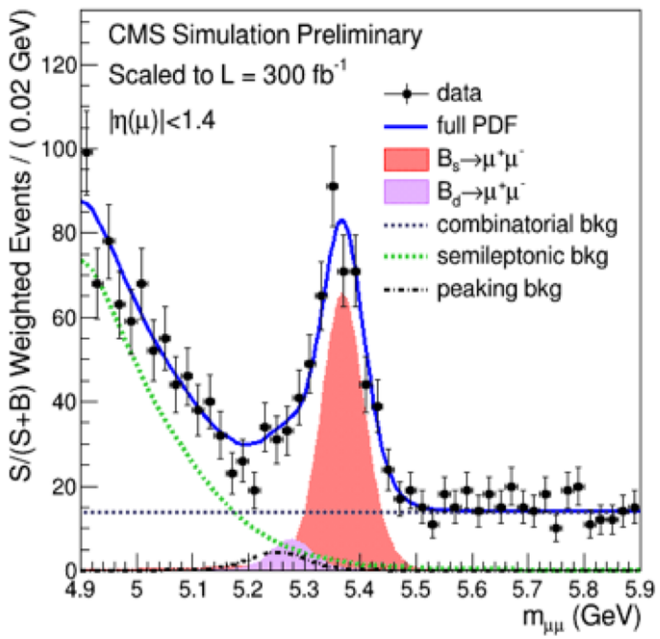
- **L~ 5-7.5 E34 Hz/cm²**
- **<PU> ~ 140-200 int / bx**

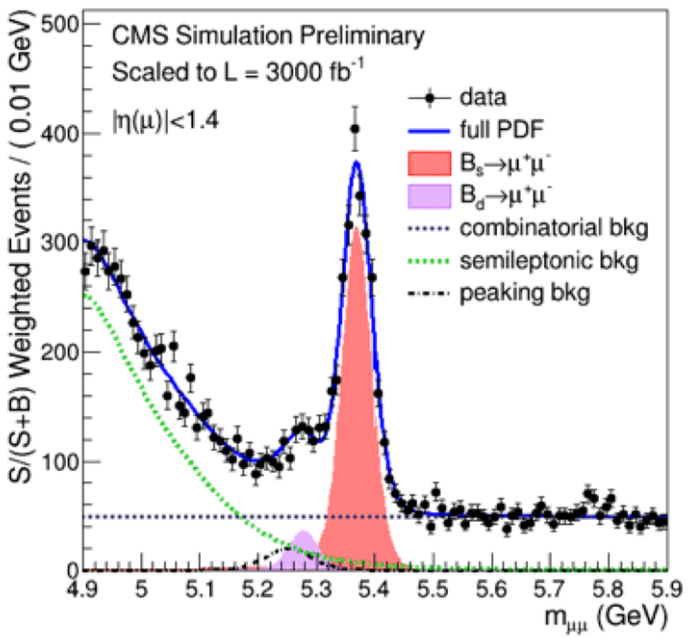


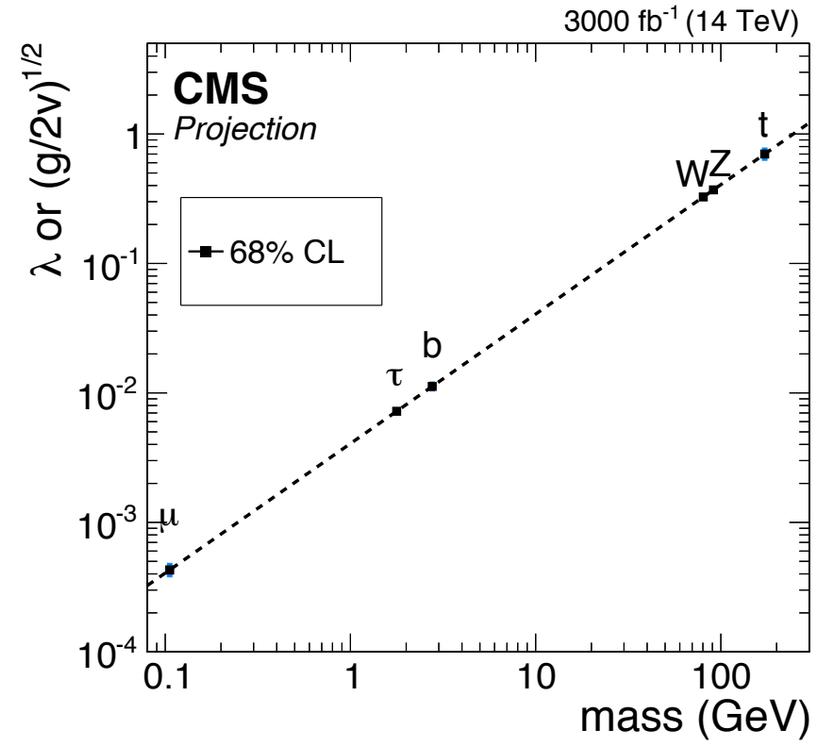
Fisica di precisione → oltre il MS

- Prospettive nel settore dell'Higgs
  - Accoppiamenti a qualche %
  - processi rari H→ $\mu\mu$, H → Z γ
  - self-coupling: σ(HH) ~ 1/1000 σ(H)
- Vector Boson Scattering
- Decadimenti rari del B
  - (es.) FCNC in $B_{d,s} \rightarrow \mu\mu$



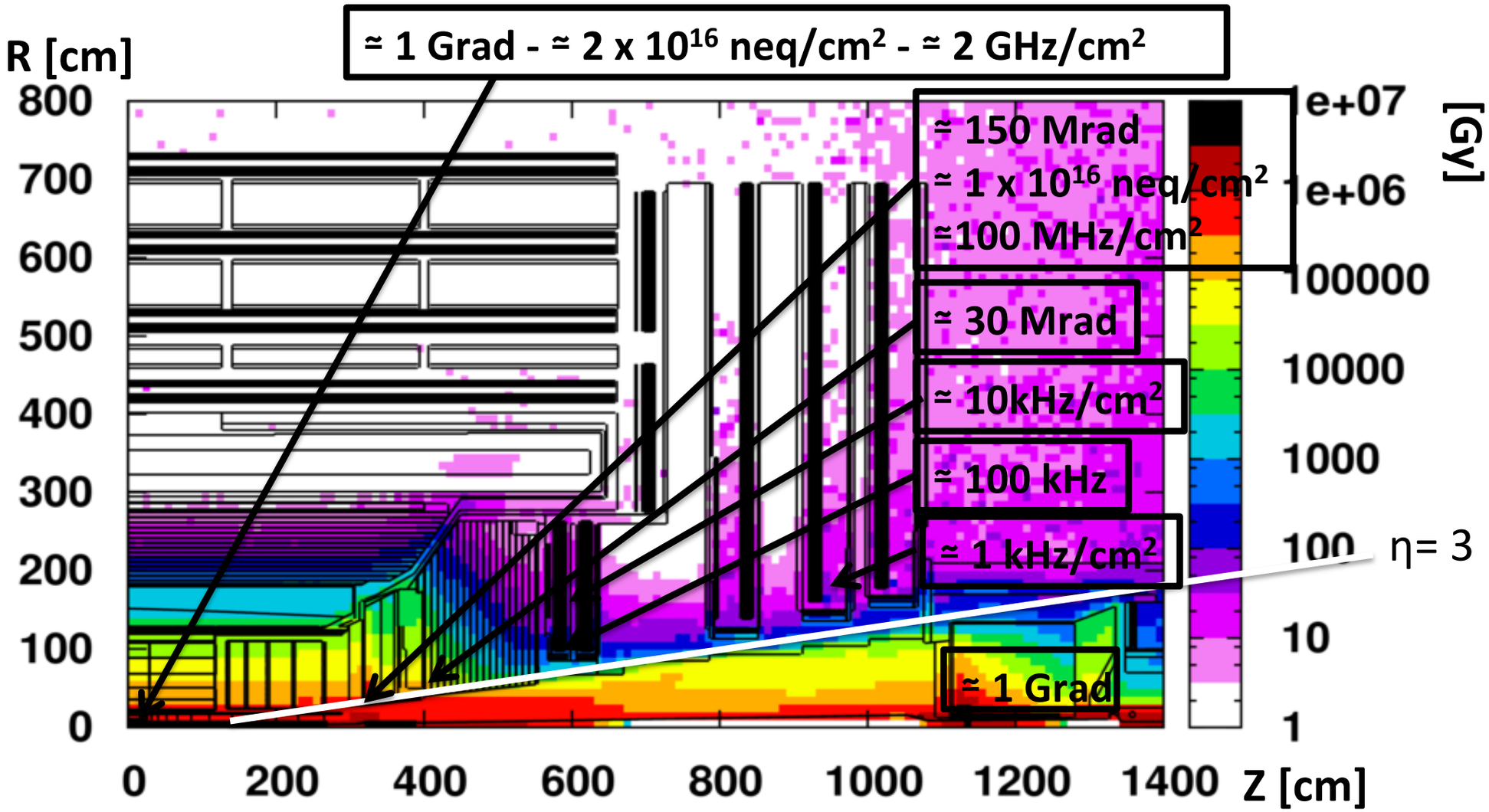






Alcune considerazioni generali

- Alti livelli di radiazione



CMS radiation dose map, neutron equivalent fluence and particle rates for luminosities of 3000 fb^{-1} (integrated) and 5 x 10^{34} Hz/cm^2 (instantaneous)

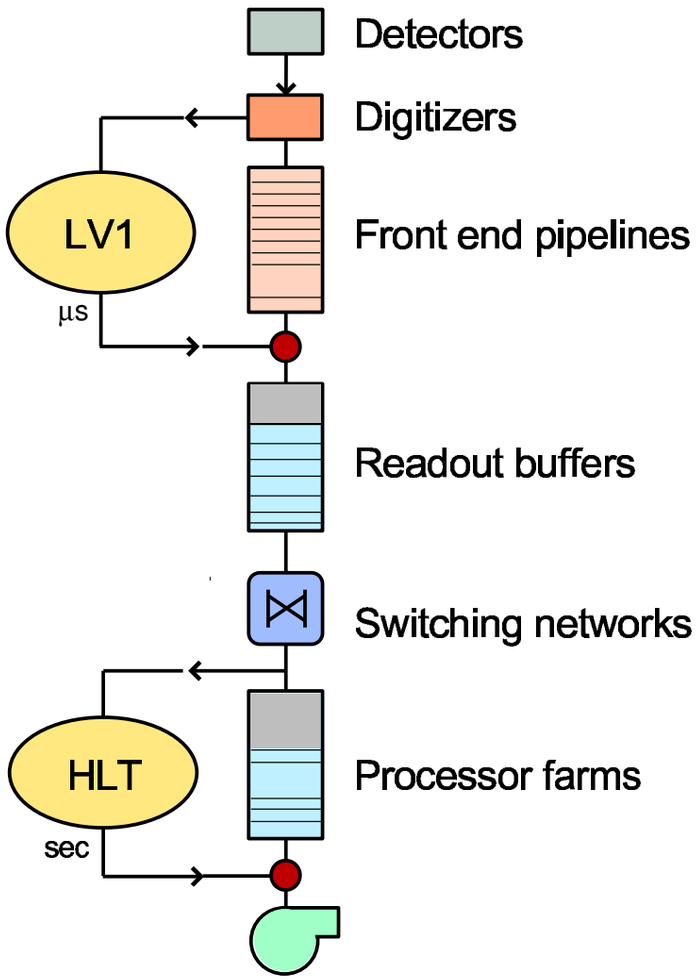
Alcune considerazioni generali

- Alto data rate

Present Trigger

Livello1 : 100kHz
Latenza ~ 3 μs

High Level Trigger: 100kHz
→ 2-300 Hz
Interamente software



Upgraded Trigger

L1 trigger latency ~ 12.5 μs

750 kHz at L1

7.5 kHz at the HLT

uso TRK @ Lv1 (Track Trigger)

Alcune considerazioni generali

- Alto PU

Maggiore segmentazione dei rivelatori (TRK, HGCAL)

Utilizzo dell’informazione temporale nei calorimetri

MIP timing layer

CMS, phase 2 upgrades

TRIGGER:

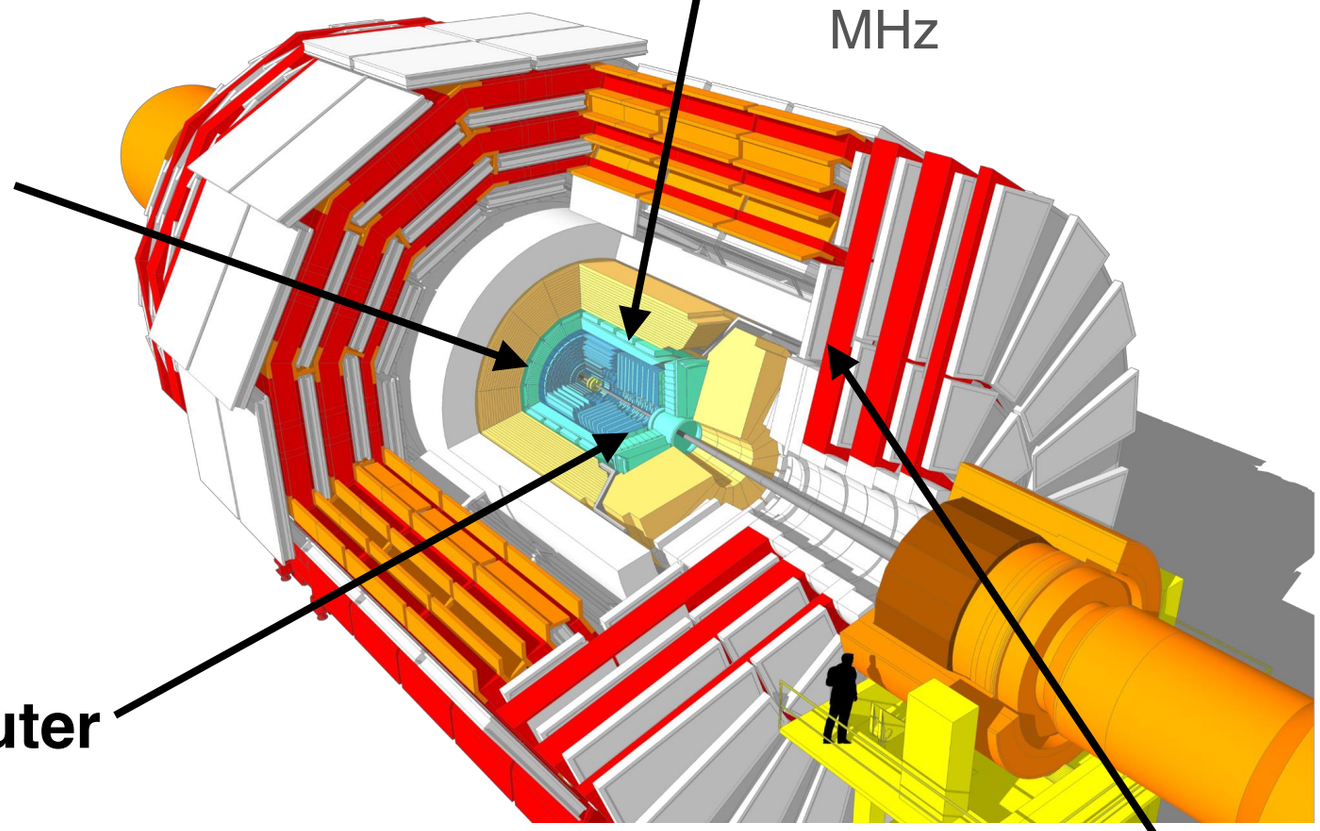
- L1 Track Trigger (hw)
- 750 kHz L1 rate, 12.5 μs latency
- 7.5 kHz HLT output

ECAL B:

- diminuita T (8 deg) → mitigato l'effetto della rad. sulla risoluzione
- nuovi VFE/FE/BE GBT @ 10Gbps → trasferimento dati dai cx a 40 MHz

Nuovo endcap "High Granularity Calorimeter"

- Rad. tolerant
- segmentazione trasversale e longitudinale
- capacità di timing

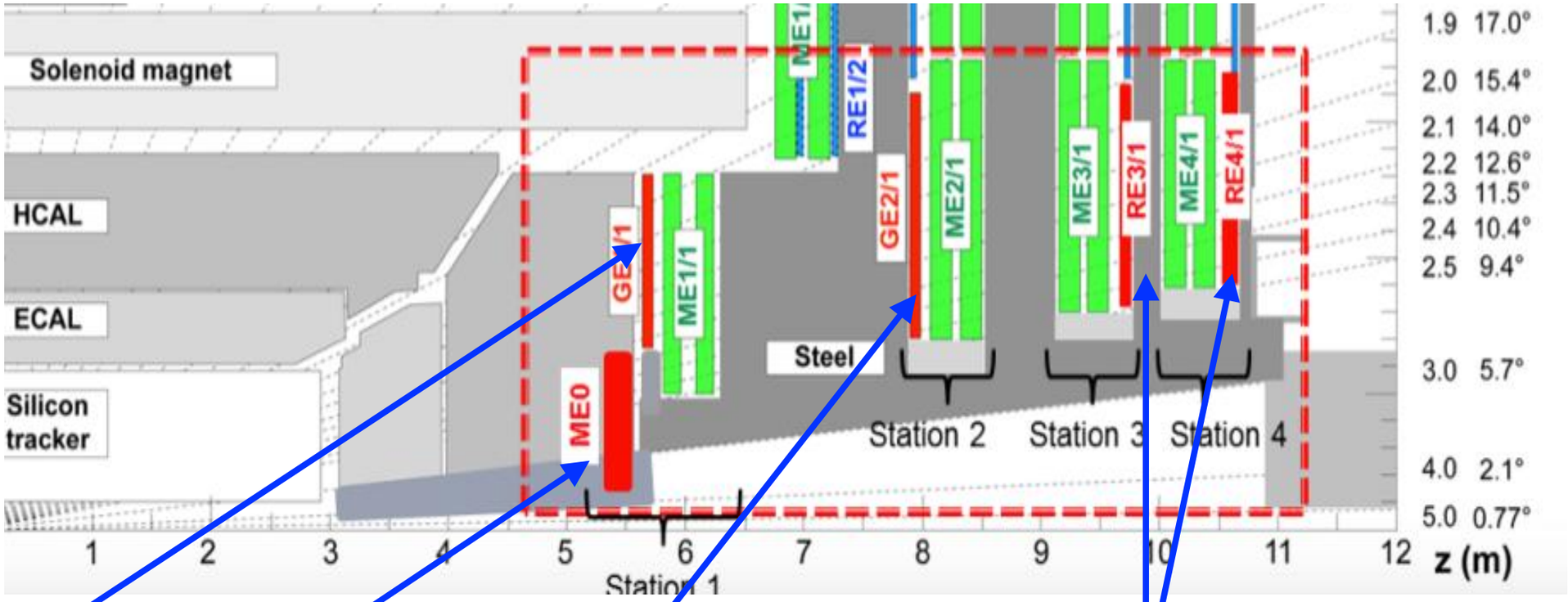


- **Nuovo tracciatore: px+outer tracker**
  - Rad. tolerant - più leggero - maggiore granularità
  - r/o selettivo a 40 MHz per L1 trigger
  - Accettanza estesa fino a $\eta \simeq 3.8$

Potenziamento rivelazione μ

- nuova elettronica FE/BE per (DT+CSC)
- complete RPC coverage $1.6 < \eta < 2.4$
- μ-tagging ad alto η: GEM/iRPC per $2.4 < \eta < 3$

μ system upgrade

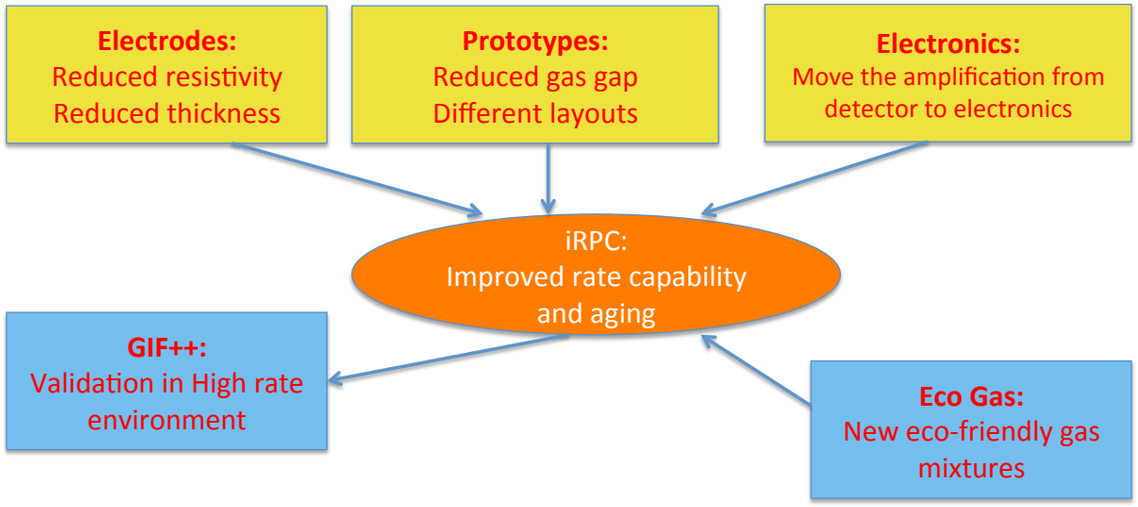


GE 1/1 : "triple GEM" (Gas Electron Multiplier) chambers
inst. LS2

MEO: MUON tagger high η (η < 2.8)
GEM chambers
inst. July 2024

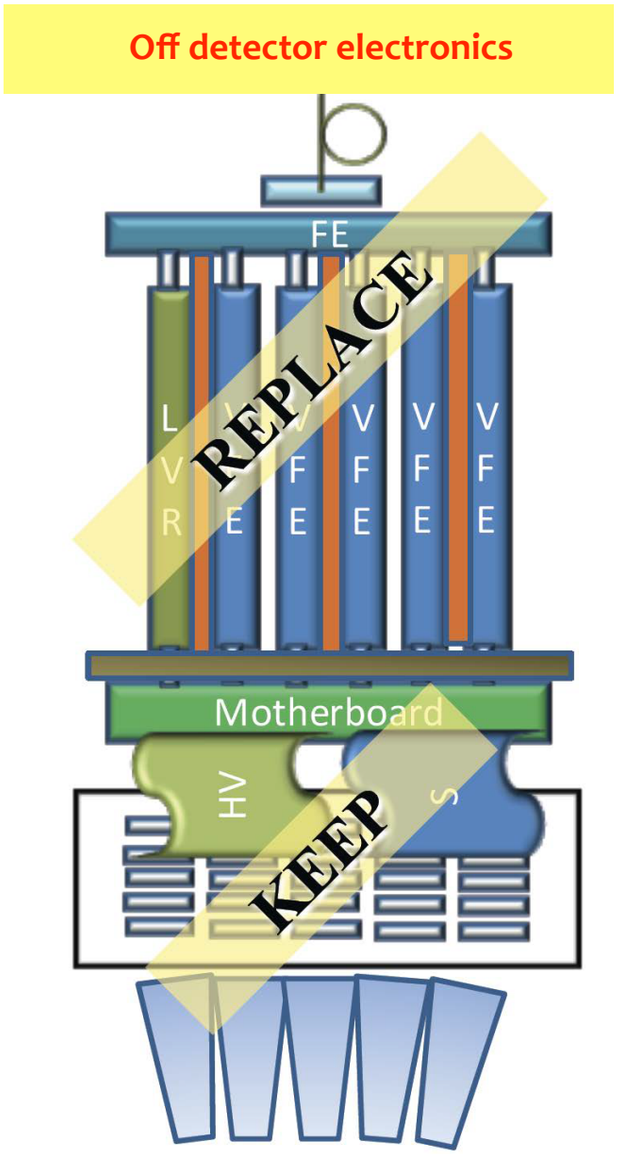
GE2/1: 1.6 < η < 2.4
installation: YETS 2022
"triple GEM" . Alternatia: μ-RWELL

RE3/1, RE4/1 "improved RPC"



ECAL barrel upgrade

- Sostituzione completa del VFE
  - per soddisfare le nuove L1 trig latency e L1 accept rate
  - uso di Versatile link con GigaBit Transceiver (GBT) per mandare informazione dai singoli cristalli al Trig L1 (trigger primitive off-detector)
  - mitigazione dell'effetto degli spikes
  - nuovo amplificatore ottimizzato per timing di precisione
    - ✓possibili ~30ps su γ da 25GeV
- raffreddamento a 8 C
  - mitigazione dark-current negli APD

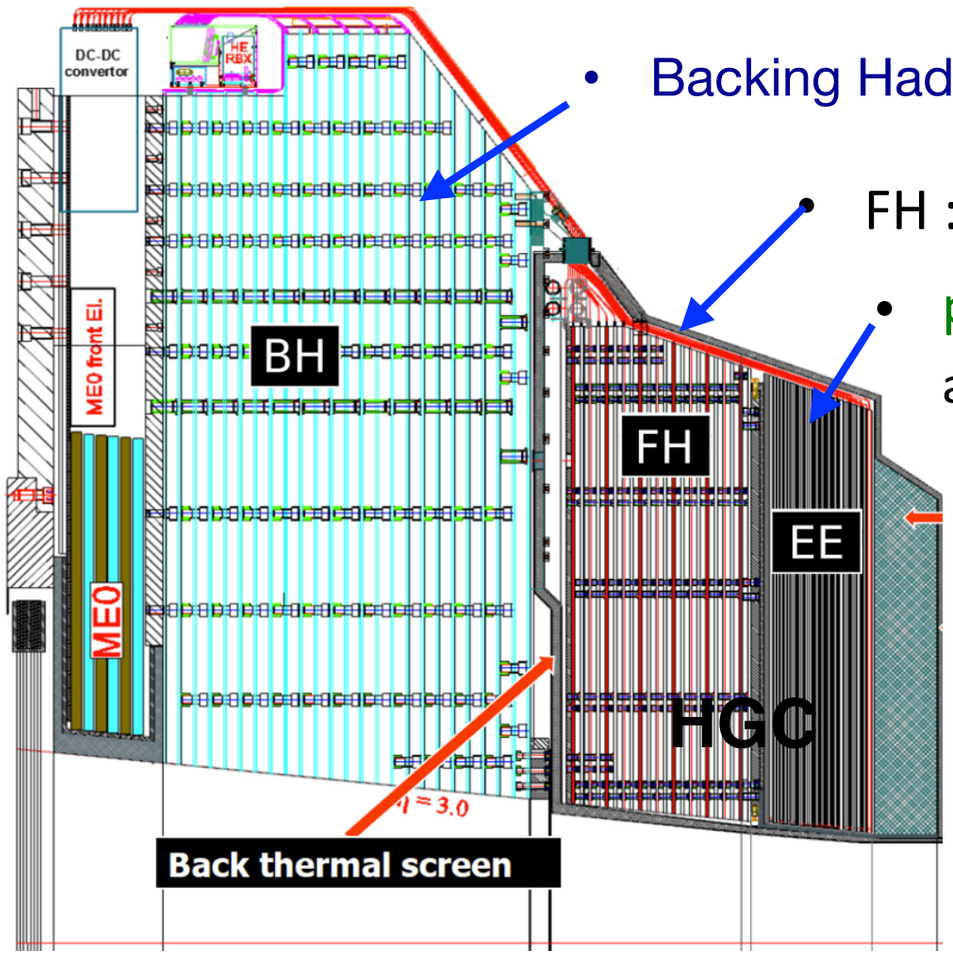


Endcap Calorimeter

- Dose e fluenza → danno troppo elevato a e cristalli → Sostituzione completa di Endcap Calorimeter
- ~50 ps timing (cell level) for pile-up rejection

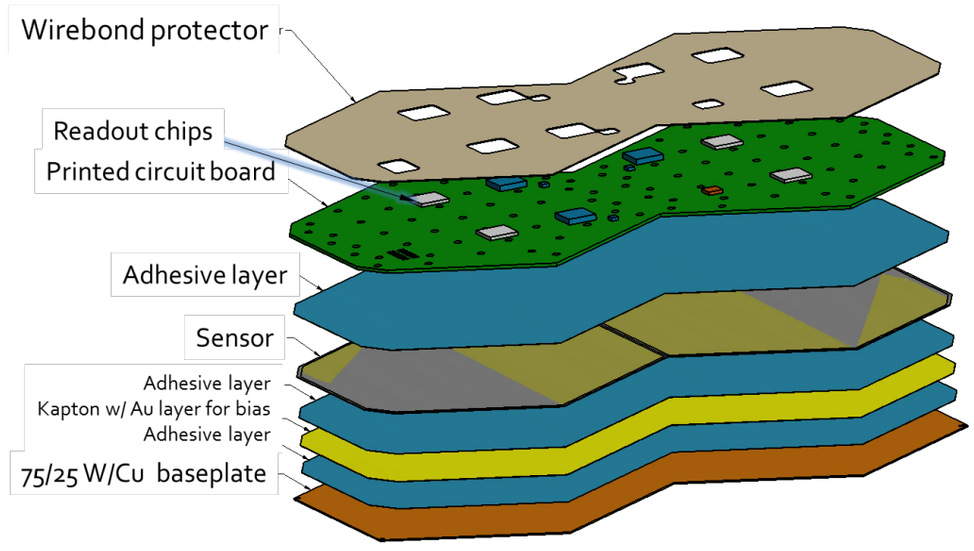
- specializzato nella misura di jets, τ-jets, boosted jets, VBF jets

- *593 m^2 di silicon*
- *6M canali, celle di 0.5-1 cm^2*
- *52 layers*
- *21,660 moduli (sensori 8” o 2x6”)*



-30 °C

- Backing Hadronic: (5.5 λ) → 12 layers di Scintillatore/ottone
- FH :parte adronica: (3.5 λ): 12 layers di Silicio/ottone
- parte e.m. (25 X_0, 1.5λ): 28 layers di Silicio con assorbitore W/Cu



2 sensors per baseplate

Tracker Upgrade

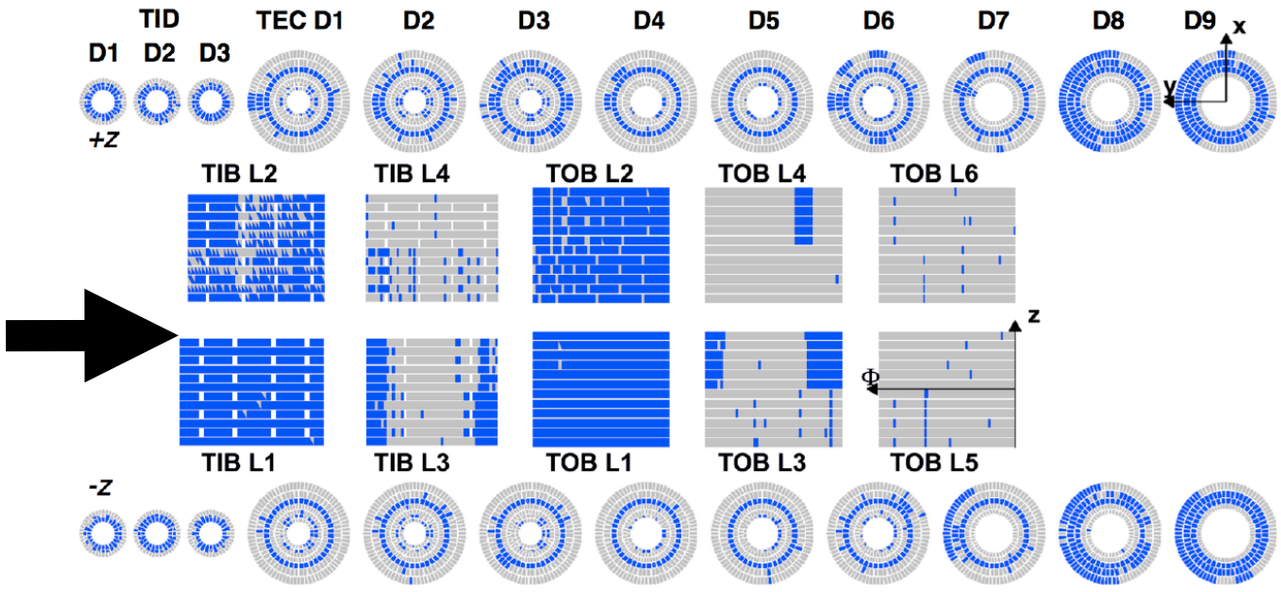
Tracker phase1: the end

	Design limitations of current Tracker	HL-LHC conditions
Pileup	20-30	140-200
int. lumi.	< 1000 fb^{-1}	3000-4000 fb^{-1}

Radiation damage will lead to many non-functional modules

- Increased leakage current cannot be compensated by cooling anymore

Simulation of non-functional modules of the current tracker (in blue) after 1000 fb^{-1} int. luminosity.



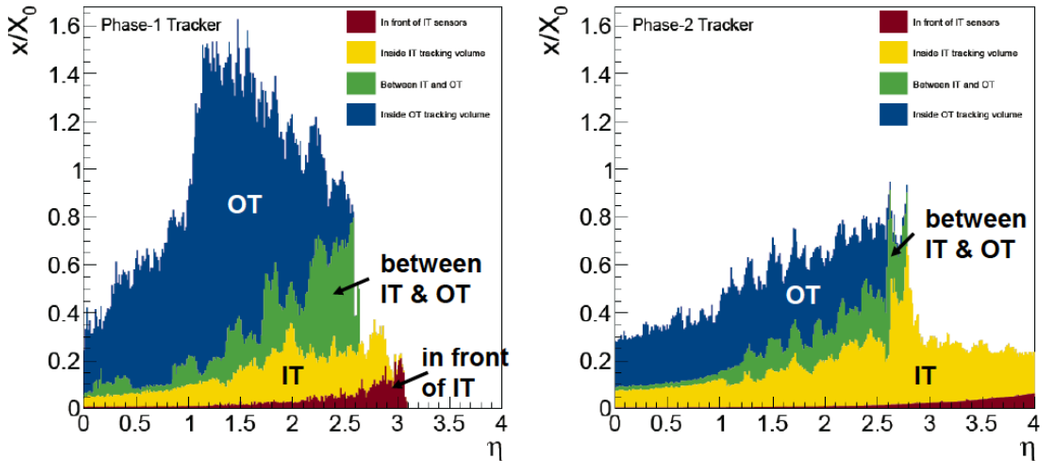
New Phase2 Tracker

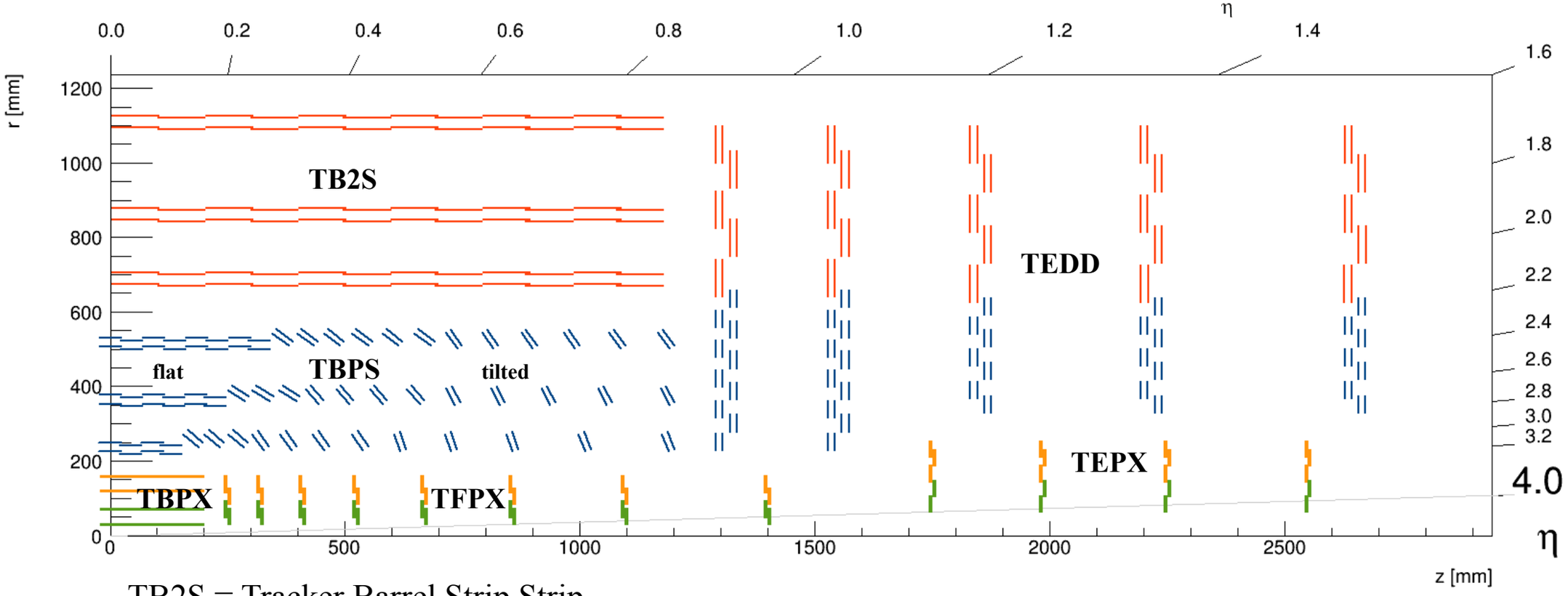
tracciatura fino a η=4

L1 track trigger fino a η = 2.4

alta granularità

material budget ridotto

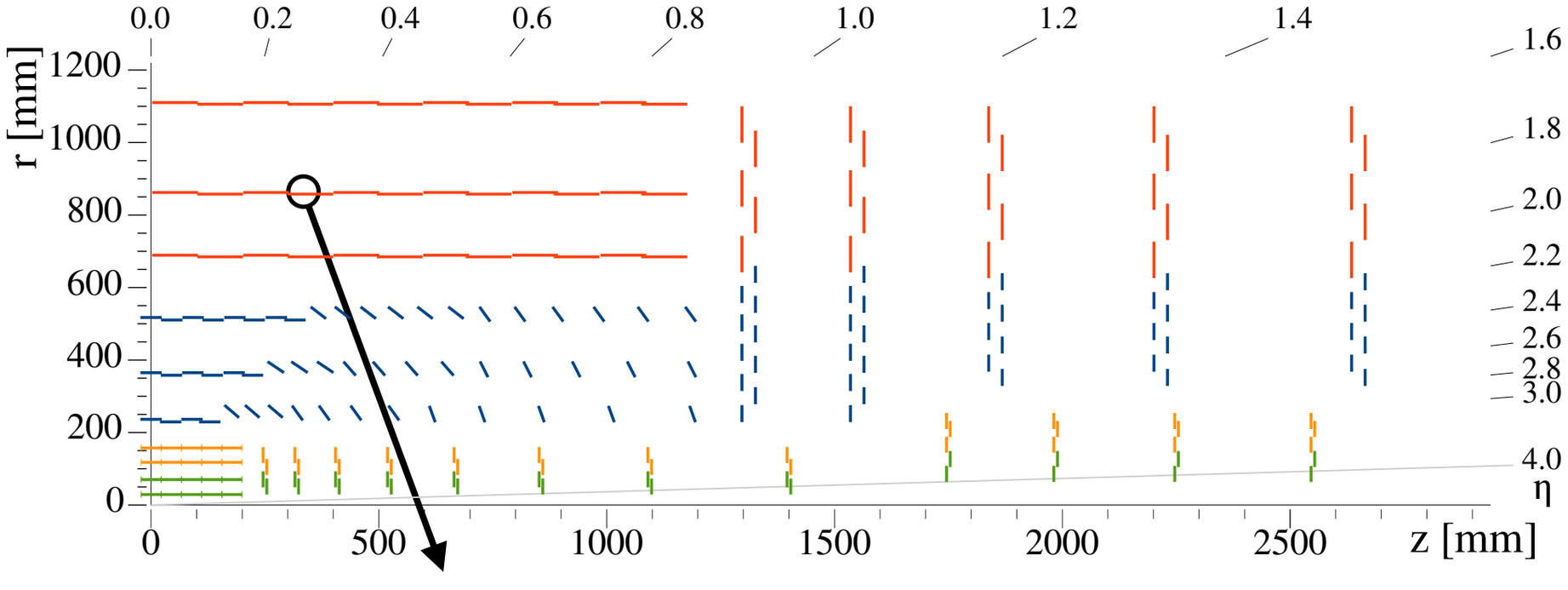


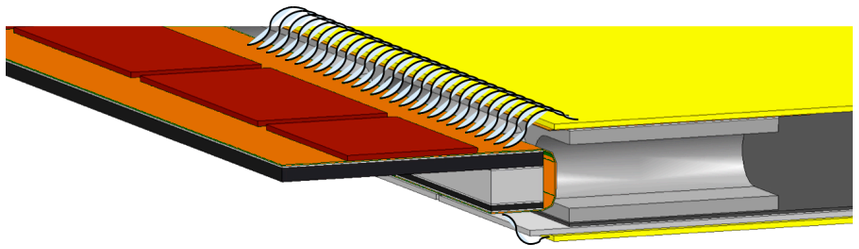


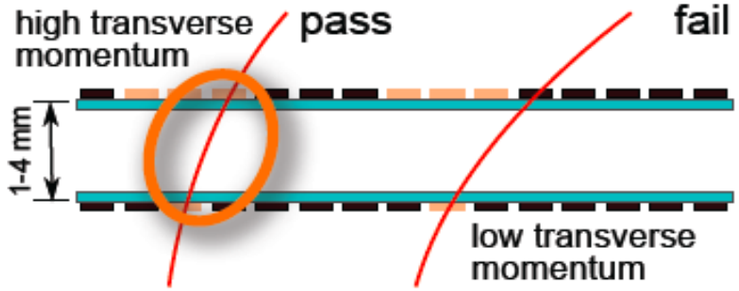
TB2S = Tracker Barrel Strip Strip
TBPS = Tracker Barrel Pixel Strip
TEDD = Tracker Endcap Disks

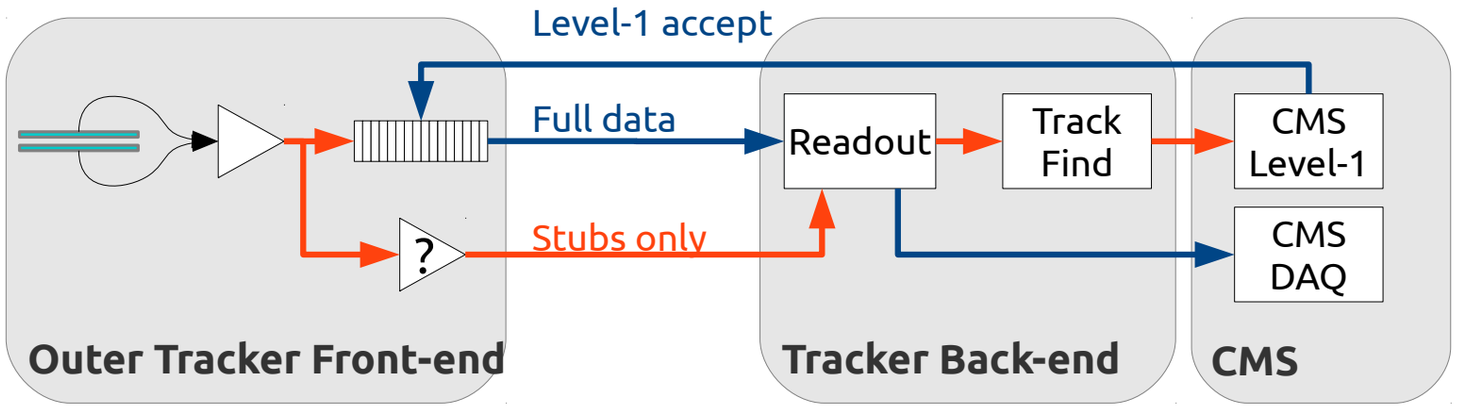
TBPX = Tracker Barrel Pixel
TFPX = Tracker Forward Pixel
TEPX = Tracker Endcap Pixel

Pt discriminating modules









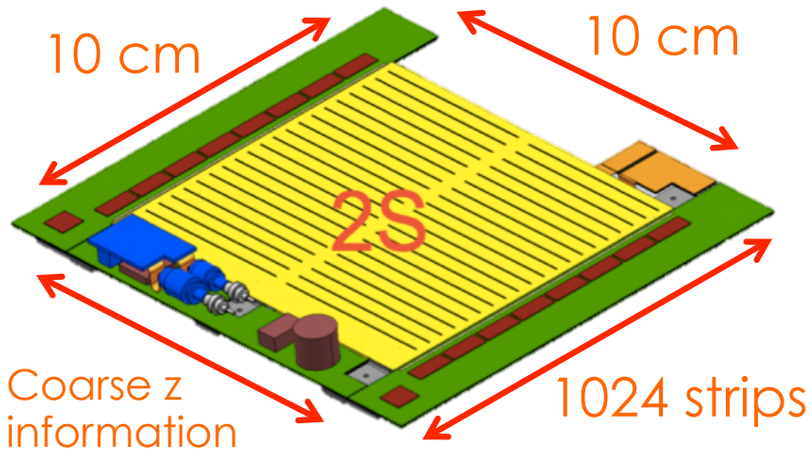
Gli “stub” vengono inviati al BE ed utilizzati per creare tracce a L1 con pt > 2 GeV @ 40MHz

@ 40 MHz – Bunch crossing
@ 750 kHz – CMS Level-1 trigger

Strip Sensor × 2:
5 cm × 90 μm

+

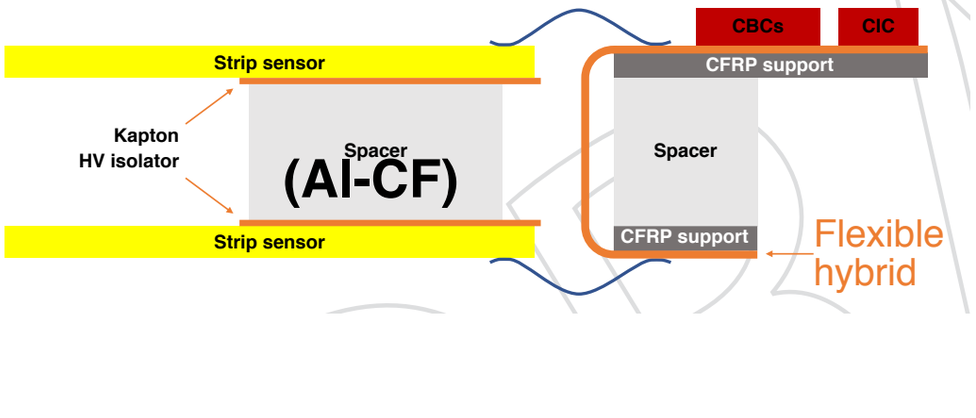
Strip Sensor × 2:
5 cm × 90 μm

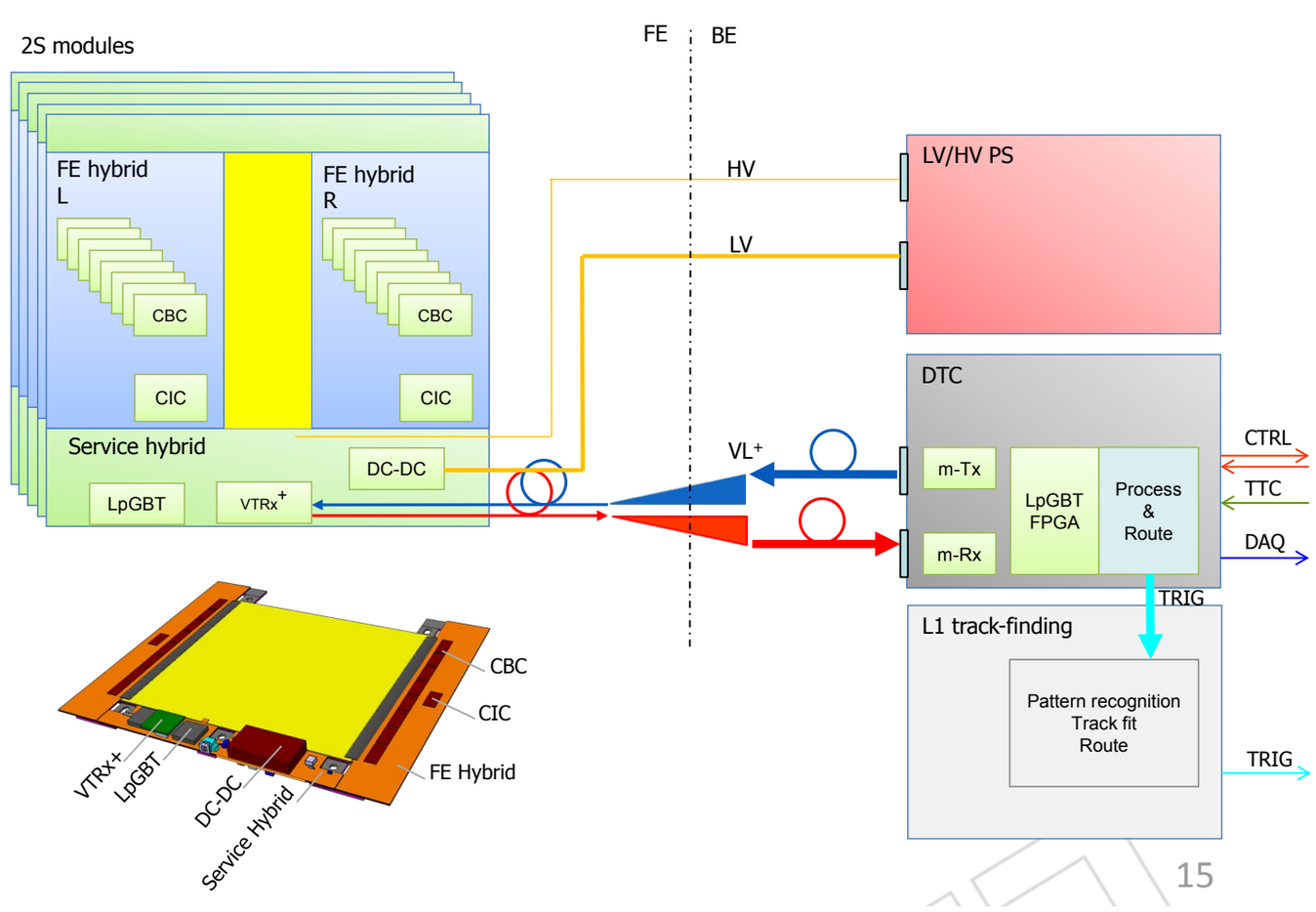


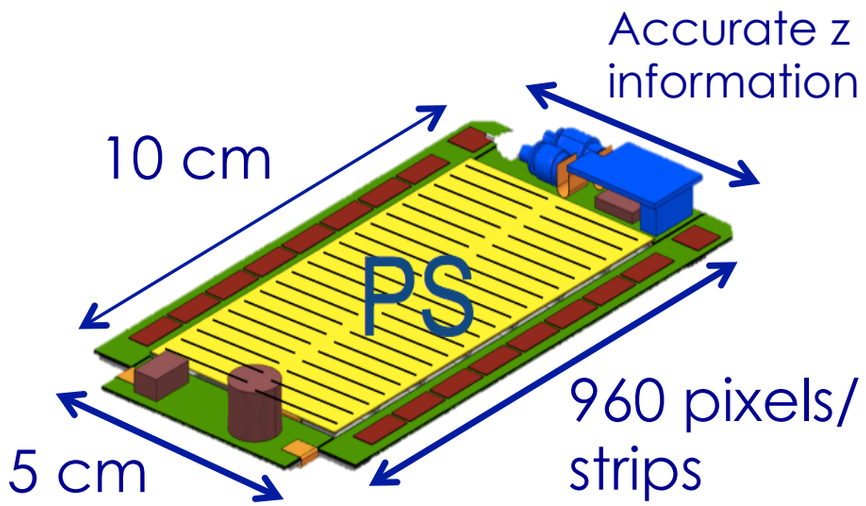
CBC = CMS Binary Chip
CIC = Concentrator Integrated Circuit

LpGBT = Low Power Gigabit Transceiver
VL+ = Versatile Link Plus
VTRx+ = Versatile TRansceiver Plus

DTC = Data, Trigger and Control Board
3 data streams: Data,TRIG, Timing and Control







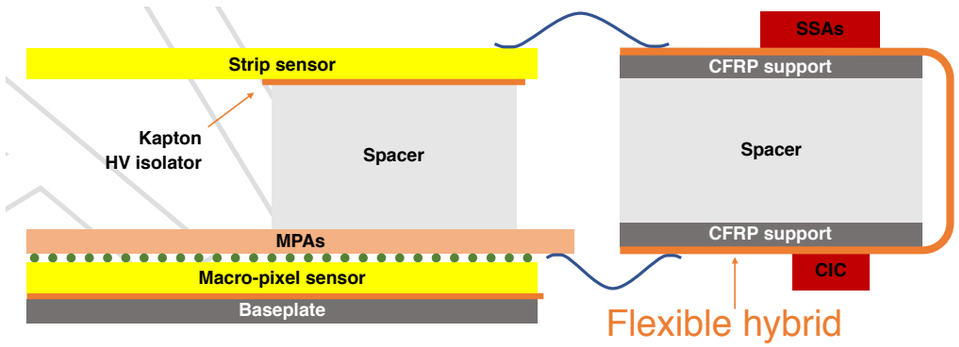
Strip Sensor × 2:
2. 5 cm × 100 μm

+

Pixel Sensor × 32:
1.5 mm × 100 μm

SSA = Short Strip ASIC
MPA =Macro Pixel ASIC
CIC = Concentrator Integrated Circuit

LpGBT = Low Power Gigabit Transceiver
VL+ = Versatile Link Plus
VTRx+ = Versatile TRansceiver Plus



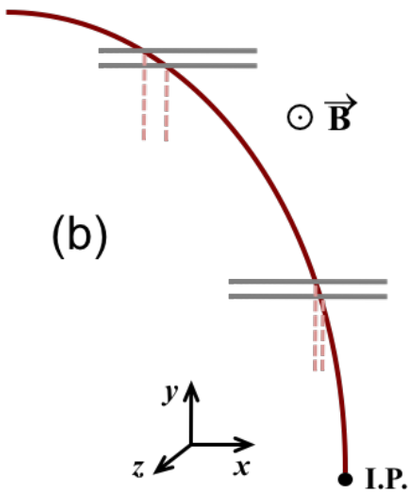


Table 3.2: Number of modules in the Outer Tracker, by module type and variant.

Module type and variant		TBPS	TB2S	TEDD	Total per variant	Total per type
2S	1.8 mm	0	4464	2792	7256	**7680**
	4.0 mm	0	0	424	424	
PS	1.6 mm	826	0	0	826	**5616**
	2.6 mm	1462	0	0	1462	
	4.0 mm	584	0	2744	3328	
Total		**2872**	**4464**	**5960**	**13296**	

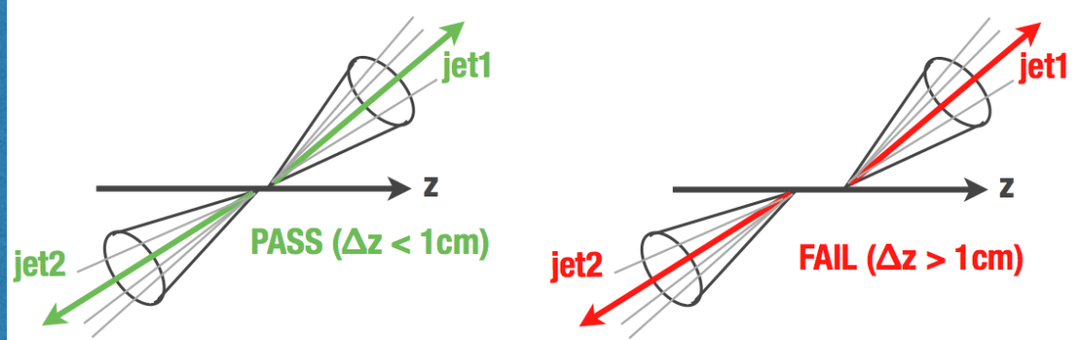
L1 TRK Trigger: motivazioni

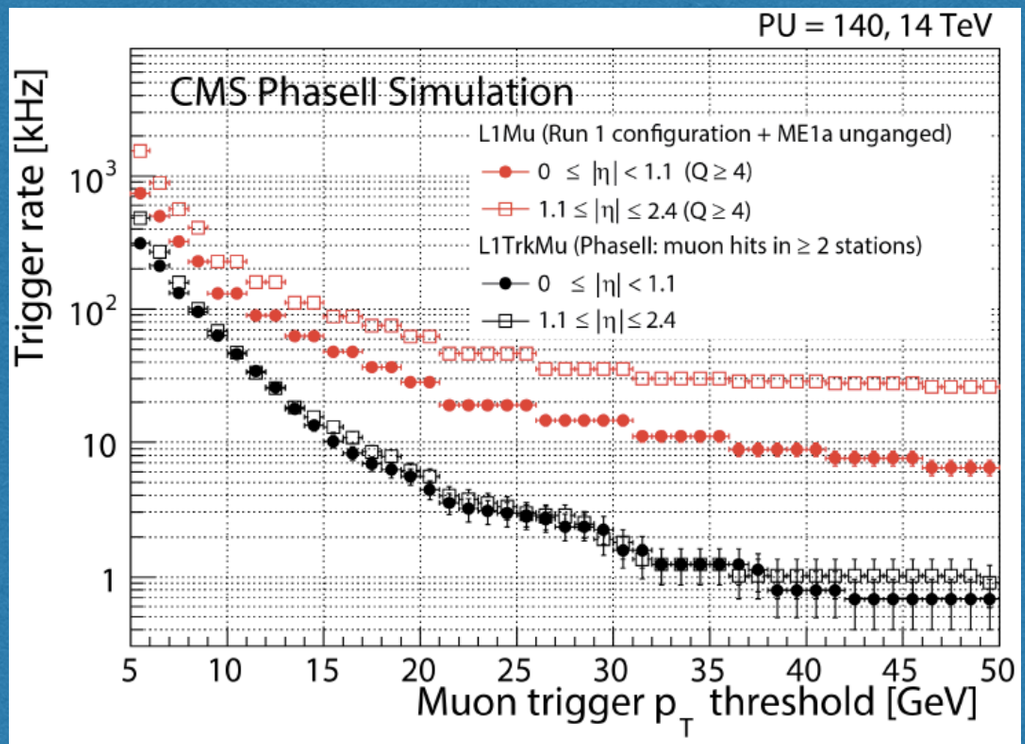
TRK necessario per guadagnare selettività sugli oggetti primari (μ, e, τ, γ, missing Et)

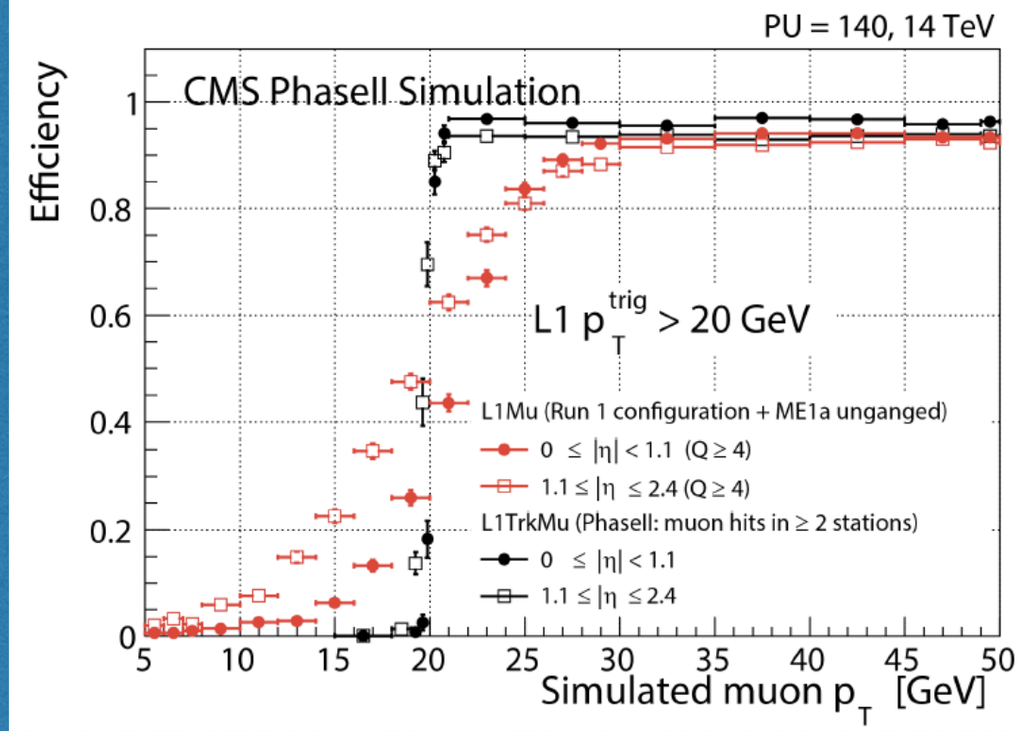
distinzione γ vs e

isolamento di γ,μ,e

misura missing Et → associazione jet-vertice in condizioni di alto pile up



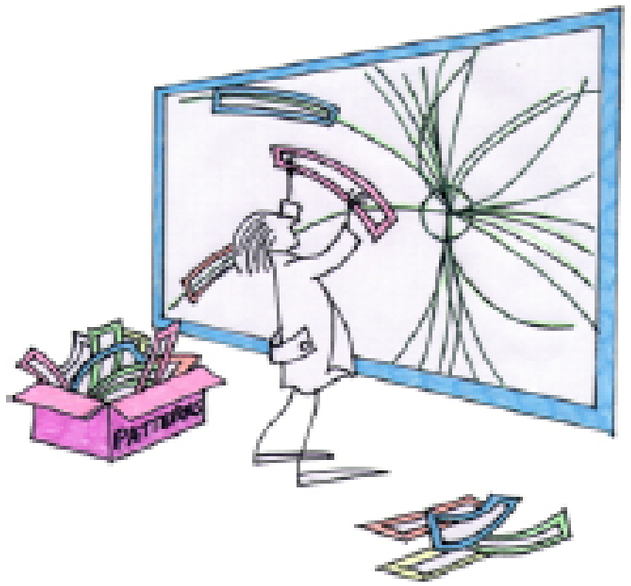




Risoluzione pt →trigger threshold.

L1 TRK Trigger: come

Challenge: ~ 20000 stubs per ogni bx a 40 MHz
fornire tracce (patter recognition + trk fit) entro 4 *μ*s



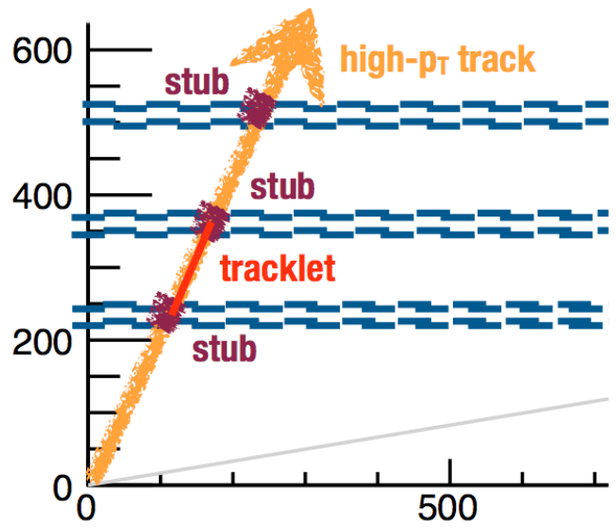
Tre approcci studiati:

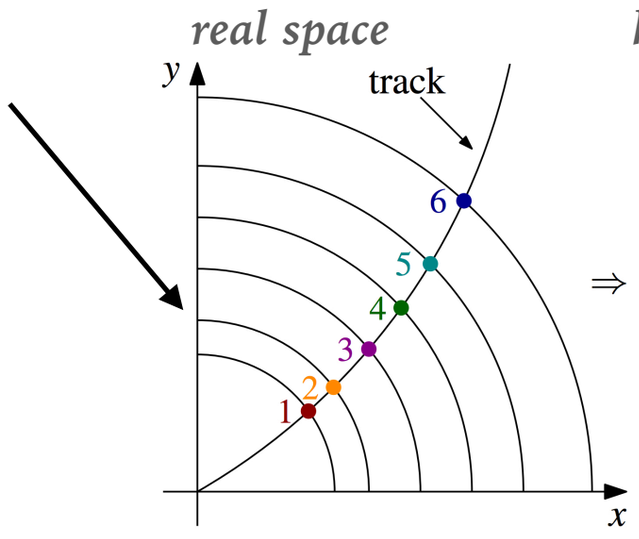
- memorie associative (AM) per la pattern recognition + FPGA per tracking

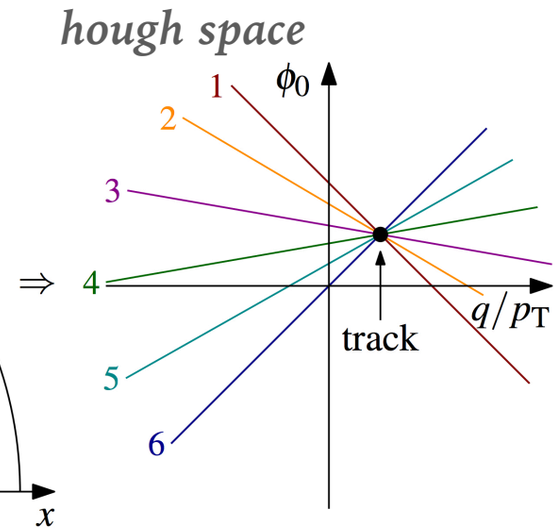
- ricostruzione basata su FPGA partendo da coppie di stubs (tracklets) (“road search”)

- Time Multiplexed: ogni bx esaminato isolatamente da un Track Finding Processor che implementa Hough Transform track finder + KF “cleaning”

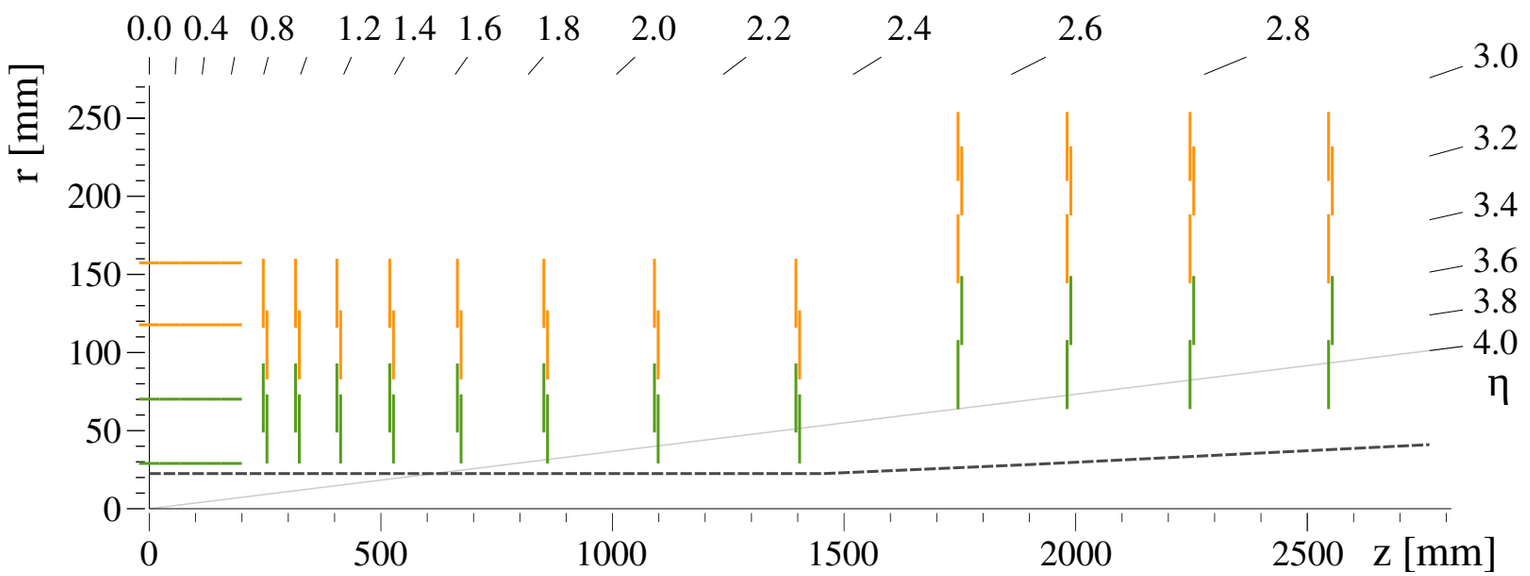
full FPGA approach







Inner Tracker

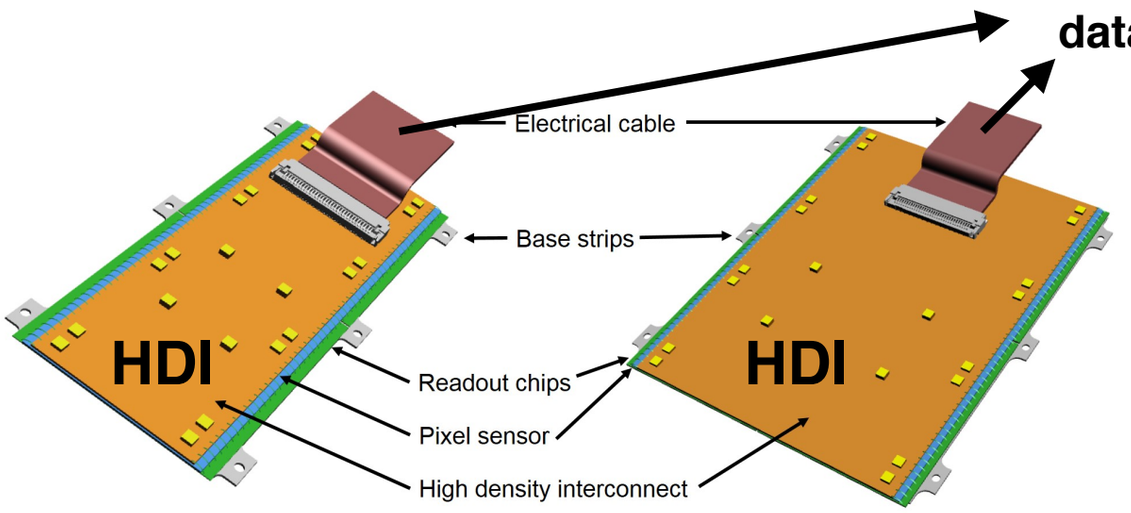


Hadron fluence after 3000 fb^{-1}

- 2×10^{16} n_{eq} cm^{-2} @ r=3 cm

Sensori **n^{+}-in-p sottili** (100-150 μm) - varie geometrie studiate (50x50 o 25x100 μm^2)

Large ROC: ~ 1.6 cm x 2 cm and ~ 144.000 pixels/PROC



2x1 RO chip **2x2 RO chip**

	TBPX	TFPX	TEPX	Total
Modules (type)	360 (1 × 2) 504 (2 × 2)	832 (1 × 2) 896 (2 × 2)	768 (1 × 2) 992 (2 × 2)	1960 (1 × 2) 2 392 (2 × 2)
Sensors	864	1 728	1 760	4 352
Pixel chips	2 736	5 248	5 504	13 488
Pixels [×10^6]	395	757	794	1947
Silicon area [m^2]	0.99	1.89	1.99	4.87

Italy @ Inner Tracker

- R&D sui sensori pixel al silicio **(FI, PI, MI, TO)**
- ROC chip: RD53 and Chipix65 **(TO, BA, PV, PD, PG, PI)**
- Serial Power distribution **(FI)**
- Struttura meccanica, cooling **(PI)**
- produzione moduli **(FI, PI)**

} **Sinergia con ATLAS**

Programma INFN su R&D px congiunto ATLAS+ CMS (RD_FASE2) ed accordo con FBK

- studio di sensori sottili planari e 3D, rad-hard per inner layers
- p-type 6” wafer, 100-130 μm spessore attivo
- layout compatibile con i chip r/o → pitch piccolo
- spark isolation, assottigliamento, bump bonding ad alta densità,
- Test su fascio dei sensori (3D e planari)

sinergia col programma AIDA2020 WP7 (Advanced Hybrid Pixel Detectors)

Programma R&D sui sensori px

- **Two pixel technologies for n-in-p wafers:**
  - Planar
    - Process Options: p-spray on wafer and/or p-stop around single pixel
    - Periphery design: standard and Active or Slim-Edge (special planar batches), multi Guard Rings
  - 3D Columnar
    - Single Sided processing optimized by FBK for different active thicknesses
    - Process options: bump on columns, poly-silicon ”cap” on top of junction columns
- **Productions, Achievements and Plans**
  - Two Planar and one 3D columnar pixel batches produced so far at FBK premises
  - Prototypes qualified in laboratory and in multiple beam test sessions 2015-2017
  - One neutron and two proton irradiation sessions done in 2016, two more to come in 2017
  - One new3D pixel batch in production now at FBK under AIDA-2020 WP7 agreement
  - One more Active/ Slim-Edge pixel batch agreed with AIDA-2020 to be started as soon layout is ready

R&D Working Groups in INFN and Universities: a long list of highly skilled people

Design, processing, qualification, assembly

M. Boscardin, G. Giacomini[(1)], S. Ronchin , N. Zorzi (FBK Trento)
G.F. Dalla Betta, D.M.S. Sultan (Trento)
M. Meschini,(Firenze)
A.Messineo, R. Dell’Orso (Pisa)
F. Ravera, A. Solano (Torino)

[(1)] Now at BNL

Test Beam and Data Analysis

M. Dinardo, D. Menasce, L. Moroni, D. Zuolo (Milano)
C. Civinini, M. Meschini, G. Sguazzoni L. Viliani, I. Zoi[(2)] (Firenze)
L. Uplegger, R. Rivera, C. Vernieri (FNAL, USA)

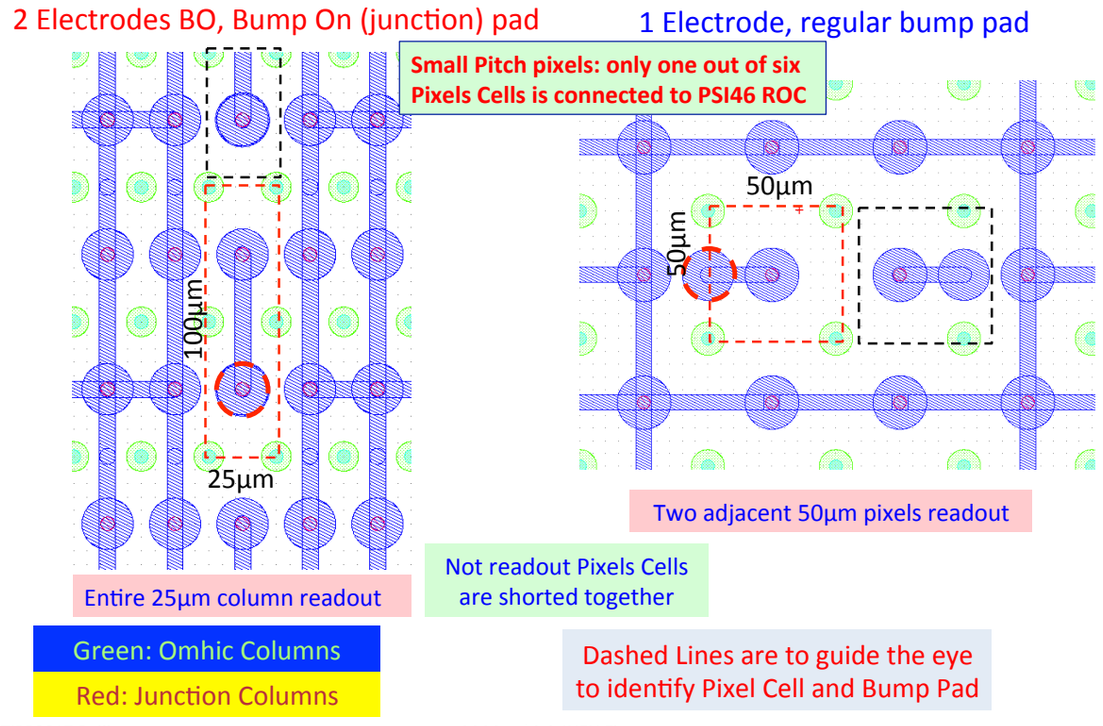
[(2)]Now at Hamburg Univ.

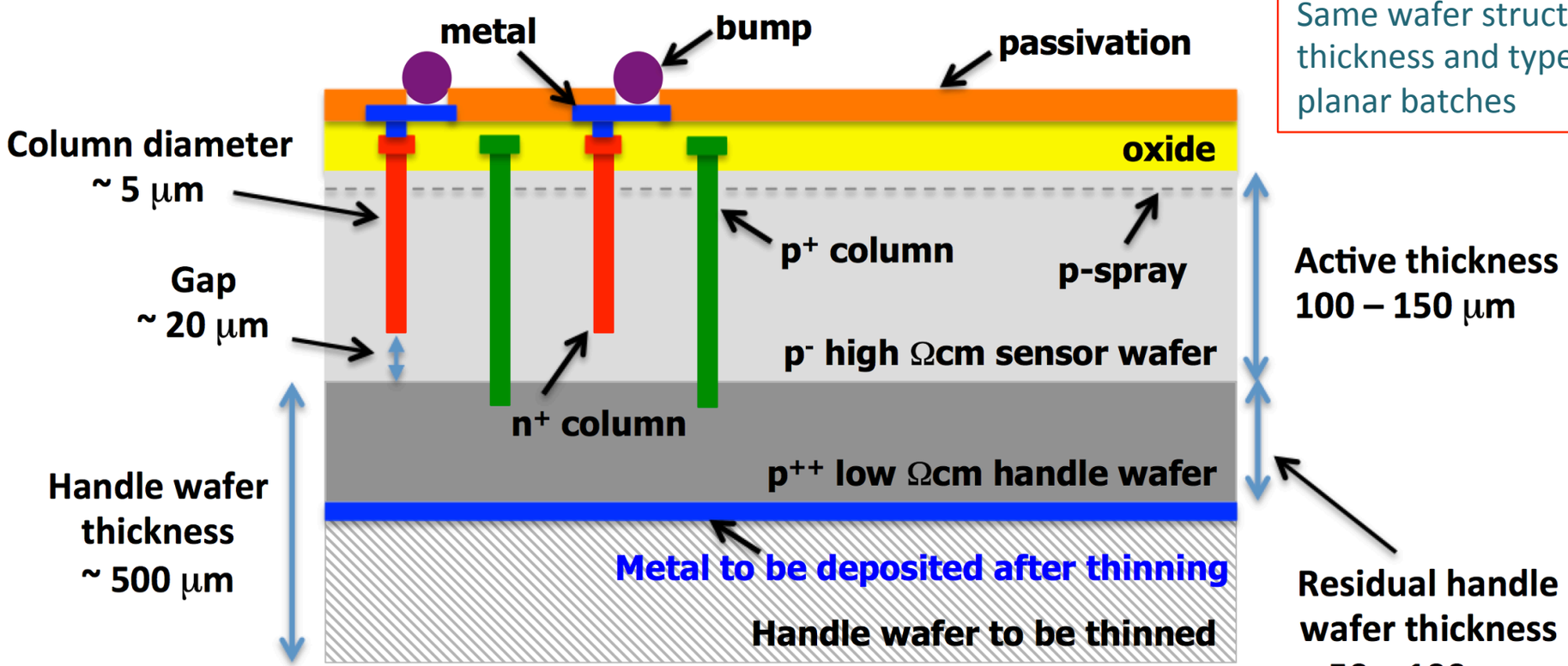
Sensori px 3D

Baseline per il primo layer del px di fase2

FBK: processo con lavorazione da un lato solo: tecnologia DRIE (Deep Reactive Ion Etching)
Provati vari disegni con

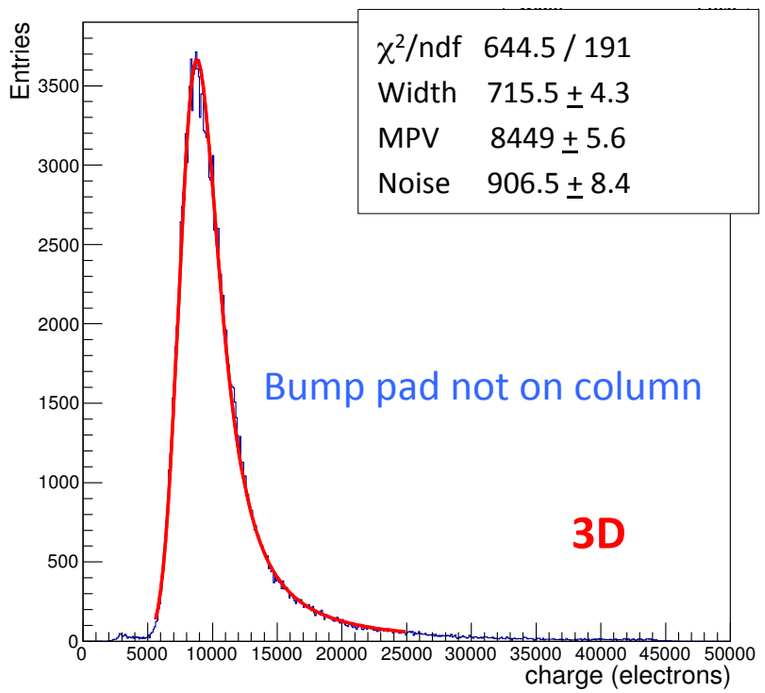
- numero vario di elettrodi collettori per cella
- differenti posizioni dei pad di bonding



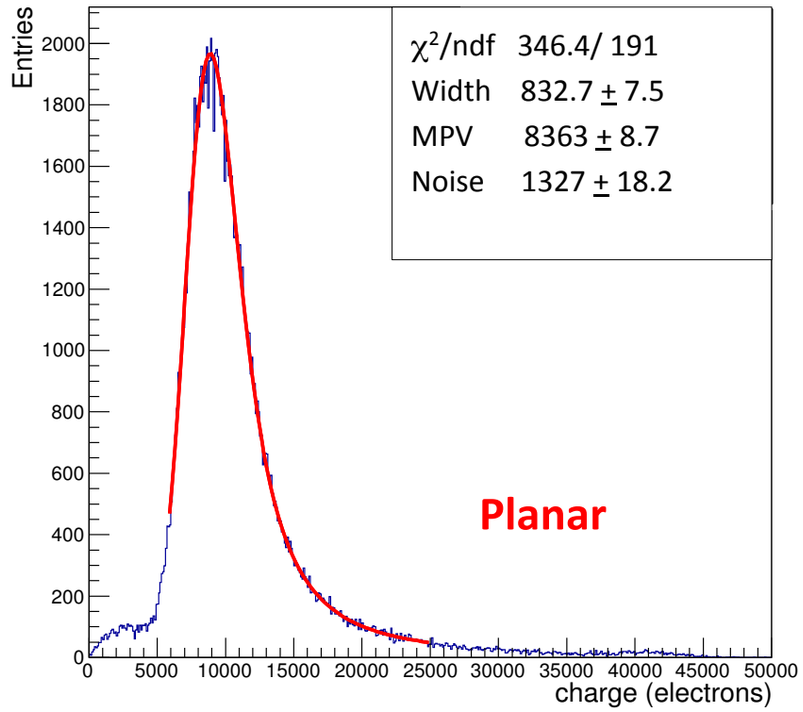


Same wafer structure, thickness and type as in planar batches

Planar and 3D prototypes on the same beam test session

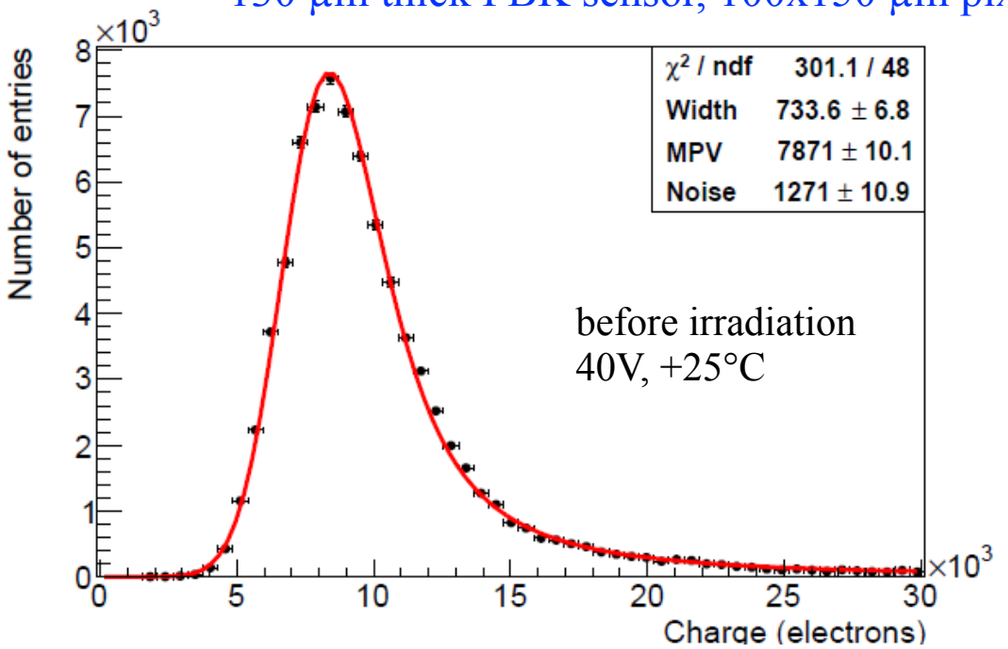


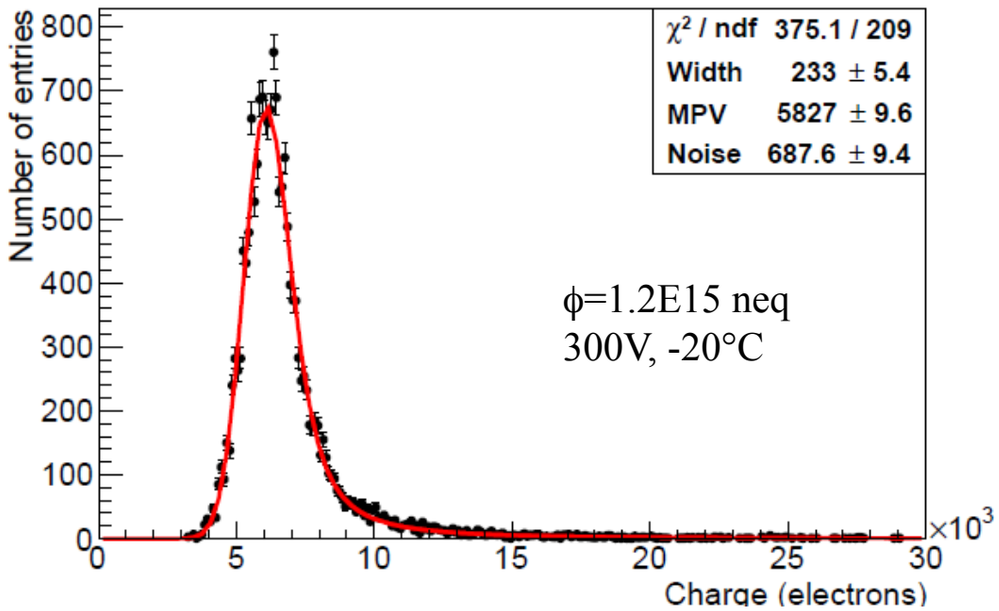
W76_1-56B (3D) – 2E 100x150 µm @40V



W75-1_2-63D (Planar) – 100x150 µm@90V

130 µm thick FBK sensor, 100x150 µm pixels

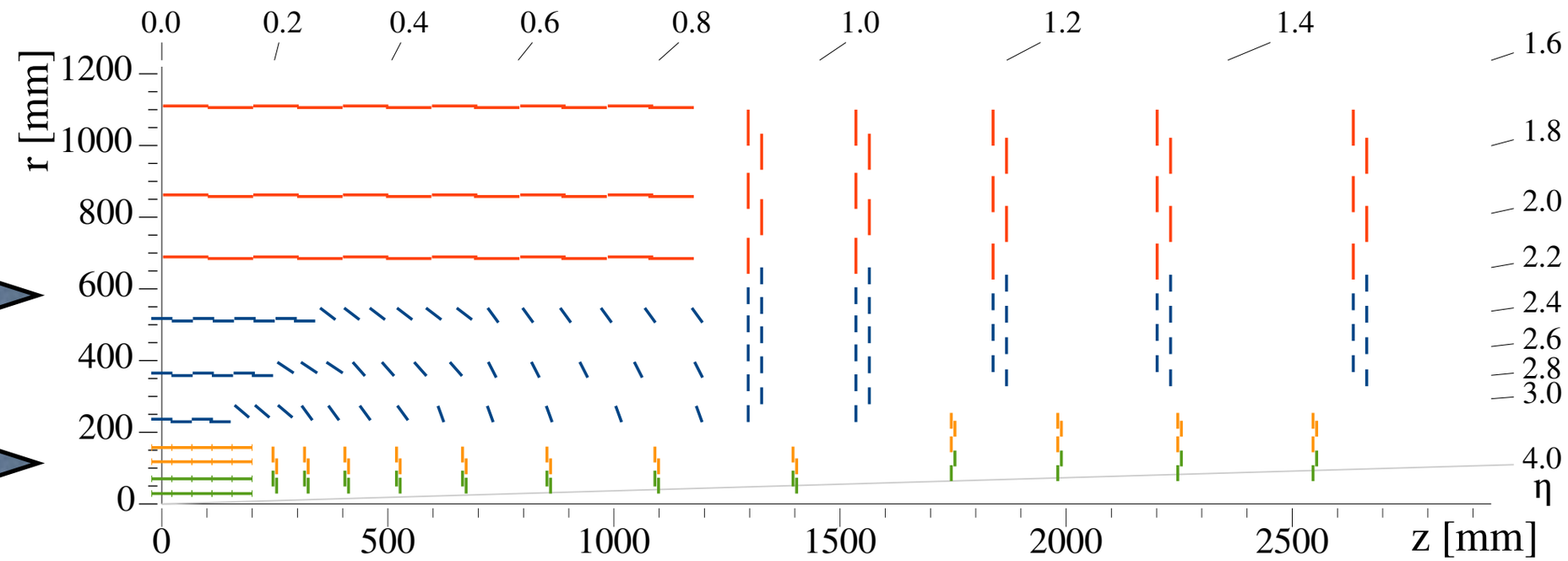




E l’alimentazione ?

~ 100 kW

~ 50 kW



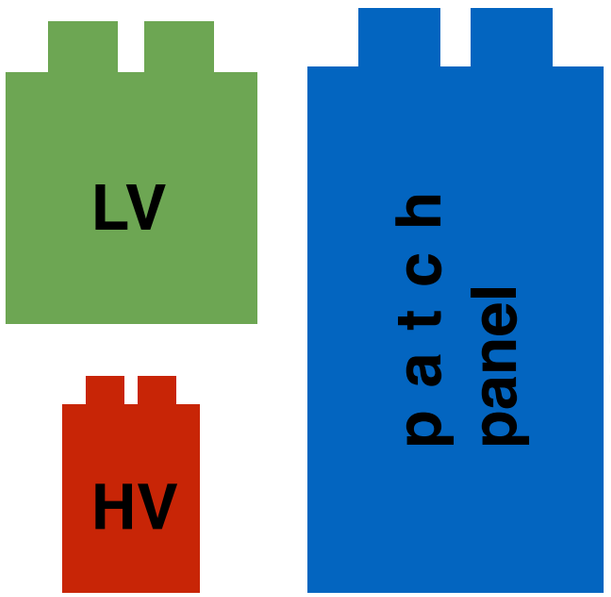
- **Richiesta di potenza ~ 3 x phase0**
- **Sezione rame dei cavi ~ invariata**

  → necessità di alzare la tensione cui viene fornita la potenza

OT: uso di convertitori DC/DC on detector

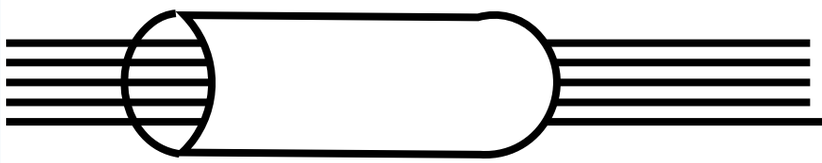
IT: schema di serial power

Possibile schema OT CMS

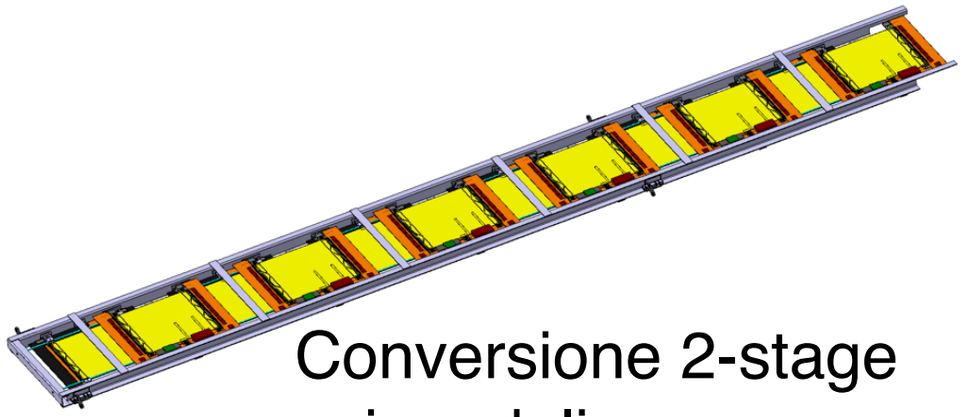


~ 12 x LV

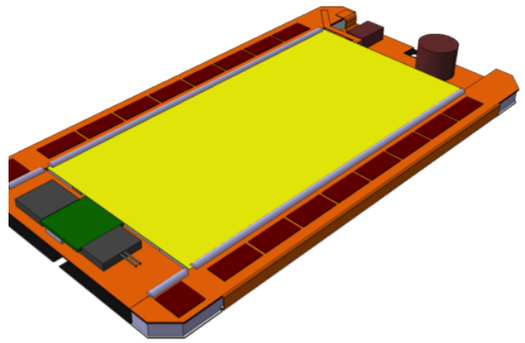
~ 12 x HV



~ 100 m



Conversione 2-stage sui moduli



~ 1300 canali di potenza, ~ 150 W/ch

~ 13000 fili LV da back-end a detector da gestire (monitoring, controlli)

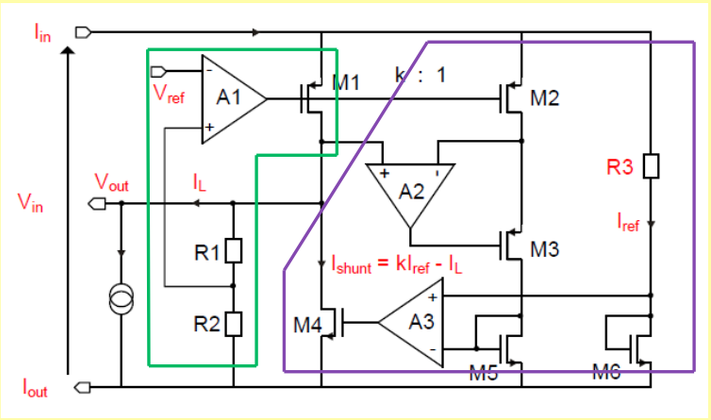
- Ubicazione ? (UXC/USC)
- Sezione dei cavi ?
- Compensazione della caduta sui cavi ?

~ 8 W per PS module

~ 5 W per 2S module

Inner Tracker: Serial Powering

- livelli di radiazione e vincoli di spazio e material budget escludono l'uso dei DC/DC sui moduli pixel
- l'opzione di base per ATLAS e CMS è uno schema di alimentazione in serie (SP)
- sviluppo in collaborazione tra ATLAS e CMS:
  - ✓ ATLAS parte dall'esperienza fatta col progetto IBL
  - ✓ FEI3, FEI4 sono dotati di circuito "shunt-LDO" e possono essere configurati per S.P.
  - ✓ in corso studi su SP utilizzando FEI4 in piccoli setup
  - ✓ prossimi tests su 65nm Shunt-LDO test chip irraggiati
  - ✓ shunt-LDO verrà incluso nel chip RD53

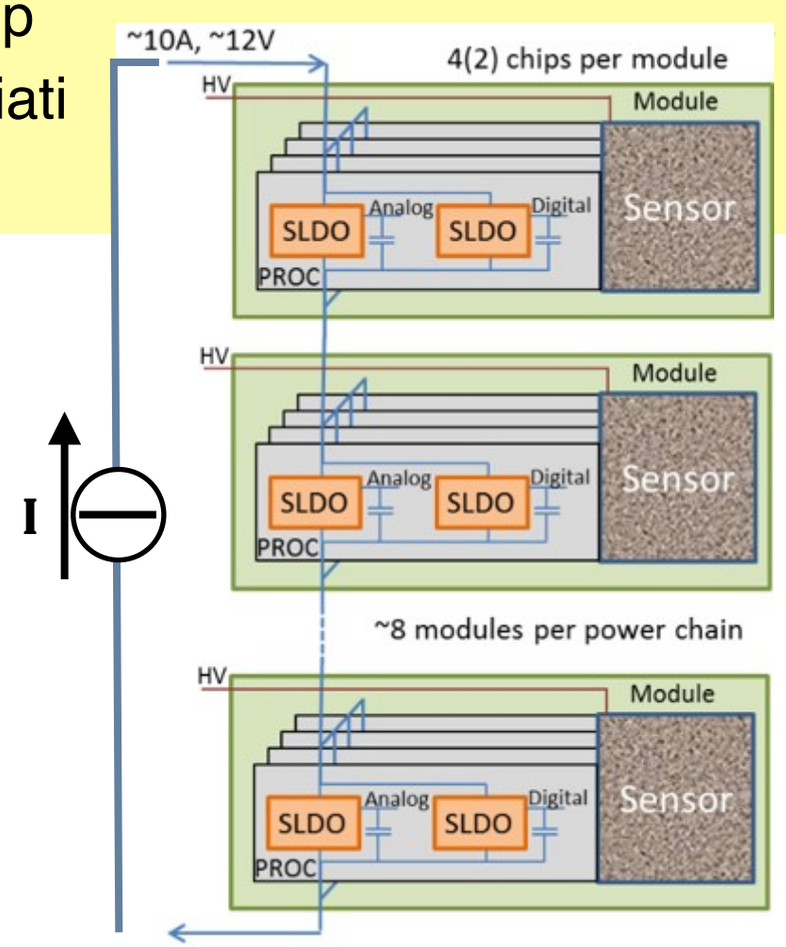


SHUNT-LDO. credits: M.Karagounis

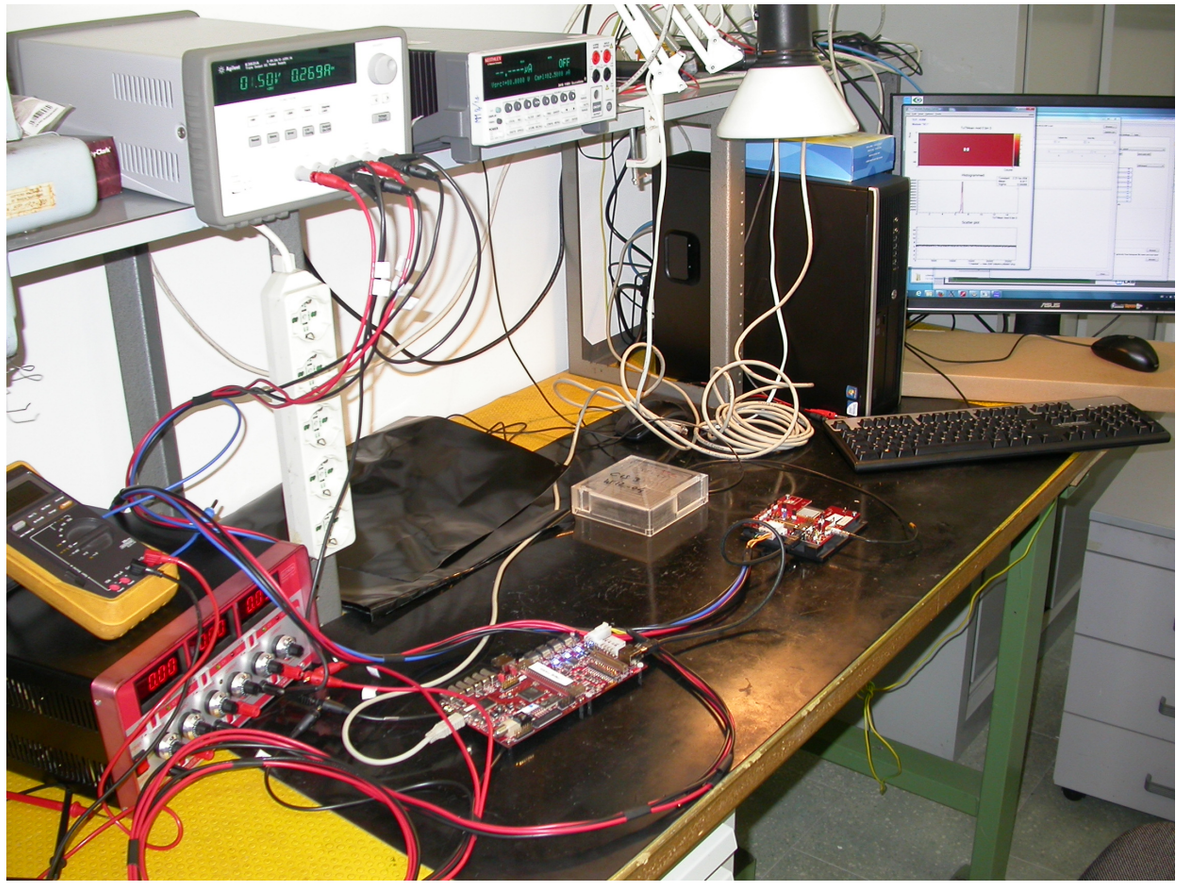
Possibile configurazione del sistema:

- ~500 power loops in corrente
- I ~ 10A
- V ~ 10-20 V

Collaborazione INFN-CAEN nell'ambito del progetto della Regione Toscana NEOLITE per lo sviluppo di una sorgente di corrente

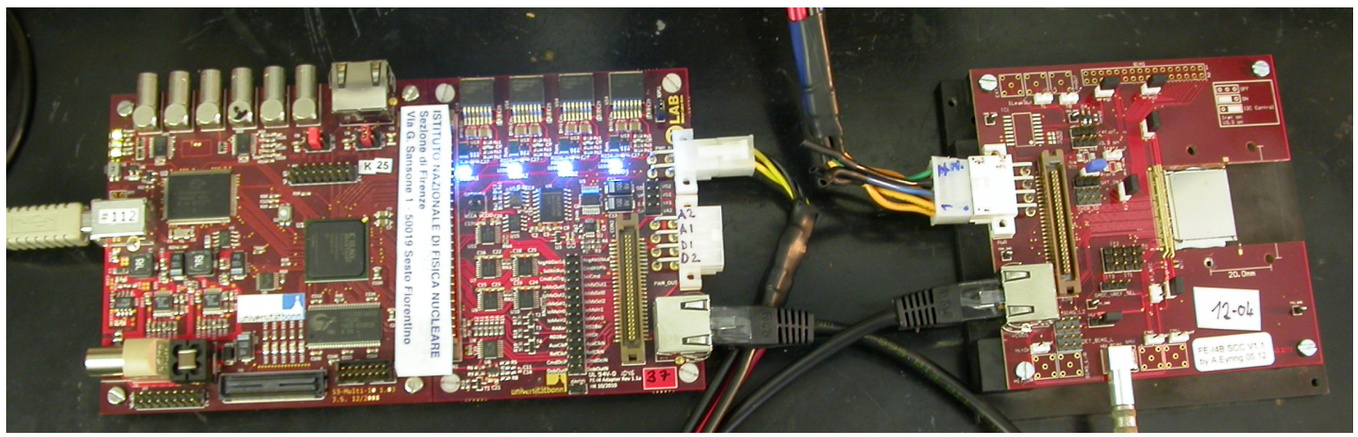


Tests con chip FE-I4

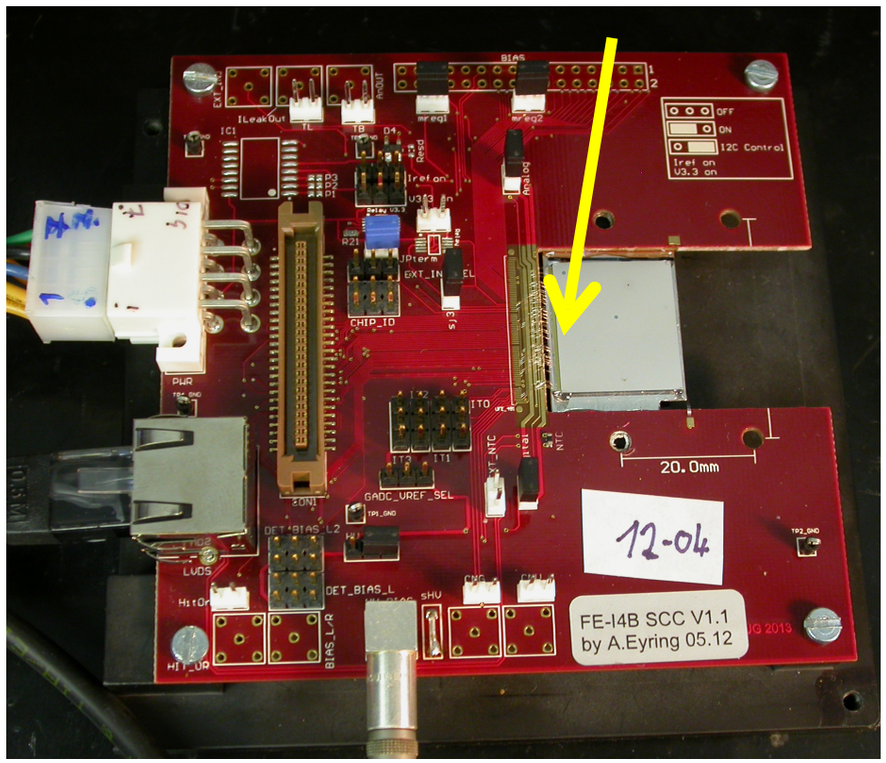


In attesa del chip di fase2 di RD53:

- Studio di configurazioni “Serial Power” per i pixel di fase-2 con Shunt-LDO (uno schema circuitale che permette il collegamento in serie dei chip).
- Tests con FE-I4 (il chip di ATLAS)
- Collaborazione col gruppo di Bonn di ATLAS



FE-I4

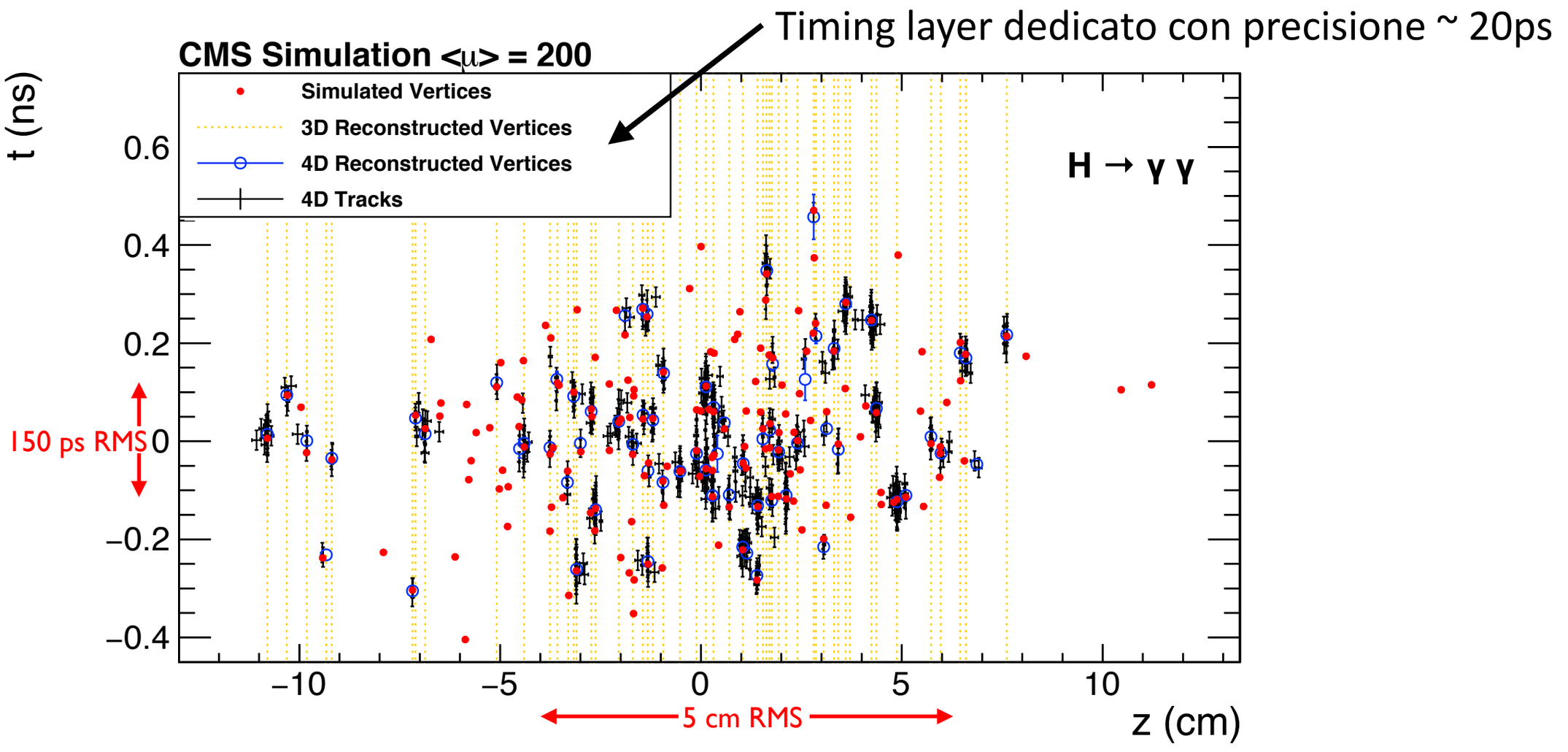


Timing Layer

Timing detectors

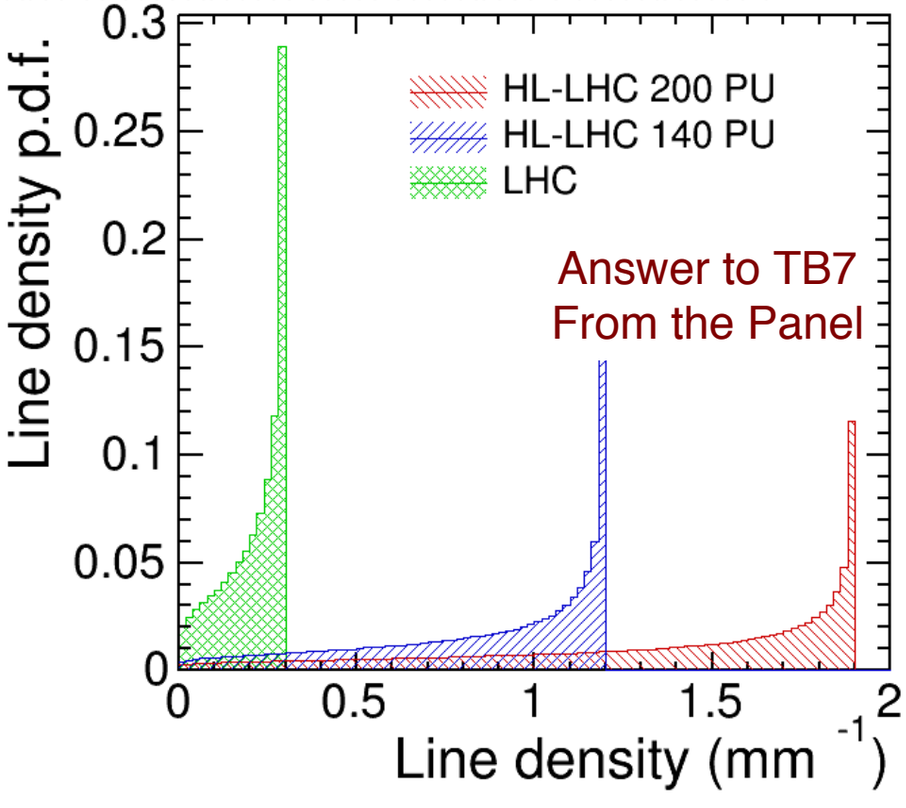
- <PU> ~ 200 pone seri problemi a livello di identificazione dei vertici
  - peggiore risoluzione calorimetrica (contaminazione da particelle provenienti da altri vertici) → MET degradata
  - ridotta efficienza nell'associare vertici ai γ (esempio: canale H → γ γ)

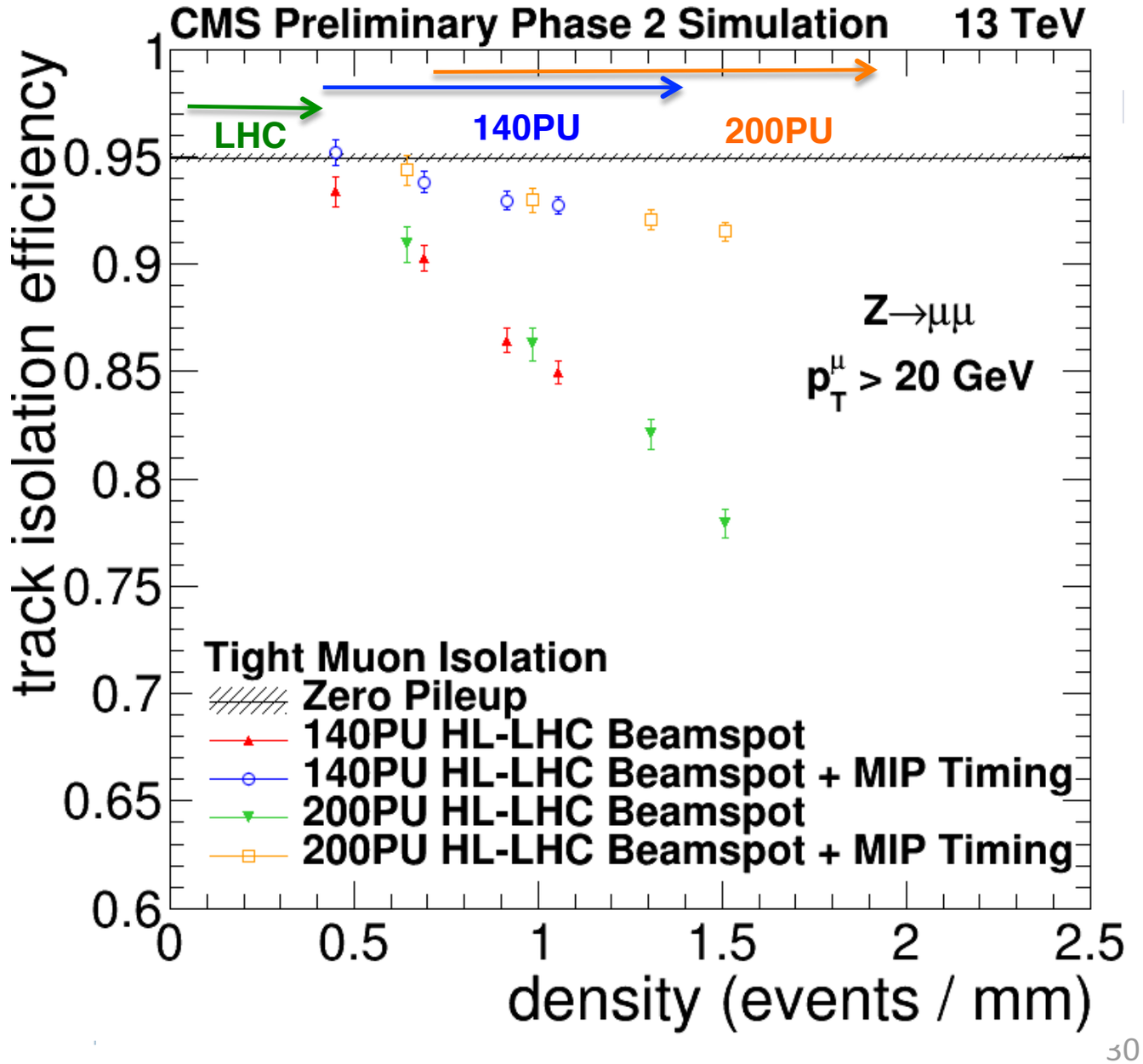
- CMS vuole ridurre l'effetto del PU sfruttando l'informazione temporale (ordine 30 ps) data da:
  - Calorimetri ECAL (γ), HGCAL (HEH + γ)
  - New MIP Timing Layer (barrel + endcal)
    - ✓cristally LYSO con lettura veloce (SiPM) barrel
    - ✓rivelatori al Si con guadagno interno endcap
- Riduzione effetti PU di fattore 4-5



. *“Precursor to a proposal” for the Phase II timing upgrade*

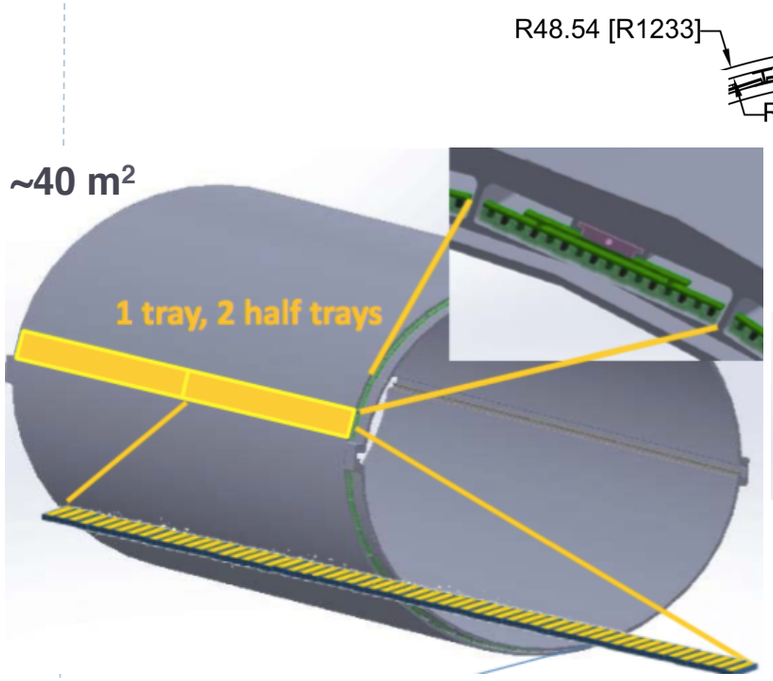
. *Report positivo da parte di un apposito CMS Review Panel*

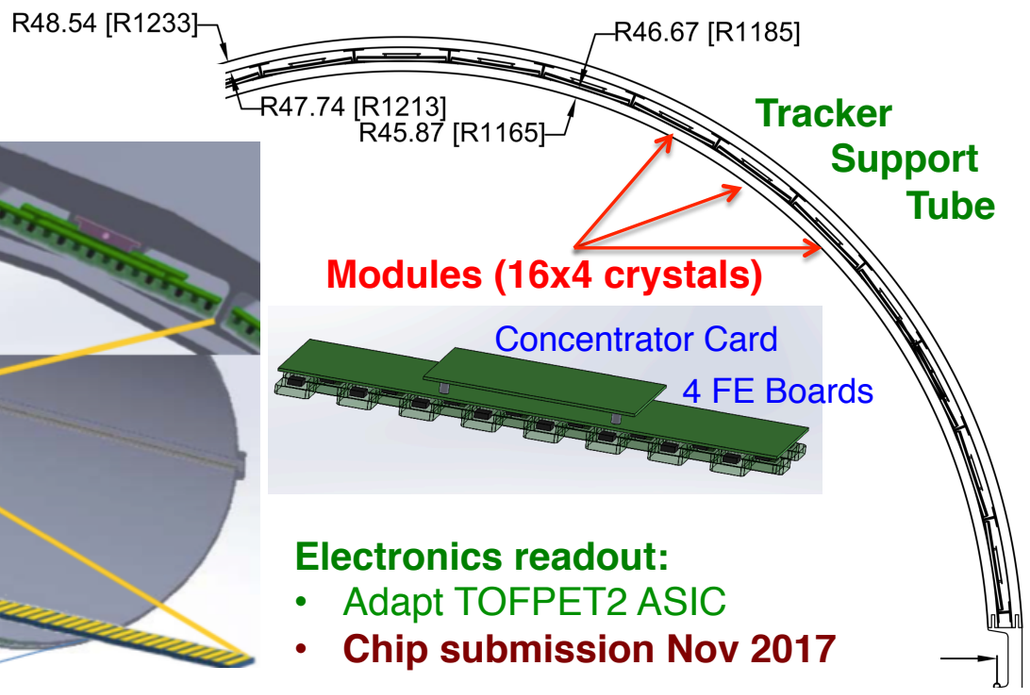




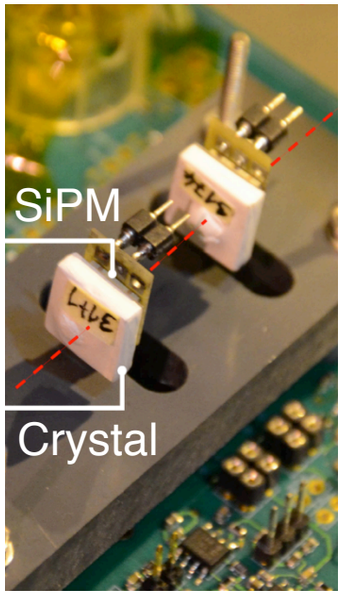
Barrel MIP Timing Detector

- **LYSO crystals + SiPM embedded in the Tracker tube**
  - Ready before TK integration (mid 2022)
  - Maintain performance at radiation level **$2x10^{14}$ n_{eq}/cm^2**





Electronics readout:
- Adapt TOFPET2 ASIC
- **Chip submission Nov 2017**



- **Nominal geometry: 12 x12 mm^2 (~ 3 mm thick) + 4x4 mm^2 SiPMs**
- **Production-like geometry qualified in test beams**
- **Good radiation hardness of production-ready SiPMs**
  - Operate SiPMs at ~ –30 ^{0}C (self-heating and dark rate)

Endcap MIP Timing Detector

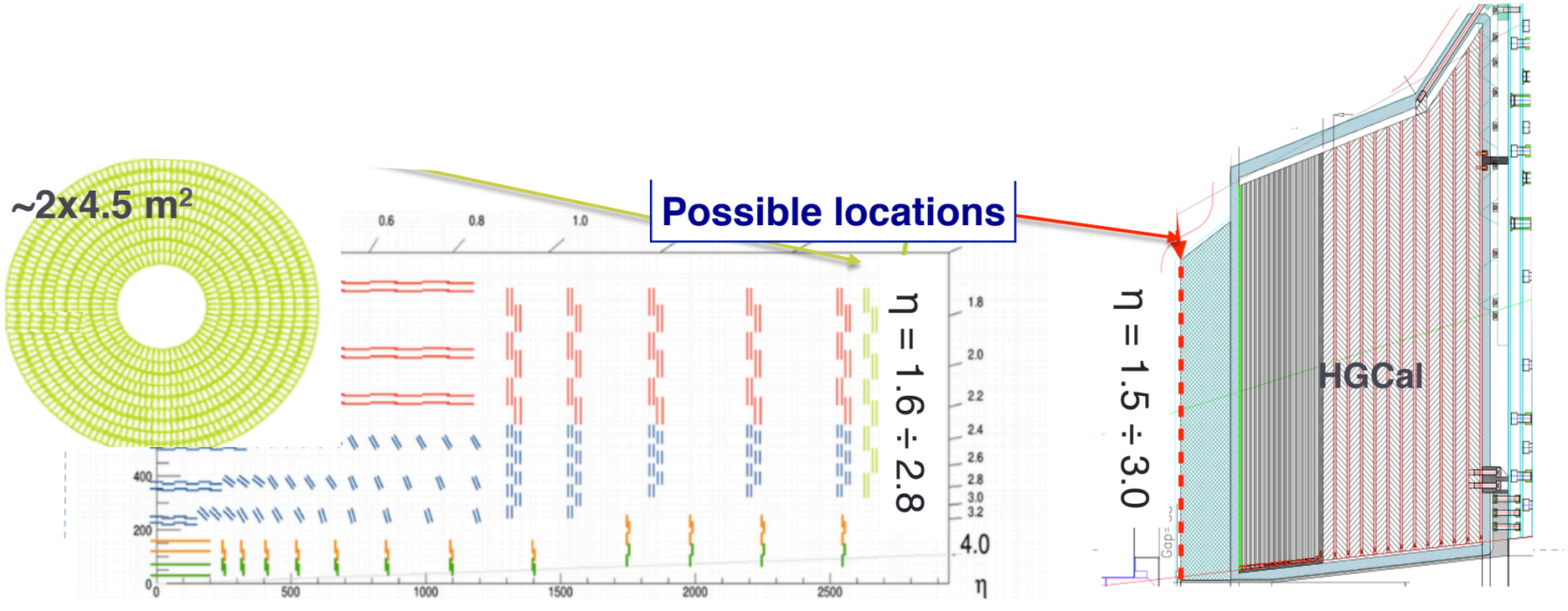
Endcap sensors (ultra-fast Si detectors)

Nominal geometry: 4.8 x 9.6 cm^2 modules with 1x3 mm^2 sensors

- 16 ASICs bump-bonded to sensors
- 3:1 ganging in the TDC at small η (3x3 mm^2 granularity)

Single sensors shown to have $\sigma_t \leq 50$ ps up to 10^{15} n_{eq}/cm^2

Readout ASIC in development



Conclusioni

- Nei prossimi anni LHC incrementerà progressivamente la luminosità, raggiungendo dopo il “Long Shutdown 3” (circa 2024) valori fino a 10 volte superiori alla luminosità nominale (1.E34 Hz/cm2)
- CMS opererà in condizioni sperimentali caratterizzate da alto rate, alto "pile up”, elevato livello di radiazioni e ha predisposto un programma di aggiornamento dei rivelatori:
  - sostituzione completa dei rivelatori maggiormente esposti alla radiazione (TRK + HGCAL)
  - Potenziamento del sistema di trigger:
    - ✓750 kHz L1 rate, 12.5 μs latency
    - ✓aumento complessità algoritmi di trigger
    - ✓elettronica “on detector” aggiornata, conversione digitale on detector a 40 MHz ed invio al back end tramite link ottici veloci
    - ✓utilizzo del tracciatore già a livello 1
  - Potenziamento delle regioni ad alto η con rivelatori a μ innovativi più veloci e segmentati (MicroMegas/GEM/iRPC)
  - Misure contro il PU:
    - ✓rivelatori più segmentati
    - ✓sviluppo di MIP Timing Layer

Backup

Title Text

Parameter	Nominal	HL-LHC
Bunch population N_b [10^{11}]	1.15	2.2
Number of bunches	2808	2748
Beam current [A]	0.58	1.12
Stored Beam Energy [MJ]	362	677
Full crossing angle [μrad]	285	590
Beam separation [σ]	9.9	12.5
Min β^* [m]	0.55	0.15
Normalized emittance ε_n [μm]	3.75	2.5
r.m.s. bunch length [m]	0.075	0.081
Virtual Luminosity (w/o CC) [10^{34} $cm^{-2}s^{-1}$]	1.2 (1.2)	21.3 (7.2)
Max. Luminosity [10^{34} $cm^{-2}s^{-1}$]	1	5.1
Levelled Pile-up/Pile-up density [evt. / evt./mm]	26/0.2	140/1.25

ATLAS, upgrade di fase2

Front End upgrade:

- Elettronica LAr (FE+BE): streaming di tutti i dati con digitizzazione “on detector” a 40/80 MHz
- Elettronica del Tile Cal.

ITK

Nuovo tracciatore interno interamente al silicio. Layout da finalizzare. Copertura fino a η=4

Strips:

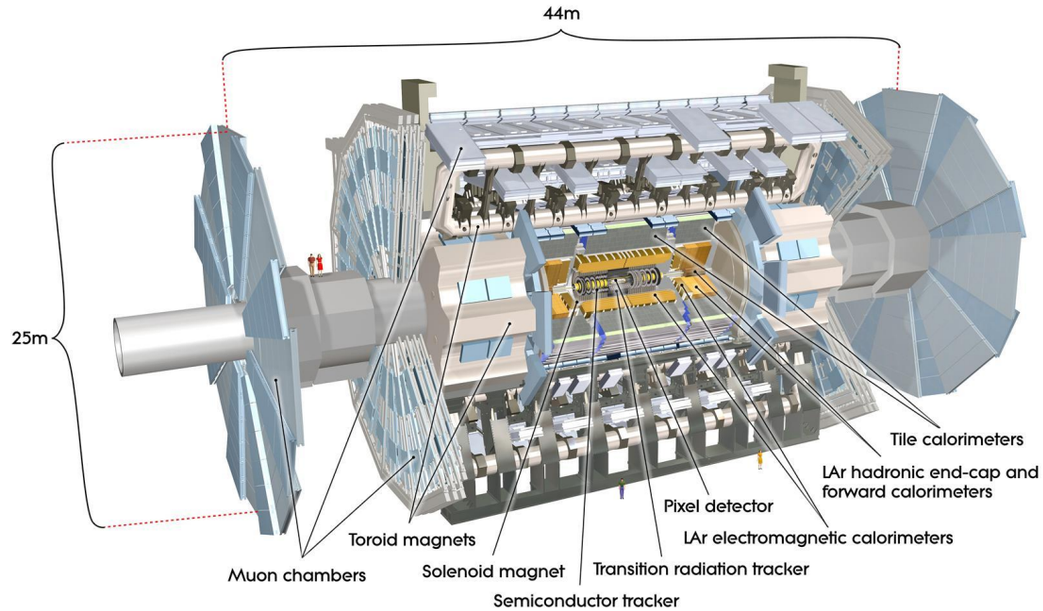
- 4 layers barrel, 6+6 layers endcaps, moduli doppia faccia
- sensori n-in-p (p-stop) spessi 320μm.
- Lettura digitale tramite “ABC130” (130 nm CMOS) con doppio buffer. Supporta varie modalità trigger: acquisizione di tutti i dati (L0), oppure su richiesta del L1 (L0/L1), oppure priorità ai dati relativi alla regione di interesse (ROI) (L0/R3/L1).
- Alimentazione: DC/DC converter sul rivelatore

pixels:

- 5 layers barrel, vari layers endcap
- varie opzioni ancora aperte per la scelta della tecnologia dei sensori

Nuovo TRIG/DAQ

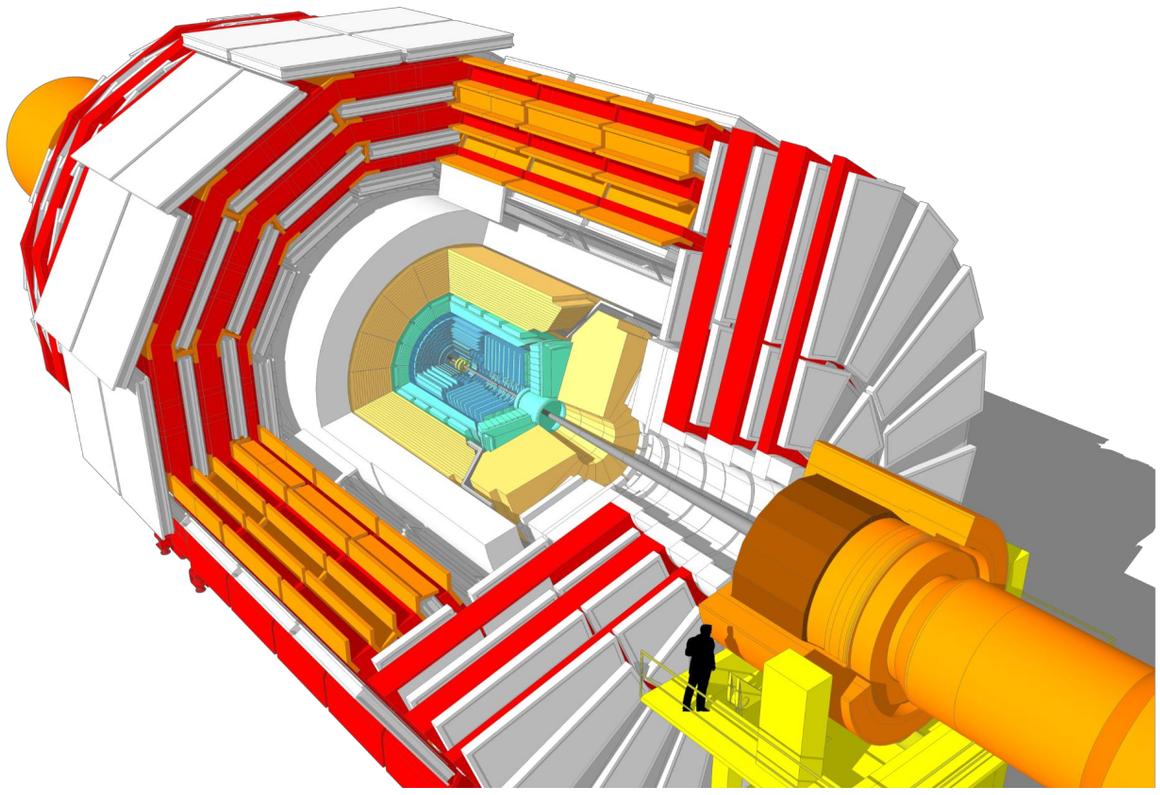
- L0 [Calo+muon] @1MHz
- (opzionale: L1 [Calo+Muon+ITK])
- Tracker@L1 → high rate regional tracking (pt > 4 GeV)
- FTK++ → tracking completo a HLT



Camere a muoni

- Nuova elettronica r/o per RPC e TGC
- Nuova elettronica r/o per MDT (L1)
- Nuove “thin-gap” RPC + sMDT (30mm → 15mm) nel layer più interno del barrel
- high-η tagger per coprire fino a |η|=4

CMS, upgrade di fase1



TRIGGER L1.

Elettronica “back end” rinnovata (sistema modulare basato su FPGA). Trasmissione dati su fibra ottica.

Incrementati sostanzialmente:

- il flusso di dati e la granularità disponibili a L1
- complessità nelle decisioni L1 (es. τ ID)
- migliore integrazione del sistema *μ*
- sottrazione PU sulle primitive calorimetriche

pixel

- 4 layer, 3 dischi
- pronto per operare @ 2E34 Hz/cm2

Rivelatori *μ*:

- YE4 → quarto endcap *μ* (CSC, RPC) durante LS1
- DT: sostituita l’elettronica sulle camere (minicrate). ROS (readout server) e TSC (trigger sector collector) spostati in USC. Segnale digitalizzato sulle camere e trasferito via link ottico in USC.

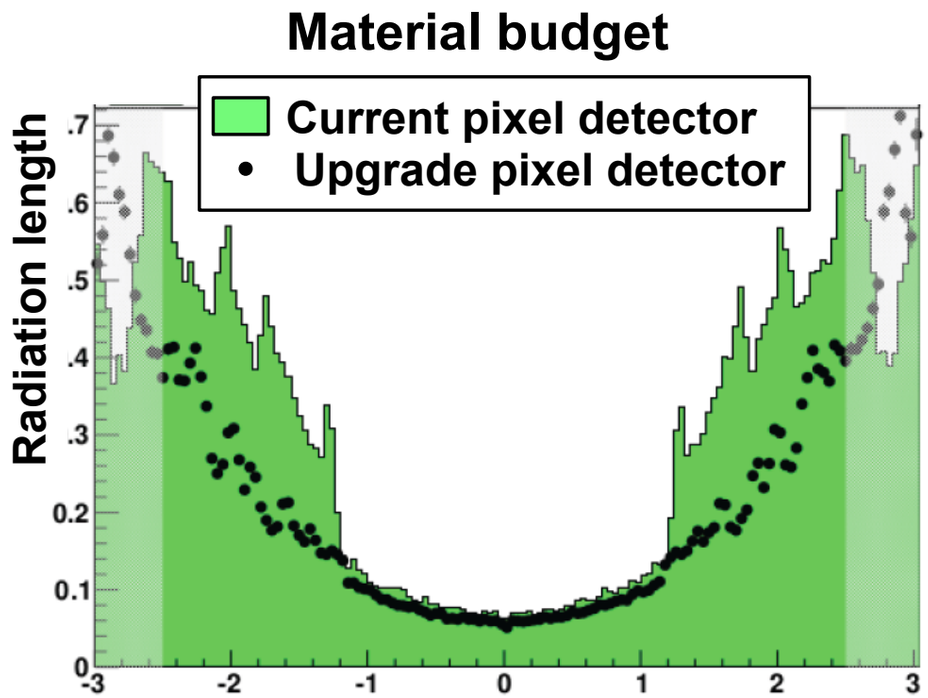
HCAL (HB, HE, HO):

- nuovi fotorivelatori (SiPM al posto di HPD)
- elettronica “Front End” + “Back End” rinnovata

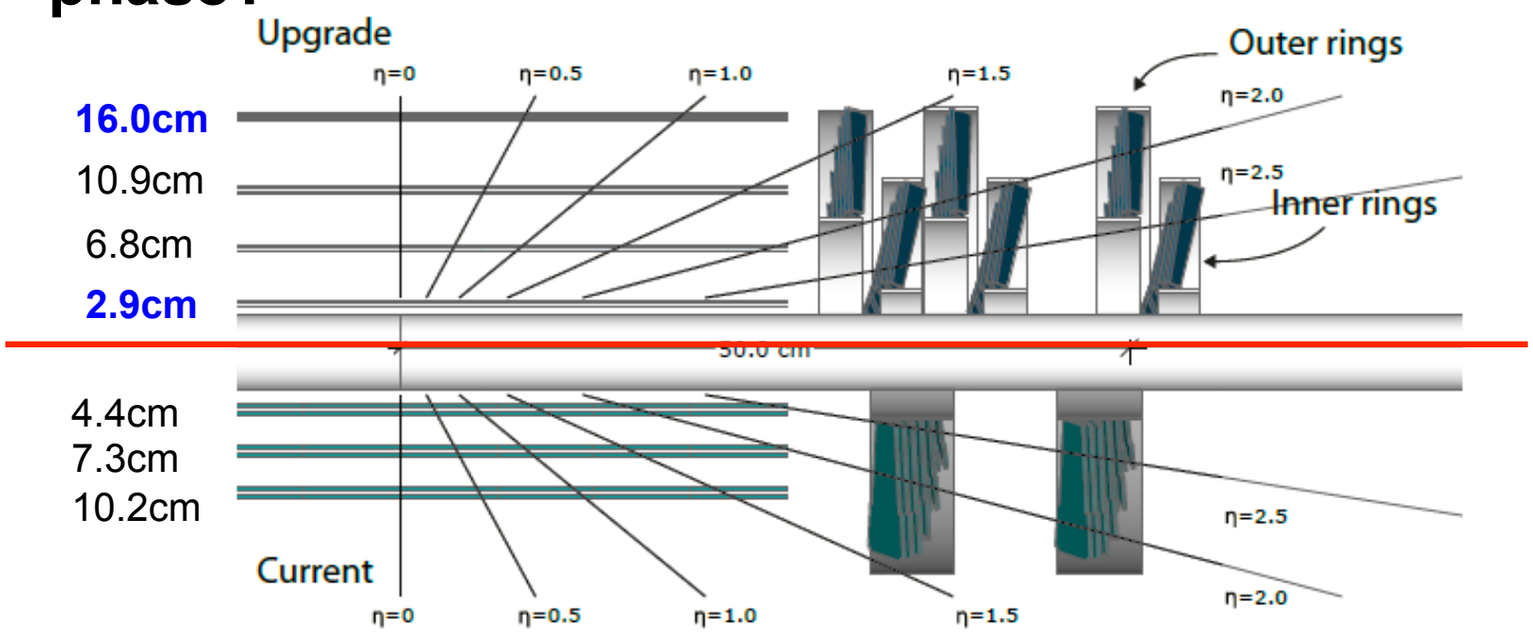
- HF:
  - nuovi fotorivelatori: MA-PMT al posto dei PMT

Il rivelatore pixel di fase1 di CMS

- necessario per operare efficientemente alle luminosità previste per il RUN3 (~ 2.0 E34 Hz/cm2), fino a L_int~500 fb^{-1}
- accettanza estesa:
  - 4 layer barrel, 3 dischi → migliorata risoluzione in IP e efficienza HLT
- riduzione material budget → nuova meccanica di supporto e nuovi servizi:
  - DC-DC power, μ-channel cooling bifase a CO_2



phase1



current

- sensori n^+-in-n 100x150 µm2
- r/o chip con tecnologia a 0.25µm:
  - FPIX e layers 2,3,4 di BPIX: PSI46dig (fino a 120 MHz/cm2)
  - BPIX layer 1: PROC600 (fino a 600 MHz/cm2)