INFN-Melbourne collaboration on Associative Memory and track trigger systems

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Associative Memory in Particle Physics

- Use of the Associative Memory technology in hadron collider experiments was first conceived by two Italian scientists working on the CDF experiment at Fermilab late 1980s
- Fast pattern recognition by the simultaneous look-up of patterns stored in the emerging (at that time) VLSI technology

VLSI STRUCTURES FOR TRACK FINDING

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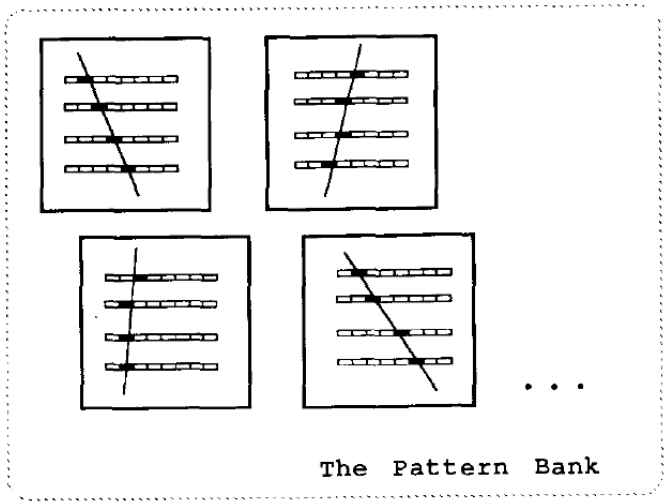
Received 24 October 1988

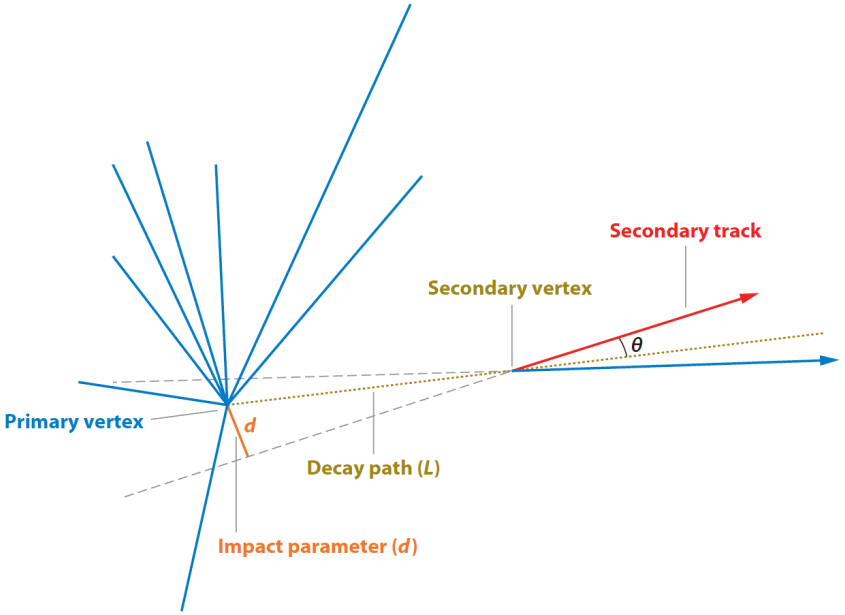


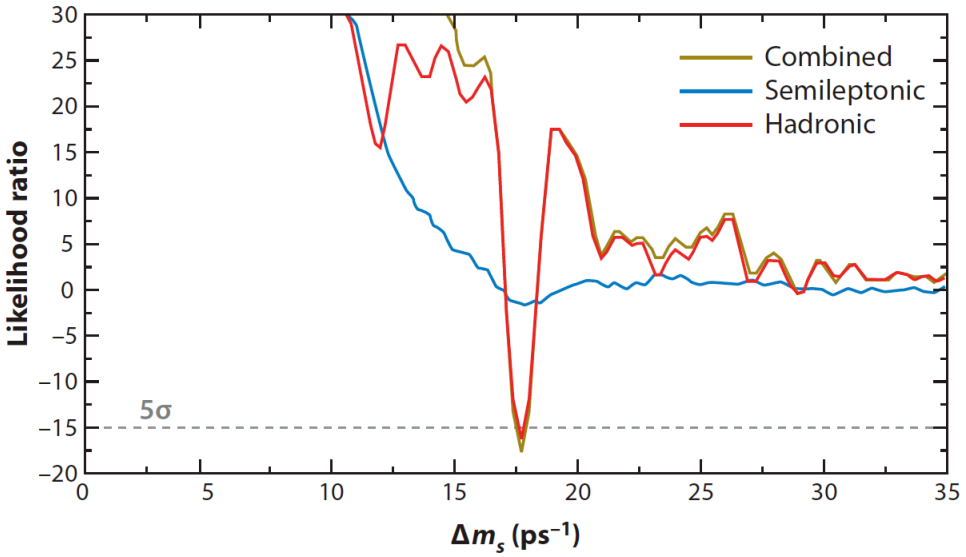
We discuss the architecture of a device based on the concept of *associative memory* designed to solve the track finding problem, typical of high energy physics experiments, in a time span of a few microseconds even for very high multiplicity events. This "machine" is implemented as a large array of custom VLSI chips. All the chips are equal and each of them stores a number of "patterns". All the patterns in all the chips are compared in parallel to the data coming from the detector while the detector is being read out.

Nucl. Instrum. Meth. A 278, 436-440 (1989)

Silicon Vertex Trigger (SVT) at CDF

- Associative Memory chip (AMchip) is employed in the trigger electronics of Silicon Vertex Detector
- Realised a trigger purely based on the information of the impact parameters (the only realisation of this type of trigger in the history)
- Achieved measurements of e.g. B_s oscillation frequency and CP asymmetry in the charmless B_d, B_s and Λ_b decays possible, which would have been impossible without SVT



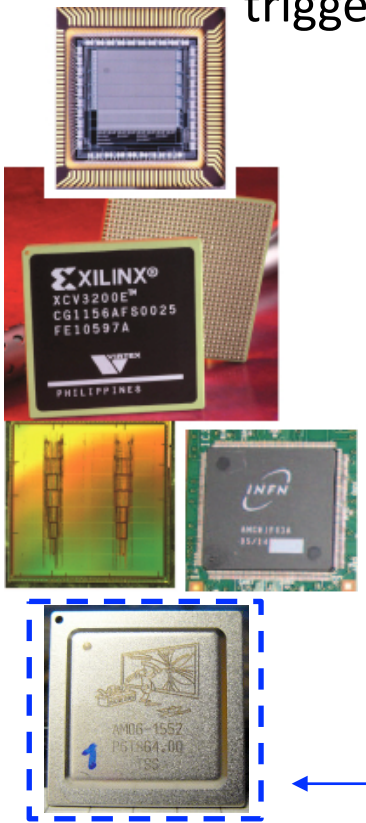


Annu. Rev. Nucl. Part. Sci. 2010.60:595-614

Phys. Rev. Lett. 103 031801 (2009)

AMChip development

- AMchip has been developed by INFN (CDF, ATLAS)
  - Based on the **Content-Addressable Memory (CAM)** technology
  - Comparison of input data with **pre-computed patterns stored in it**
  - Maximum level of **parallelisation with high-density memory** to deal with ever increasing hit occupancy and ever decreasing latency of the trigger system of hadron collider experiments

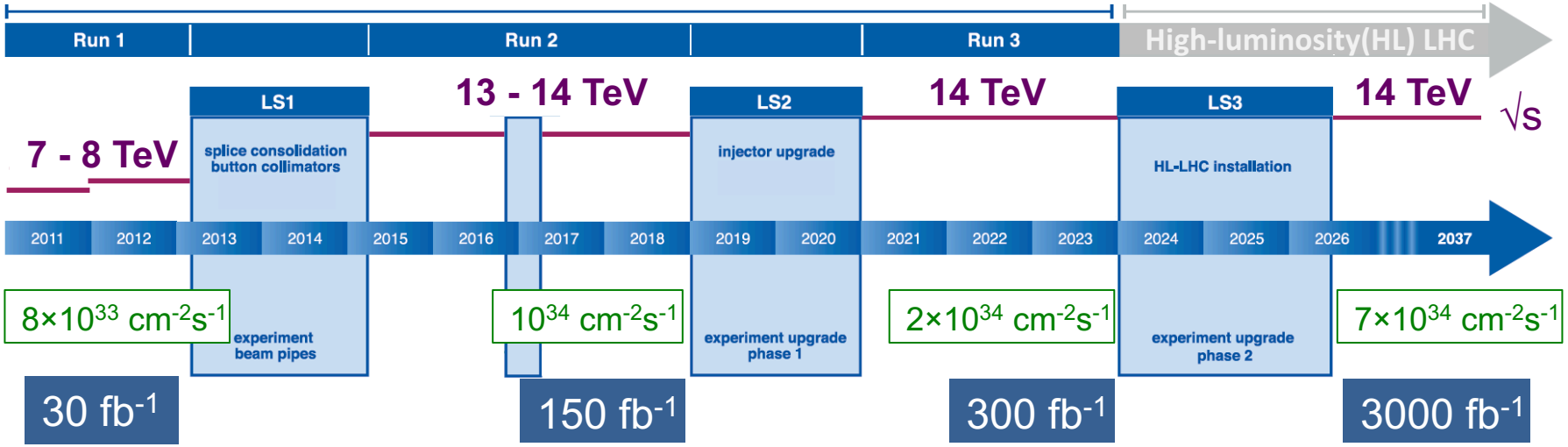


Vers.	*Design*	*Tech.*	*Area*	*# Patt.*	*Package*
1	full custom	700 nm		128	QFP
2	FPGA	350 nm		128	QFP
3	std cells	180 nm	100 mm^2	5k	QFP
4	std cells + full custom	65 nm	14 mm^2	8k	BGA
5	std cells + full custom + IP blocks	65 nm	12 mm^2	3k	BGA
6	std cells + full custom + IP blocks	65 nm	168 mm^2	128k	BGA

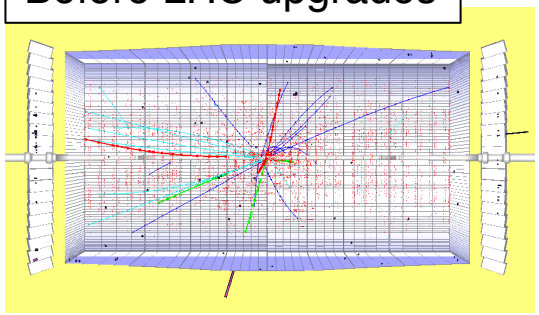
AM06 is the core of the Fast TraKer (FTK) in the ATLAS experiment

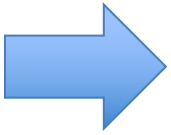
LHC upgrades

- Ambitious upgrade program of LHC's energy and luminosity
  - First go to design energy ($\sqrt{s}$ = 14 TeV) and luminosity (L = 10^{34} $cm^{-2}s^{-1}$)
  - Obtain *O*(100) more data with the High-Luminosity LHC (**HL-LHC**)
  - …more occupancy due to the increased pileup collisions

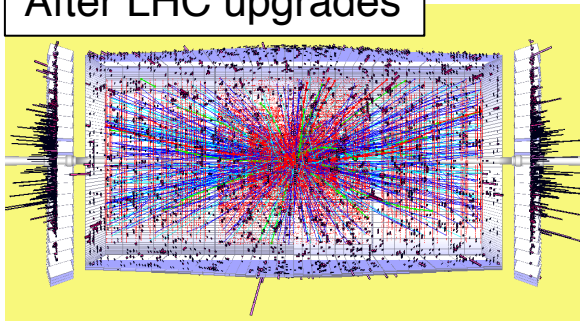


Before LHC upgrades



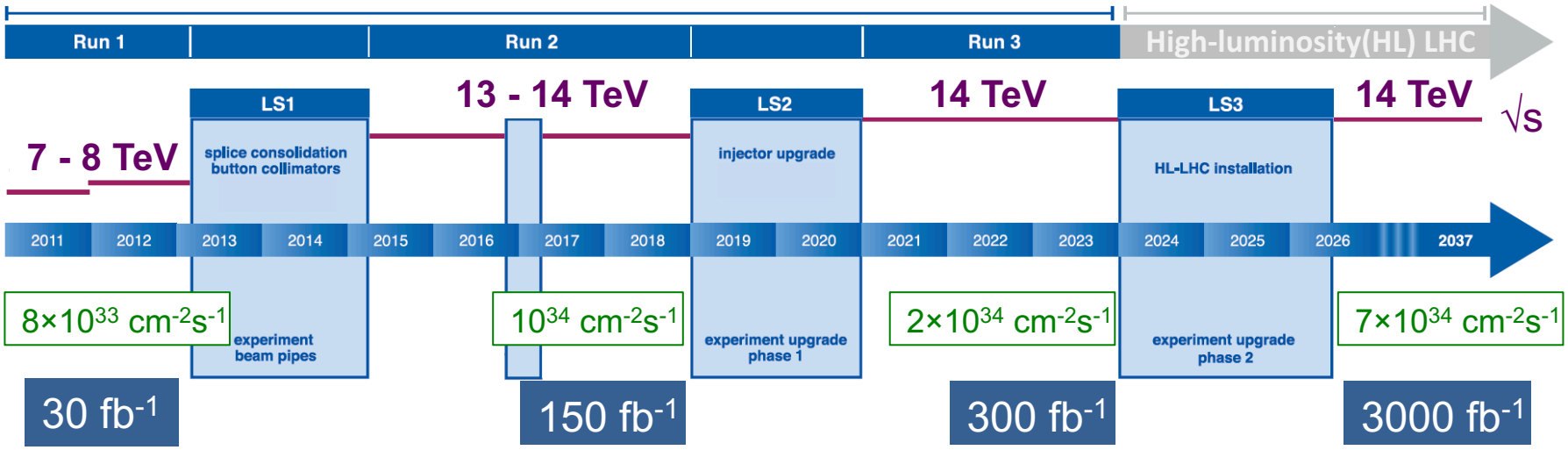


After LHC upgrades



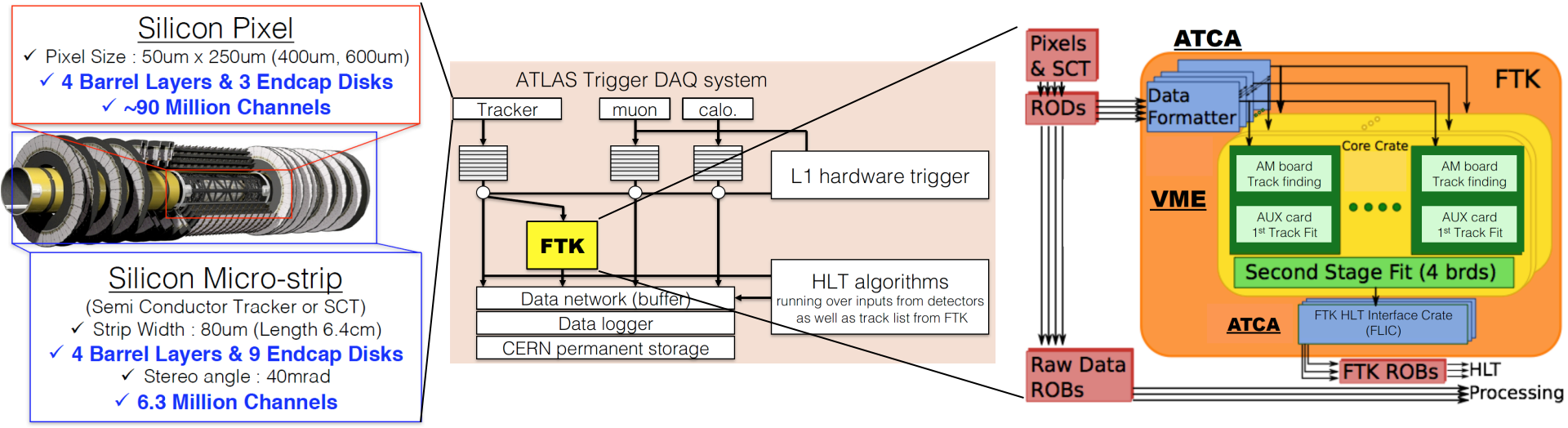
AMchip applications in LHC upgrades

- **Fast TracKer (FTK) system in ATLAS**
  - Currently being commissioned into the ATLAS trigger system
  - Will operate by the end of 2023
- **Phase-II detector upgrade for HL-LHC**
  - Full scan track trigger system in ATLAS and CMS
  - Region-of-Interest based track trigger system in ATLAS
  - Muon tracking trigger system in ATLAS



FTK system in ATLAS

- Electronics system which reconstructs all tracks with p_T > 1 GeV in all events passed Level-1 trigger within O(100 μs)
- Access to track information will help trigger algorithms to retain high efficiency and reject background
  - Charged lepton, b-tagging, τ-tagging, missing E_T and jet reconstruction
- Sustainable INFN-Melbourne collaboration with researchers from INFN Pisa
  - Paola Giannetti, Mauro Dell'orso, Alberto Annovi (former FTK project leader), Chiara Roda



Melbourne contributions to FTK

- **Commissioning of the AMBoard at CERN (TK)**
  - Took the role of the contact person at CERN in 2015

- **RunControl software of the AMBoard (TK)**
  - Responsible for the AMBoard operation software
- **Online (TK) and offline (Noel Dowe) monitoring of FTK**
  - On-time comparison of the HW and SW track reconstruction
  - Development of the core offline software
  - Responsible for the nightly test system of FTK offline simulation

- **Development of Fast simulation of FTK (Federico Scutti)**
  - Critical for the stable MC production and hence physics analysis

- **Integration of FTK tracks in tau triggering chain (Daniele Zanzi)**
  - Responsible for tau-trigger






AMChip development for HL-LHC

	Technology	Area (mm^2)	Memory size (No. Mbits)	Power (fJ/comp/bit)	Speed (MHz)	I/O	For
AM06	65nm	160	19	2.3	100	serial	FTK (2016)
AM07	28nm	10	2.4	< 1.0	200	parallel	R&D (2017)
AM08	MWP with including full AM09 architecture & functions						R&D (2018)
AM09	28nm	~160	57 - 76	< 1.0	> 250	serial	HL-LHC (2020) large scale chip

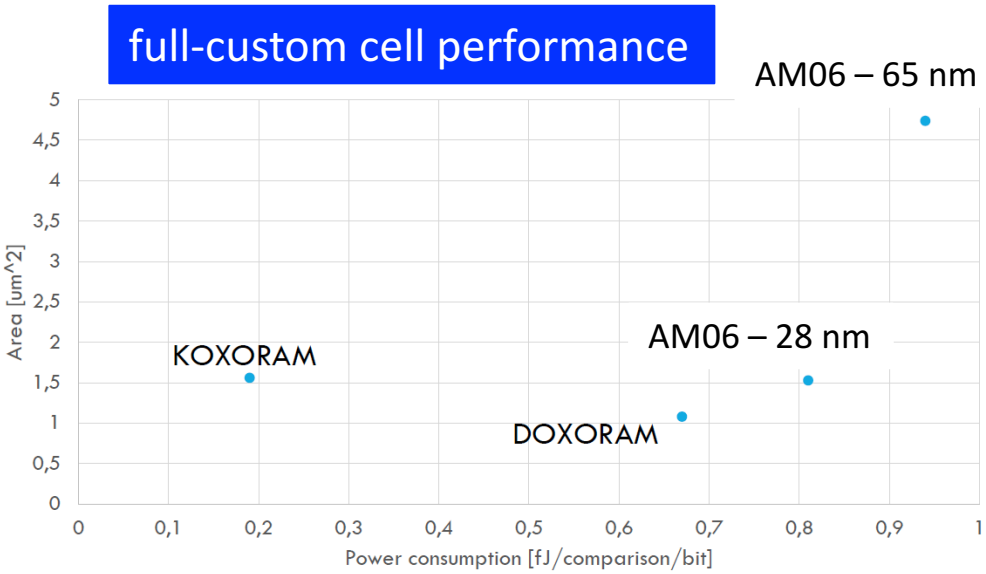
- **Goal: delivery of AM09 around 2020**
  - Memory density: at least three times higher than AM06
  - Power consumption: less than 1.0 fJ/comparison/bit
  - Clock frequency: faster than 250 MHz
- **AM07 project on-going**
  - Move from 65 nm to 28 nm CMOS technology (TSMC HPL)
  - New low-power & higher-density CAM cell designs
  - Test LVDS I/Os for the operation at 1 Gbps
  - **Design submitted → start characterising the chip in summer 2017**

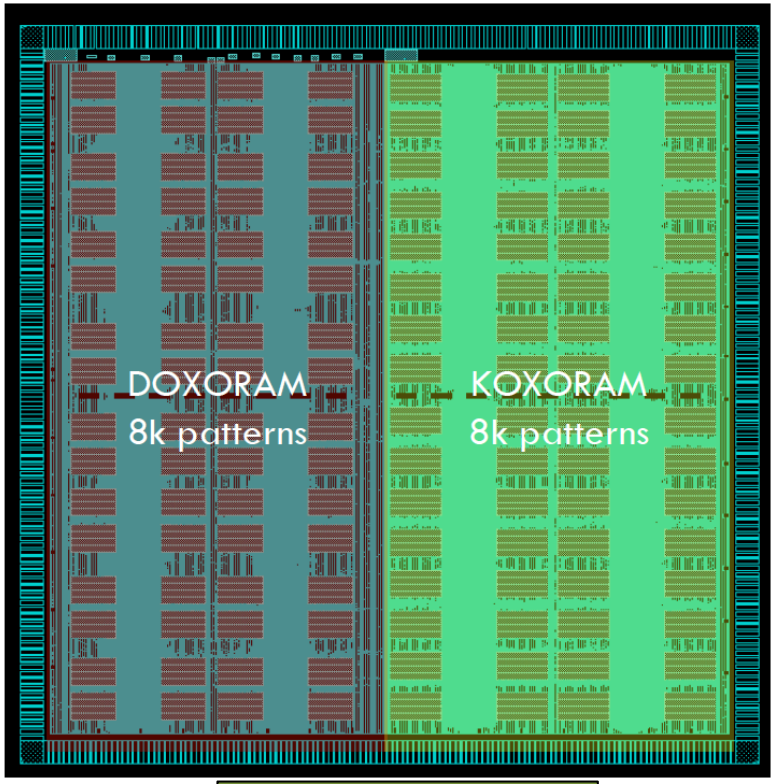
Collaboration of AMChip development

- INFN ***RD_FASE2 Track Trigger*** (INFN Pisa)
  - Alberto Annovi (coordinator of the ATLAS phase-II track trigger)
  - Fabrizio Palla (coordinator of the CMS phase-II track trigger)
- INFN ***IMPART*** (INFN Milan)
  - Alberto Stabile
  - Valentino Liberali
- ANR ***Fast Track*** (CNRS LPNHE)
  - Giovanni Calderini
  - Francesco Crescioli
- ARC ***Discovery Projects DP160100315*** (Melbourne)
  - Takashi Kubota
  - Elisabetta Barberio
  - Seyed Ruhollah (Jafar) Shojaii
    - Obtained PhD in Milan (2016)
    - Joined us from 2017

AM07 design performance

- Both full-custom layouts achieve about 4 times higher densities w.r.t. AM06
- Power consumption/comparison/bit is less than 1.0 fJ
- Melbourne is responsible for the hardware programming and validation of the front-end logic
- Jafar is instrumental in the (preparation of) AM07 chip characterisation





AMchip07 layout

MOCAST 2017

- International conference on **M**odern **C**ircuits **A**nd **S**ystems **T**echnologies
- 4 – 6 May 2017 in Thessaloniki, Greece (http://mocast.physics.auth.gr/)
- A special session for the AMchip development
  - A Low-Power and High-Density **Associative Memory** in 28 nm CMOS technology (T.K)
  - Pop-count Circuits for **Associative Memories**: a Comparison Study (L. Frontini (Milan))
  - Design of LVDS Driver and Receiver in 28 nm CMOS Technology for **Associative Memories** (F. De Canio (Bergamo))
  - Power Distribution Network Optimization for **Associative Memories** (V. Liberali (Milan))
  - A Software Demonstrator for **Cognitive Image Processing** Using the Associative Memory Chip (S. Gkaitatzis (AUTH))
- Plus two other AMChip related talks
  - Heterogeneous computing system platform for **high-performance pattern recognition applications** (V. Voisin (LPNHE))
  - Track Finding Mezzanine for **Level-1 Triggering in HL-LHC Experiment** (C. Gentsos (Perugia, AUTH))

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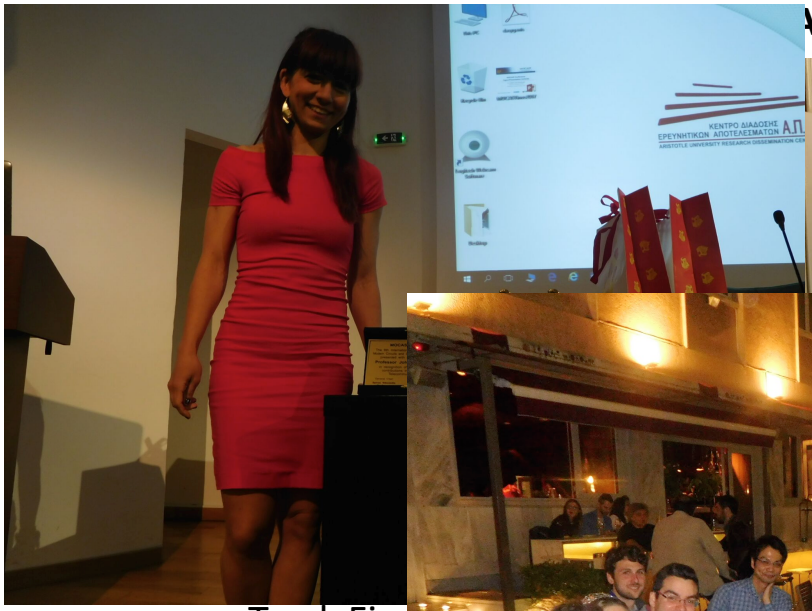


Associative Memory in 28 nm CMOS technology (T.K)

– Track Find
(Perugia,

Cognitive image processing

- Extract “meaningful patterns” at an early stage of the image processing
  - Reducing the amount of data to process
  - Keeping the image “identifiable” (or increasing identifiability)

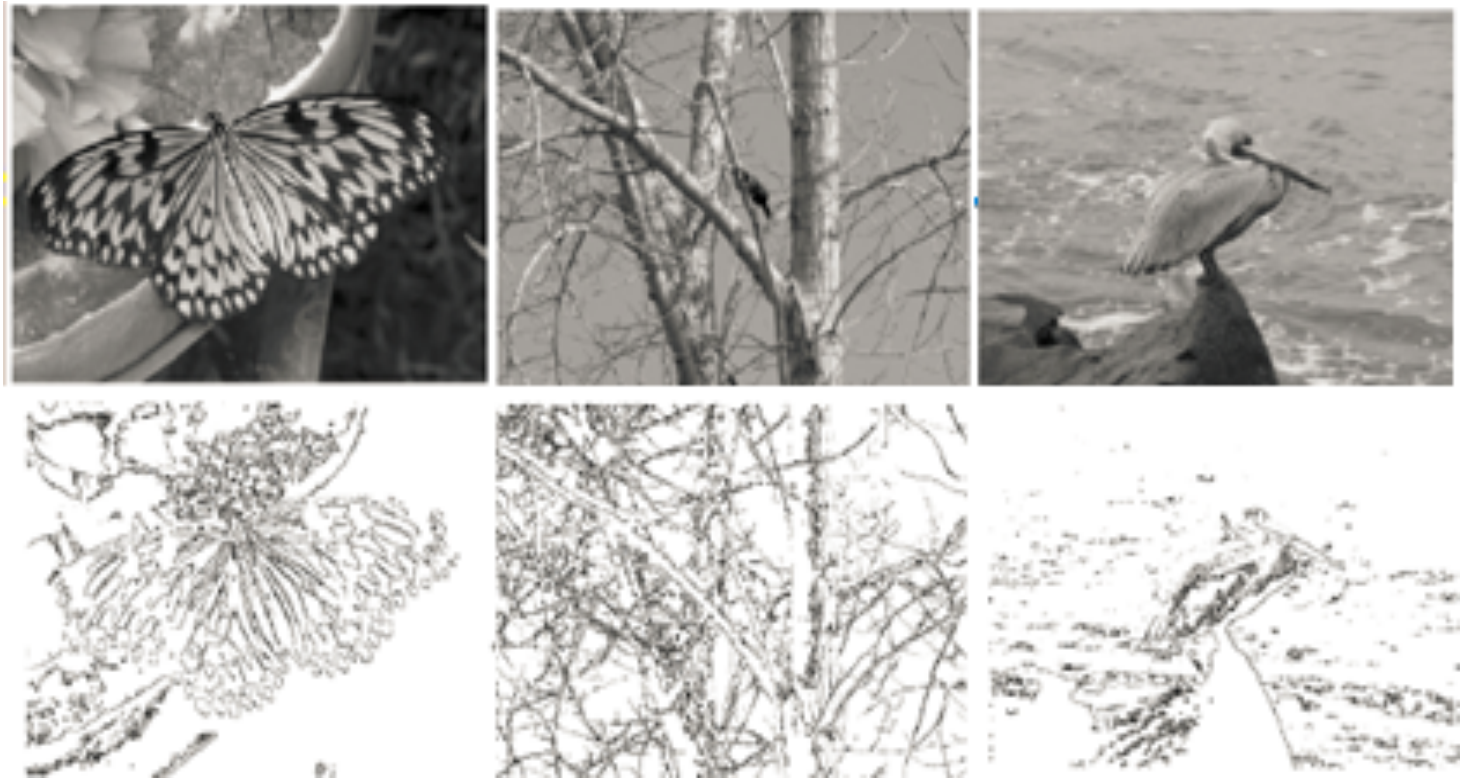
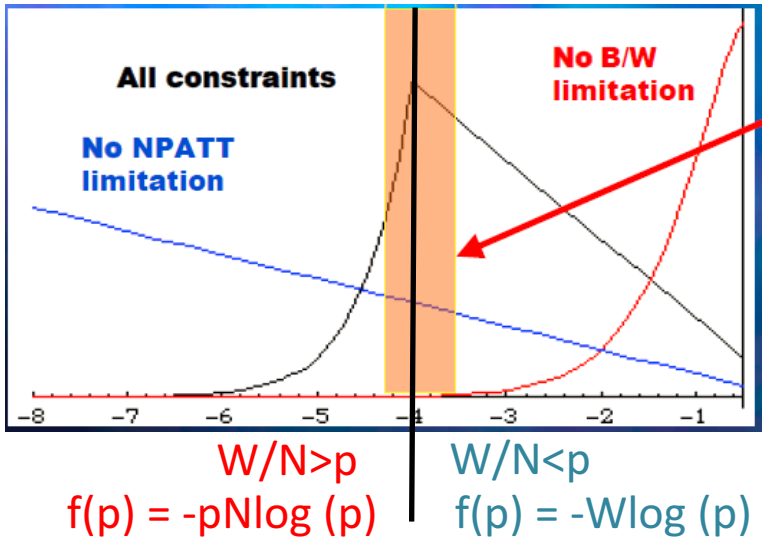


Image processing

- Adopt a brain function model to define “meaningful” patterns

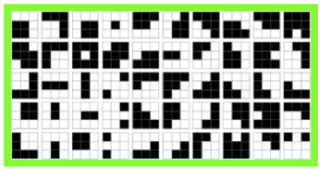
$$f(p) = \frac{-p\log(p)}{\max(1/N, p/W)}$$

$$H = \sum_i^{NPatt} [-p_i Log_2(p_i)]$$

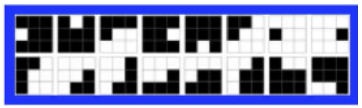


Patterns that are efficient carriers of information given the bandwidth (W) & memory limits (N)

Accepting only these 50 patterns



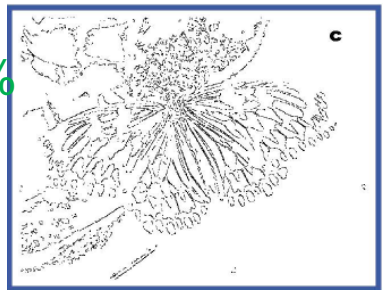
Accepting only these 16 patterns



4 levels of grey: 2^{18} patterns Stored N=2000

9.8%

5.5%

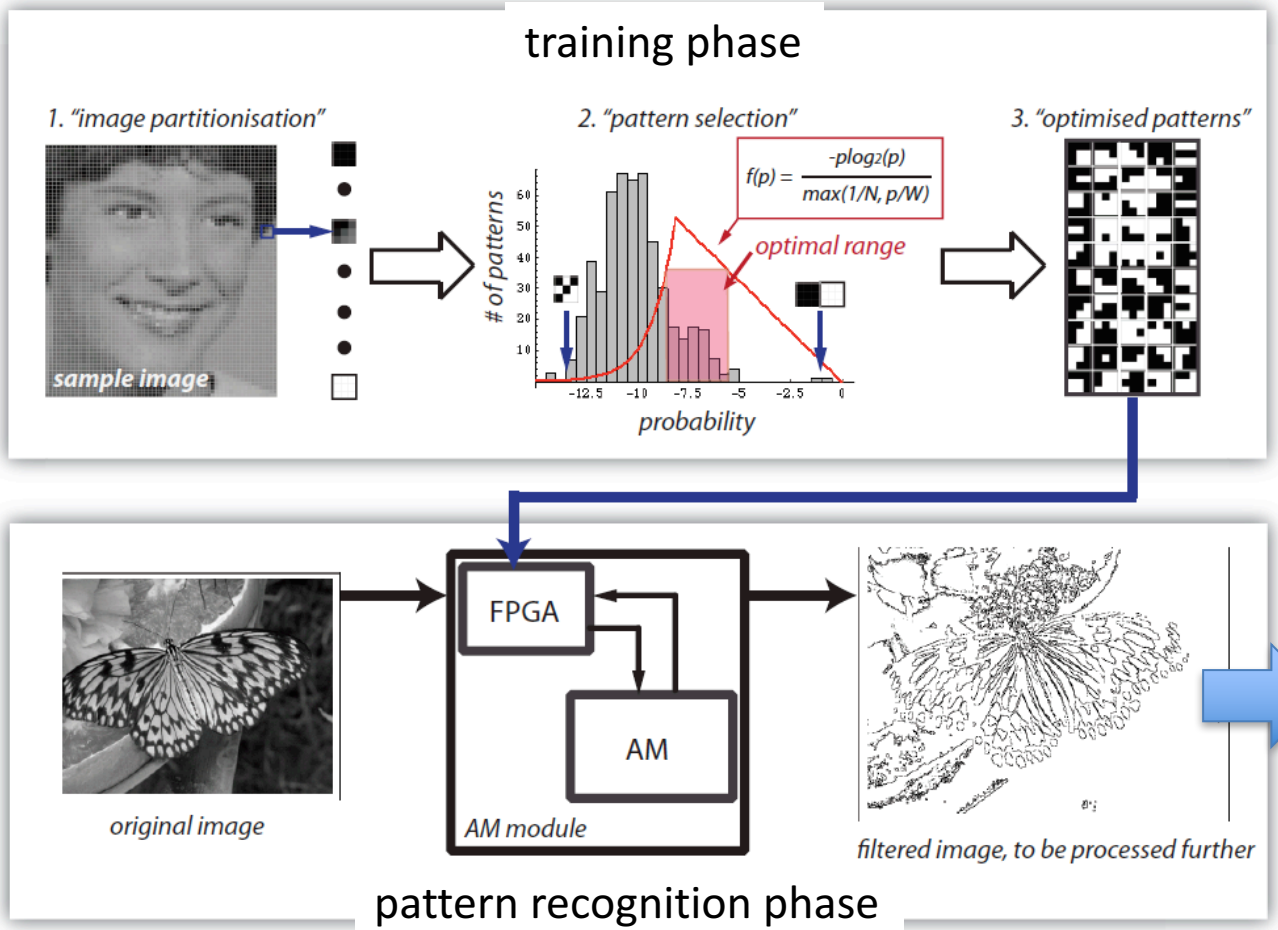


M. Del Viva *et al*, “information and Perception of Meaningful Patterns”, PLoSone 8.7 (2013): e69154.

Hardware concept

pattern recognition other functions

- AMchip + Field-Programmable Fate Array (FPGA)
  - FPGA could enable self-learning feature
  - Ambition is to replace “expert eyes” with the system



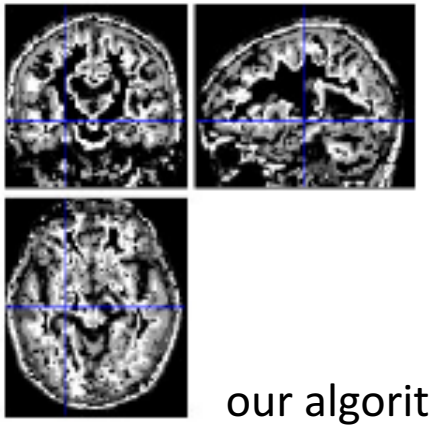
Diagnosis, surveillance, brain/vision study

Application to MRI

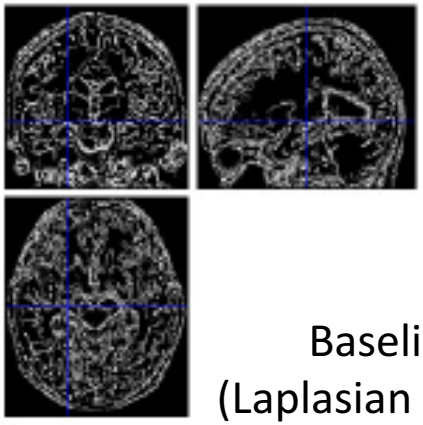
- Result of processing 3D brain MRI images

original

C. Sotiropoulou (Pisa)



our algorithm

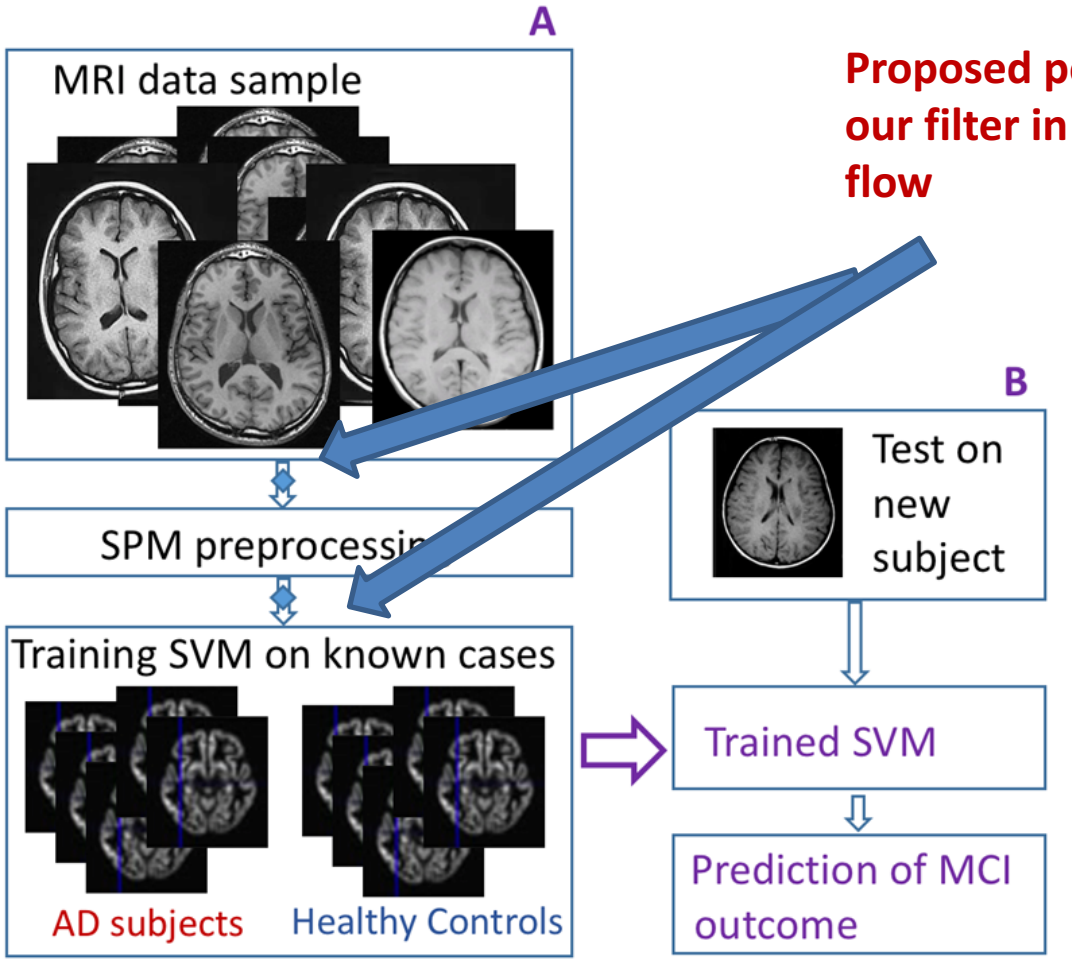


Baseline
(Laplasian Kernel)

These are software result. Implementation of firmware framework is on-going.
C. L. Sotiropoulou *et al*., *Nuclear Instruments & Methods in Physics Research* A (2016), http://dx.doi.org/ 10.1016/j.nima.2016.06.030

Application to MRI

- Try in Alzheimer's disease diagnosis

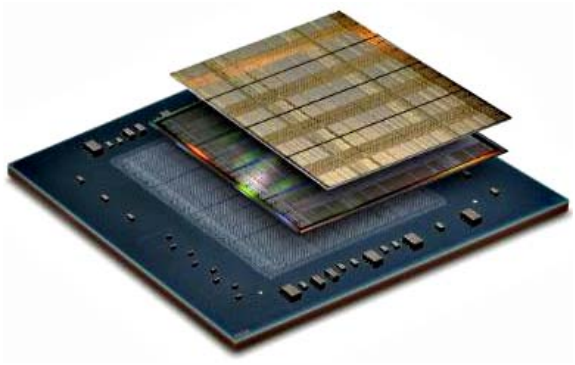


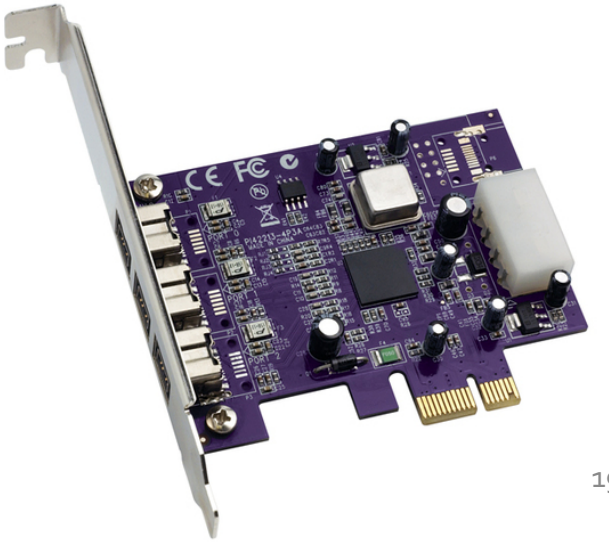
C. Sotiropoulou (Pisa)

Image processing platform

- Targeting a portable and flexible hardware platform equipped with AMchip + FPGA (possibly with a PCI type interface)
  - Track trigger systems for HL-LHC will accommodate the development of basic hardware and algorithms

- SiP approach: Direct FPGA interface to AMchip, high probability to use a Zynq as we could largely profit from the presence of an ARM device





Heterogeneous computing system platform - Vincent Voisin's presentation at MOCAST 2017

Configure Amchip

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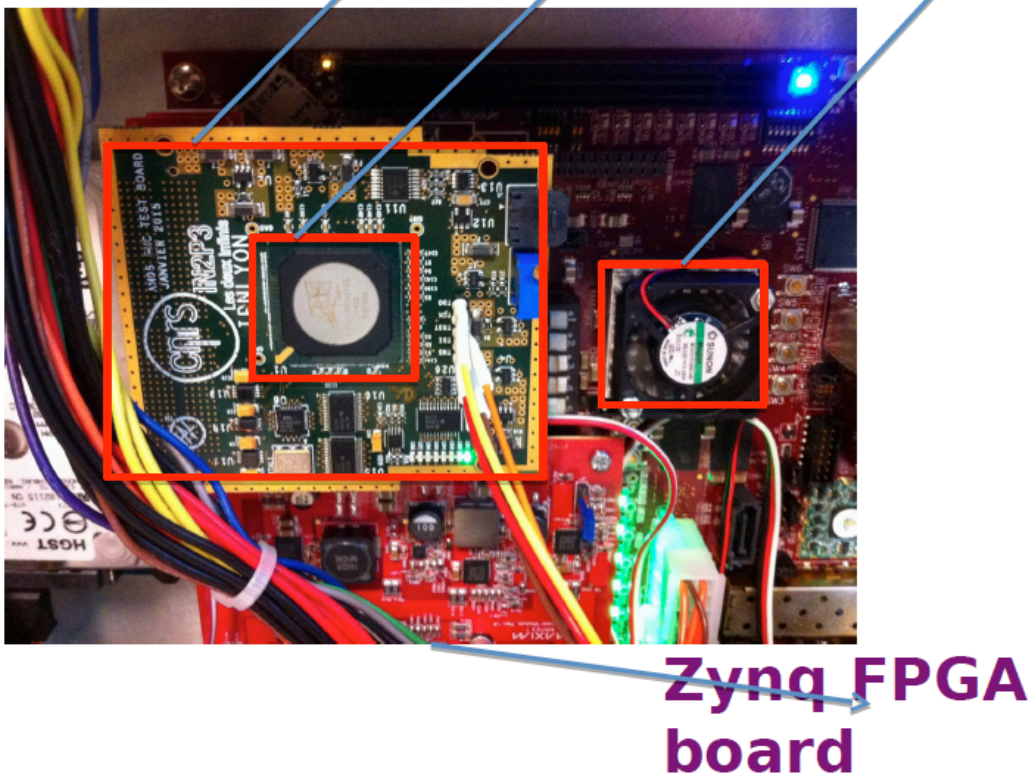
Hardware of The Development Platform



Conclusions

- Very successful and productive collaboration has been maintained between INFN and Melbourne through the development of AMchip and FTK, which are essential in the LHC physics program

- Sustainable collaboration will continue on the AMchip development toward HL-LHC as well as envisioning interdisciplinary applications of the technology

Back-up