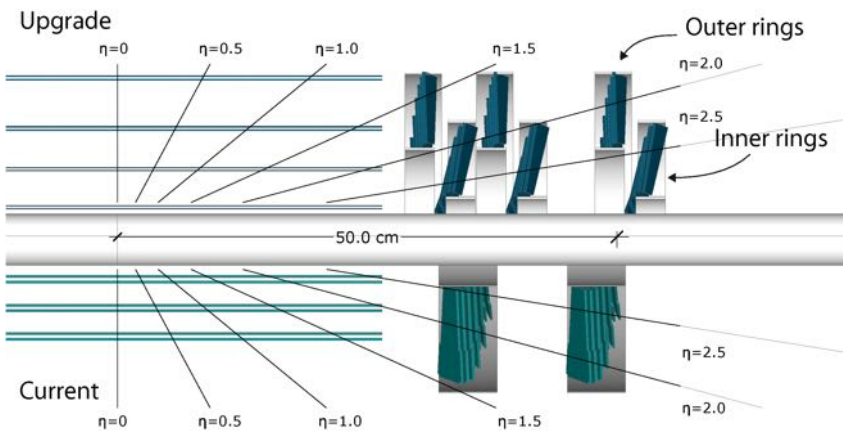
Pixel, tracking e b-tagging 2017

A. ROSSI

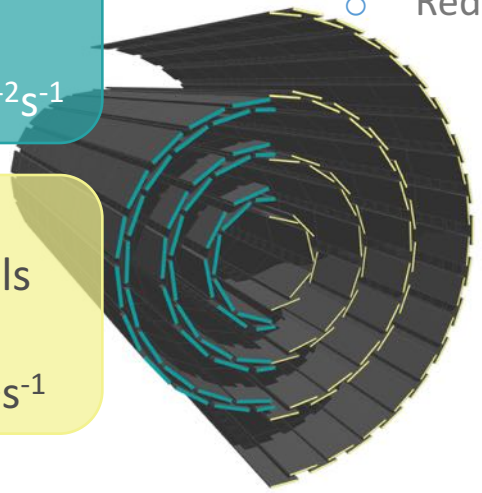
Pixel Phase 1 detector



- Requirements for the new detector
  - No bandwidth limit and reduced dynamic inefficiency up to PU~110: **beyond** $L \sim 2*10^{34}$ $cm^{-2}s^{-1}$
  - Layer 1 closer to the beam pipe: 4.4 cm → 2.9 cm
  - 4 layers and 3+3 disks
  - Fully functional up to LS3
  - New ASICs
    - PSI46dig (BPIX L2-L4, FPIX): larger buffers, digital data transmission
    - PROC600 (BPIX L1): different double column readout
  - New DAQ system
  - Reduced material: CO2 cooling, DCDC converters

Old detector
1444 modules – 66M pixels
R~4.4cm
150MHz/cm^2 @ $1.4x10^{34}$ $cm^{-2}s^{-1}$

New detector
1760 modules – 117M pixels
R~2.9cm
580MHz/cm^2 @ $2x10^{34}$ $cm^{-2}s^{-1}$

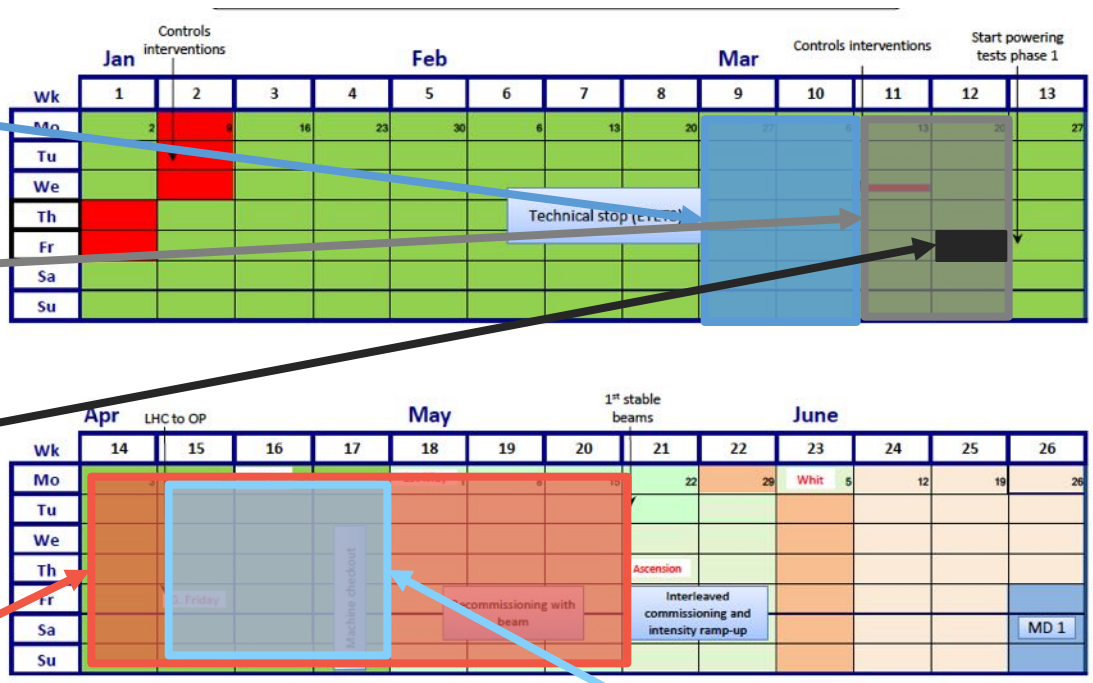


Installation and Commissioning

Detector Installation

Connection Checkout

Cooling plant running cold:
no problem → CMS can be closed



NEW (!!) Pixel detector commissioning:

- Phases readout and control links
  - New 400 MHz data links
- Readout chip shaper tuning
- Pulse height and gain tuning
- Thresholds tuning
  - FPIX profited of pre-installation calibration
  - BPIX L1 with conservative thresholds

Cosmic runs:

- Verify detector(s) tuning
- DAQ in global runs with the whole detector(s)
- Coarse time alignment
- First space alignment
- MAJOR RESULT: found and fixed a serious bug in the pixel geometry

Phase1 : New aspects

- Power delivered through on detector DCDC converters
  - 11-11.5V → 2.4-3.5 V
  - On-detector protection fuses will be removed during LS2
    - No incident in the detector…up to October 5th
  - Turned out to be ideal for the power cycles to recover modules affected SEUs
    - It is enough to disable/re-enable single DCDC converters
- CO_2 2-phase cooling: a new entry in CMS
- Completely new DAQ system
  - New readout links: 400 MHz fully digital
  - New back end standard: uTCA
    - New back end boards: FEDs, FECs, AMC13
  - Bandwidth limit improved with respect to old detector: ~80 pileup events at 100 kHz
    - New f/w in development to go over PU=100 (Heavy Ions)

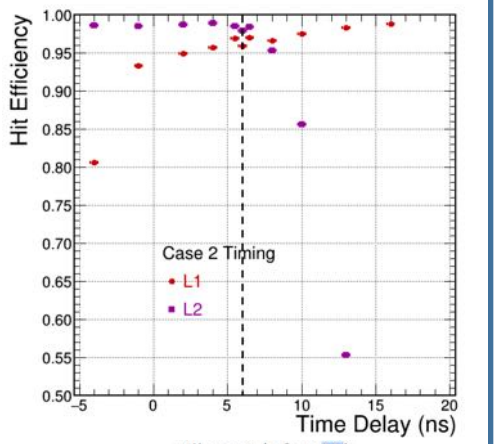
Commissioning: Detector Issues

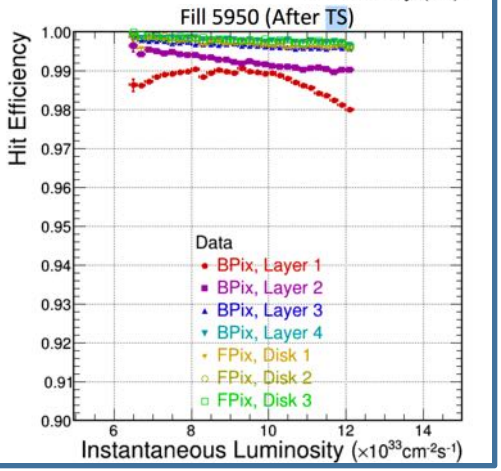
- PROC600 (BPIX L1) main source of problems
  - Rate-dependent cross-talk noise observed during module test
    - Thresholds set, conservatively higher than planned (~3000-4000 e-). In time thresholds depend also on timing setting
  - Different clock phase w.r.t. PSI46dig (BPIX L2)
    - Not possible to choose optimal timing setting both for BPIX L1 and L2: observed with first collisions
      - Phase difference had to be corrected in the clock distribution circuits
  - Higher than expected dynamic inefficiency (rate-dependent data losses)
    - Exact cause(s) not yet understood fully
    - Several adjustments and studies done to mitigate and understand it
  - Larger spread in pixel signal gain and pedestals
    - Require careful pulse height tuning and high granularity offline corrections
      - Postponed during commissioning without beam and completed during TS1
- Observed “unrecoverable” SEUs in Token Bit Manager (TBM)
  - Mostly in BPIX L1 because of the higher particle rate
  - It requires a power cycle (DCDC converter dis/re-enabled)

Commissioning : Timing Scan

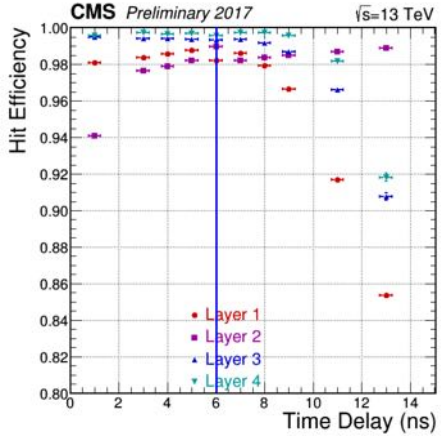
- Different approach tested in order to get the best performance from Bpix L1 and Bpix L2

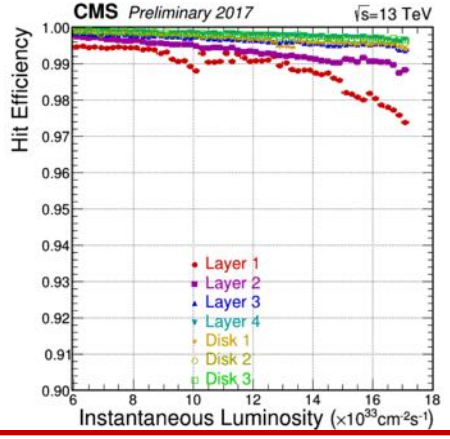
2nd attempt: L1 early, L2 late





3rd attempt: L2 early, L1 late



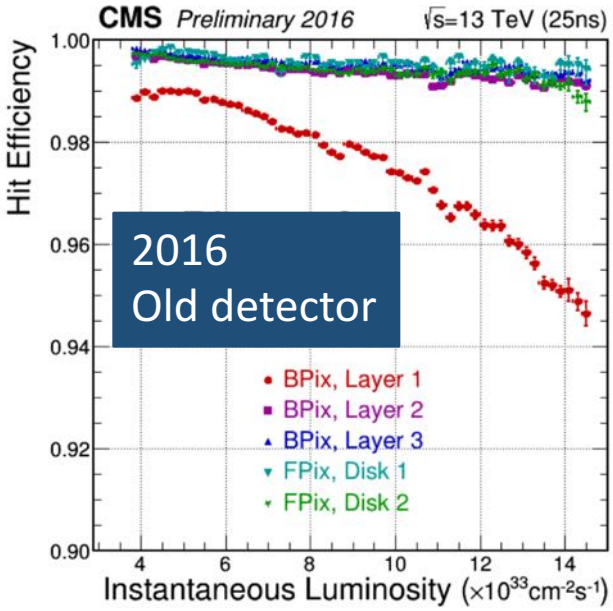


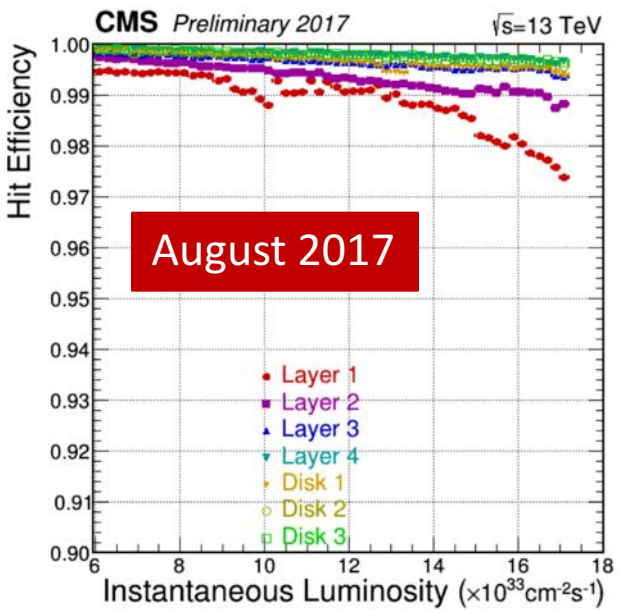
Final Settings:

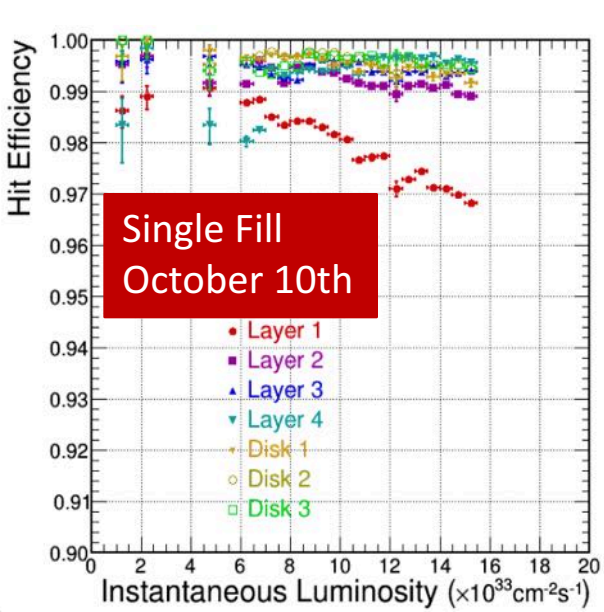
- Not optimal for Bpix L2: threshold 1000e- higher than ideal one

Dynamic inefficiency

- Dynamic inefficiency is smaller than in the old detector
- Expected to be even smaller
  - 98% at $2x10^{34}$ $cm^{-2}s^{-1}$
- Source not completely understood

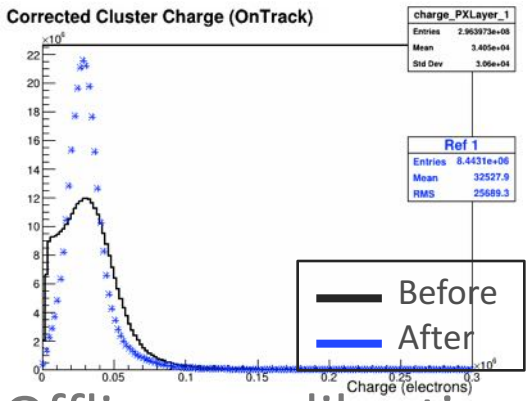




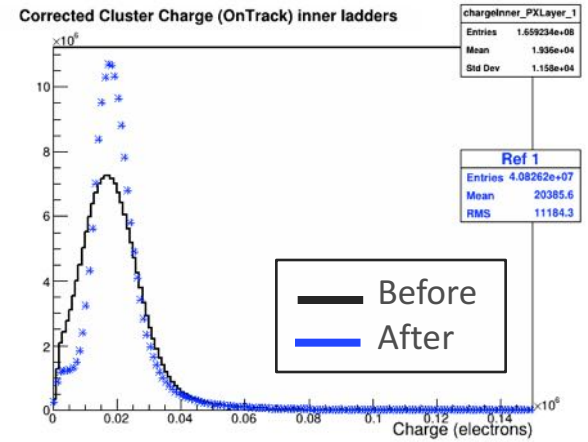


Impact of detector tuning

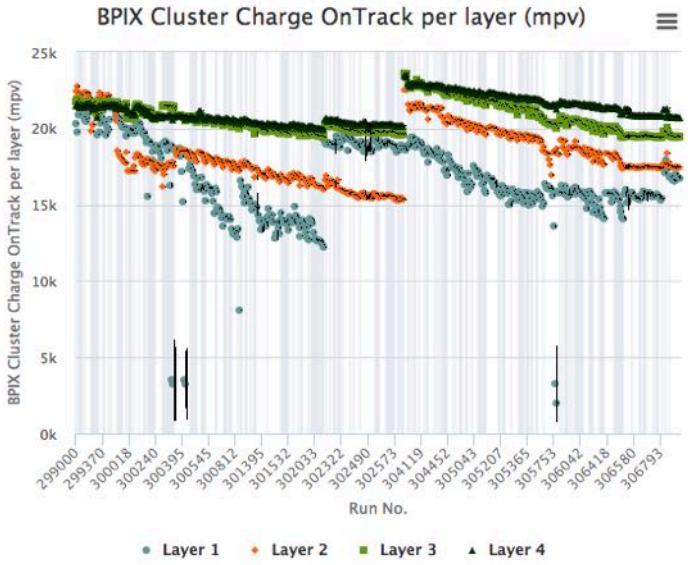
- i.e. : Cluster Charge
  - Pulse height and gain calibration



  - Offline recalibration + Bug fix (ReReco)

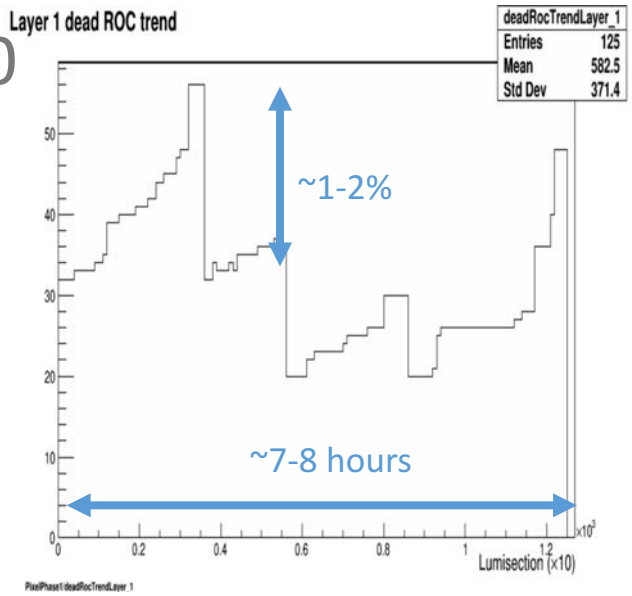


  - HV increase recover steady signal loss



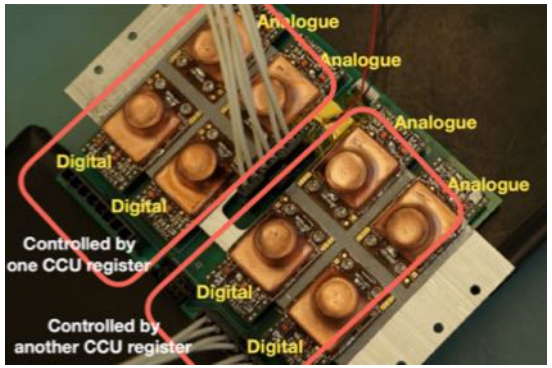
Temporarily inactive channels

- Single Event Upsets (SEUs) affect ROC, TBM and portcard
  - ~2ROC (1/8 module) inactive every 10 minutes at L~$10^{34}cm^{-2}s^{-1}$
    - Mainly on Bpix Layer1
  - Some SEUs on TBM are not recover with a reset ("stuck" TBM)
    - power cycle needed
- Automatically masked without affecting data taking
- Soft Error Recovery attempted when 20 channels affected (15 in L1, 8 in central L1)
  - Firstly by reprogramming the modules
  - Modules not recovered at first attempt are power cycled
  - SEUs in port cards (~10 modules) are detected and recovered by reprogramming



DCDC Issue

- DCDC stop working without (apparently) no reason
- First event on October 5th
- Almost all of them after a dis/en-able cycle or a power cycle
  - Only one hours after the last power cycle and one during stable beams
- Both digital (3.3/3.5V) and analog (2.4V) DCDC converters are affected
- Both Bpix and Fpix
- Power cycle or dis/en-able many of them in any case
  - to recover modules affected by the “unrecoverable” SEUs in the TBM
  - To investigate the problem
  - Because of global power cycles of the detector
    - LHC and beam conditions
- Failures almost continously up to now
  - Rate slightly decrease in the last 2 weeks

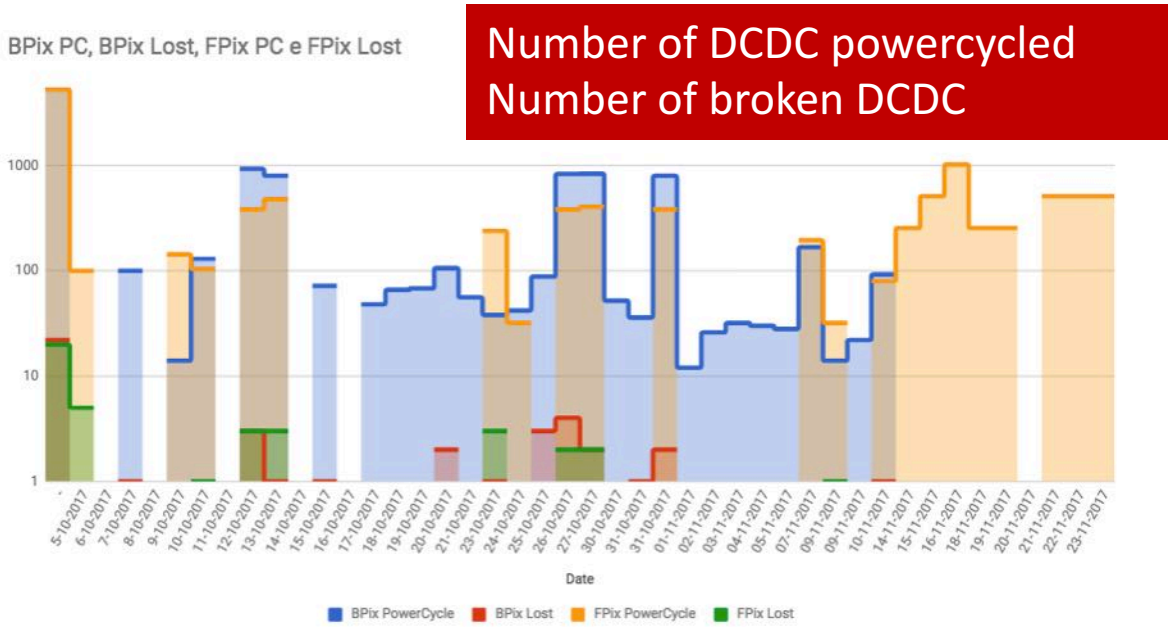


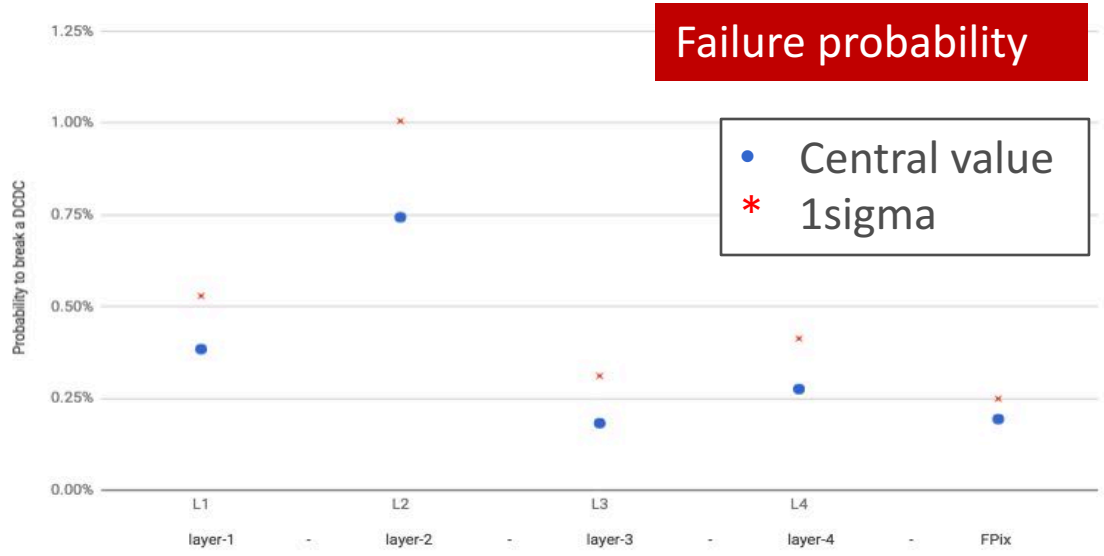
Investigations

- Task Force in place
  - https://twiki.cern.ch/twiki/bin/view/CMS/PixelPowerProblems
- Daily Pixel Operation meeting : https://indico.cern.ch/category/1732/
- Technical Incident Panel
  - https://indico.cern.ch/event/677774/

- Explanation and solution not yet found

Failure statistics



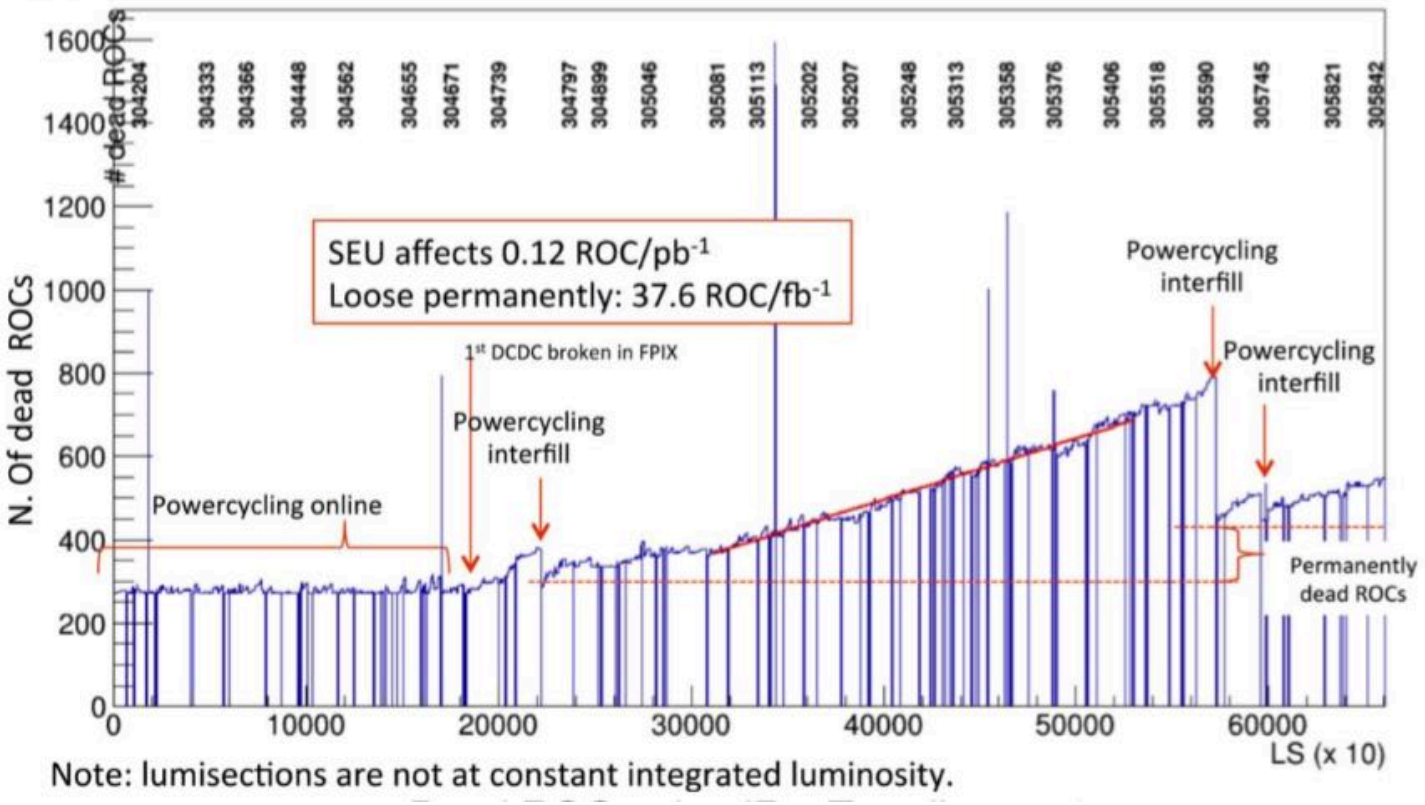


- All DCDC power cycle from October 5th
  - Manual dis/en-abling to recover ”stuck TBM”
  - Full detector power cycle (5)
  - Fpix D1+D3 massive power cycles (10)
  - Automatic PC
    - Re-enable for few hours
- 55 DCDC converter failures
  - **Few of them restart to work (spontaneously)**
    - 5 Analog, 4 Digital
      - 3 unstable
      - 2 provide limited analog current

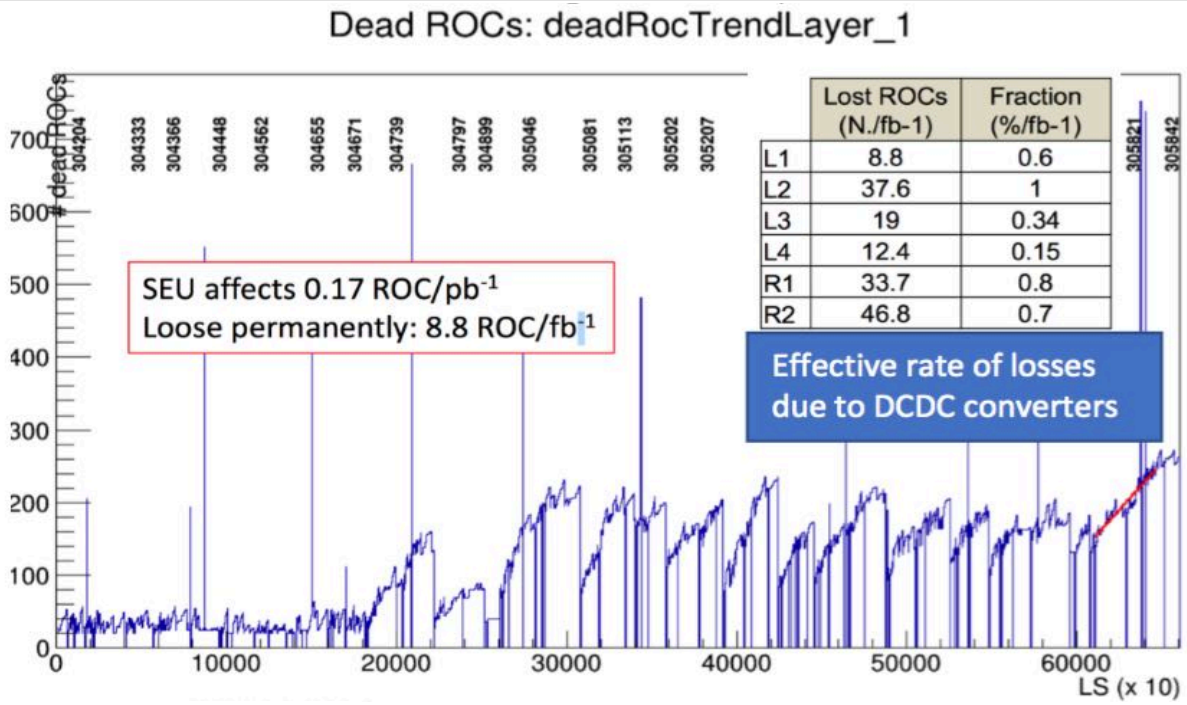
SEUs and loose rate estimation

- Inactive channels build up because of “stuck TBM” and no automatic power cycle
- Interfill power cycles recover them but can break DCDC converters
  - DCDC failure proportional to luminosity

Bpix Layer 2

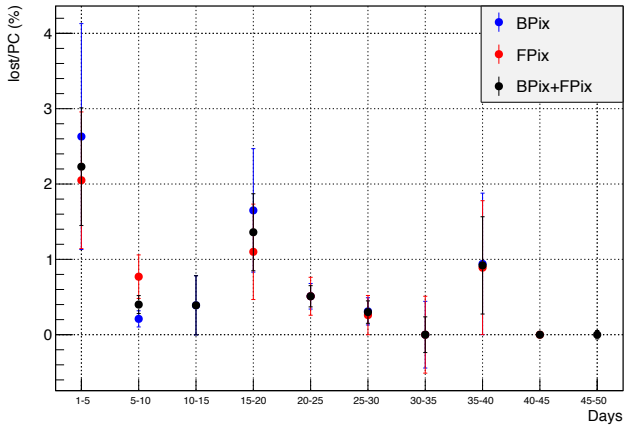


SEUs and loose rate estimation



	Lost ROCs (N./fb-1)	Fraction (%/fb-1)
L1	8.8	0.6
L2	37.6	1
L3	19	0.34
L4	12.4	0.15
R1	33.7	0.8
R2	46.8	0.7

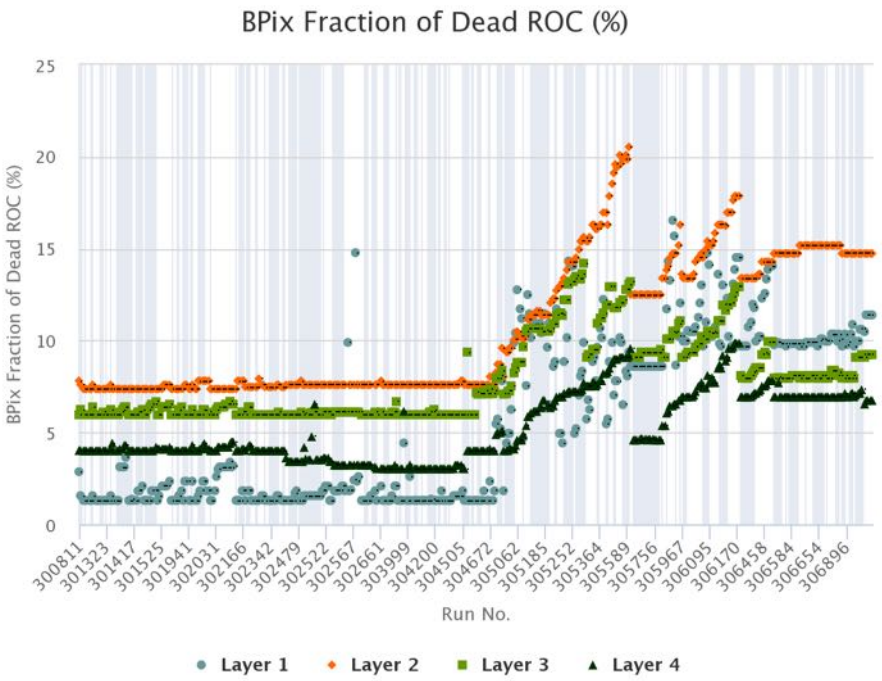
Probability to lose a DCDC (in bins of 5 days)

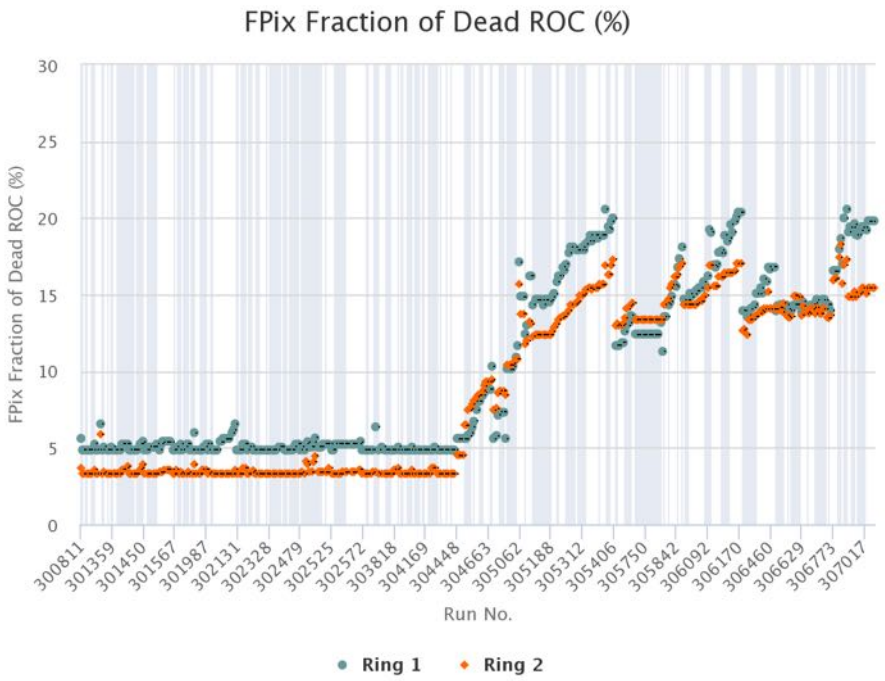


- During the last two week the rate decrease

Inactive channels 2017

- Clearly visible the moment when automatic Software Recovery was disable





- Total fraction of inactive ROC now ~11%

Conclusion from statistical analysis

- No correlation between the number of power cycle and broken DCDC
  - All the DCDC have experienced almost the some number of power cycle (mainly in April/May)
- No patterns in the distribution of the broken DCDC converters
- The failure rate per power cycle almost steady
  - Cause is not radiation or (unsafe) operations ?

Test Strategy adopted

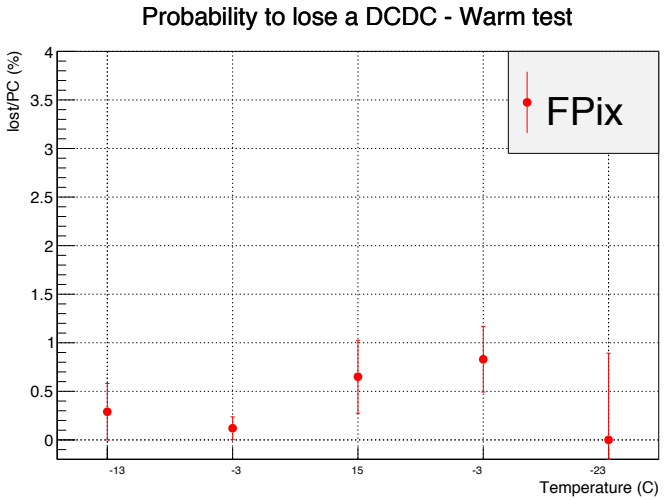
1. Understand the source of the problem
   - Main goal is to stop the problem
     - No success → Detector will be extracted
   - Find some hints in order to understand where to look once the detector will be out
   - Check all the procedure for 2018
2. Finish the 2017 data taking in good condition
   - Keep the number of power cycle as low as possible
3. Assumptions (continuously stressed)
   - Problem on DCDC board
     - Common component of Bpix and Fpix
     - Also not connected DCDC failures
   - Module not compromised by these failures
     - Everything works fine on recovered DCDC modules
     - Module cannot be replaced

Tested possible cause

- Something change on October 5th
  - Nothing has been identify
- Blow fuse at DCDC input
  - Evidences exclude this
- Overvoltage at DCDC input
  - ASIC could break
    - DCDC failure reproduced in lab only with OV
- Failure of components on DCDC board
  - Test ongoing
- Mechanical failure
  - Not compatible with recovered DCDC
  - Any kind of short should blow the fuse or trigger power supply protection
- Problem in the DCDC enable line form CCU
  - Not obvious how this can break DCDC
  - No anomaly observed due to radiation or GND level differences
- Noise in/from power system
  - No evidence on both Lab and UXC
- External causes
  - Radiation, high luminosity
    - No changes on failure rate
  - Magnetic field
    - No evidence from Lab test inside magnetic field

Tests with detector

- Try to understand what is broken
  - DCDC converter IV curves of several power groups
- Monitor the input voltage on DCDC
  - DCDC chip designers suggest to check for Over Voltage
  - Installed scopes to monitor power supply outputs during dis/en-able cycles: no anomaly observed
- Modify conditions to modify failure rate
  - Statistical analyses
  - Reduced input voltage (11V→9V) in 50% analog converters
  - No failure of ANY analog converters since then...
- Some DCDC on Bpix are unused, stress test on those
  - ~500 dis/en-able cycles: no failure
- Stress test of four DCDC converter sets (8 converters) in FPIX
  - One failure after ~250 power cycles (for each converter), digital converter
  - after ~3300 power cycles no other failure show up
- Failure rate measured at different temperatures
  - Failure rate per power cycle close to the one observed in standard conditions **in the first 30 days**



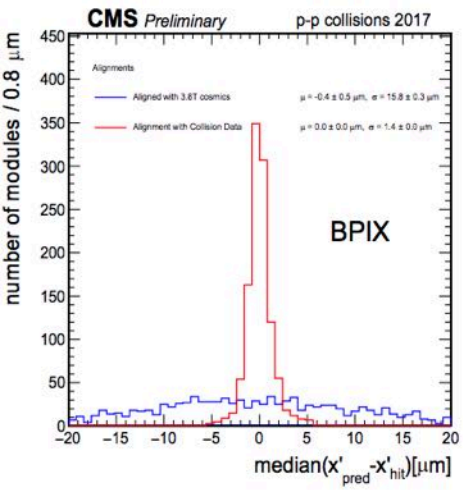
Tests in Lab

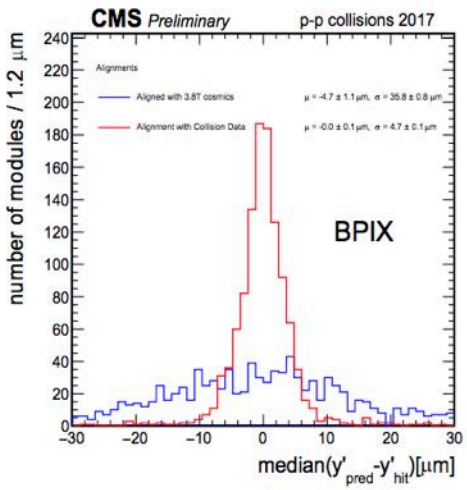
- A lot of different tests in Lab
  - Try to reproduce the failure
    - Very frequent dis/en-abling sequence
      - No failure up to 1000's cycles and passive loads
      - No failure up to 100's cycles and real modules
  - Look for anomalies (spikes, oscillations…) in the power system
    - Nothing observed
  - DCDC behavior inside magnetic field (3T)
    - No failure observed with 500Hz dis/en-able cycles and different orientations
  - Radiation
    - Old results on irradiated converter show no anomalies
    - New irradiation with X-rays (1.5Mrad, CMSx2) has the some conclusions (same chip but different boards)

Tests in Lab (cont'd)

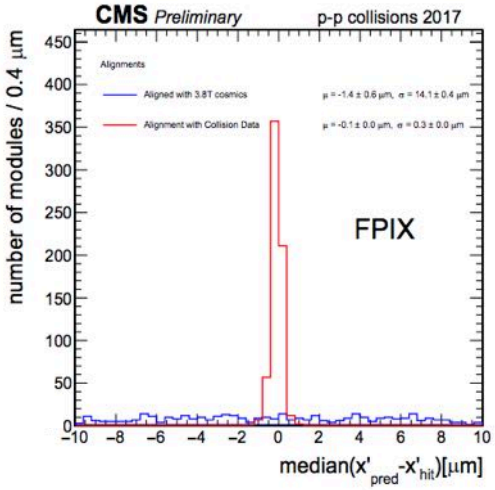
- Fast dis/en-abling sequence (enabling before voltage is 0)
  - No failure
- Back power from neighbour DCDC
  - No failure
- Anomalous signal on enable line
  - No failure
- Attempt to break DCDC
  - Only two possible scenarios found up to now
    - Input voltage exceed 17-18V
    - Input capacitor removed (or damaged)

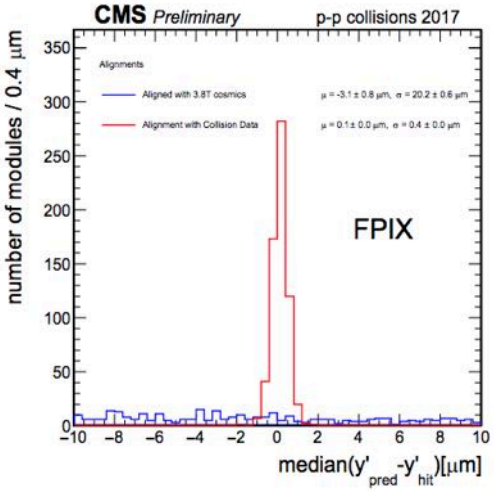
Performances: Alignment

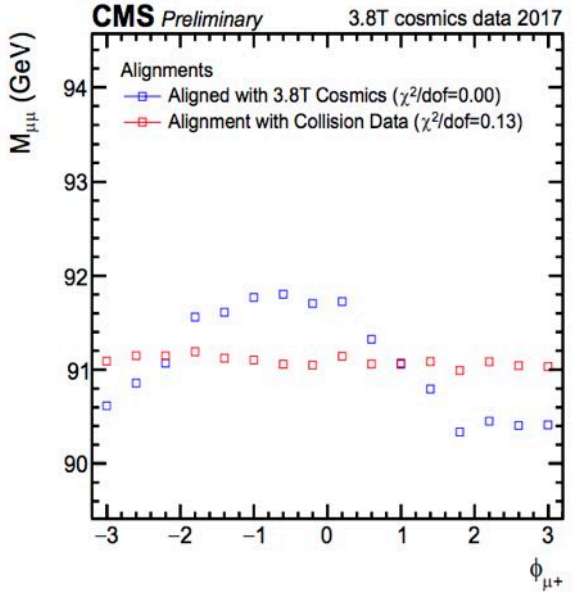




- Many alignment campaigns
- Intrinsic resolution reached very soon

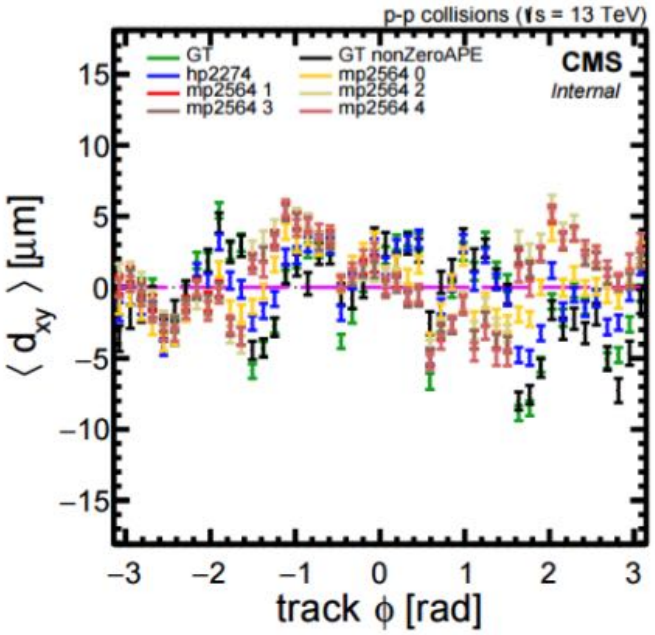


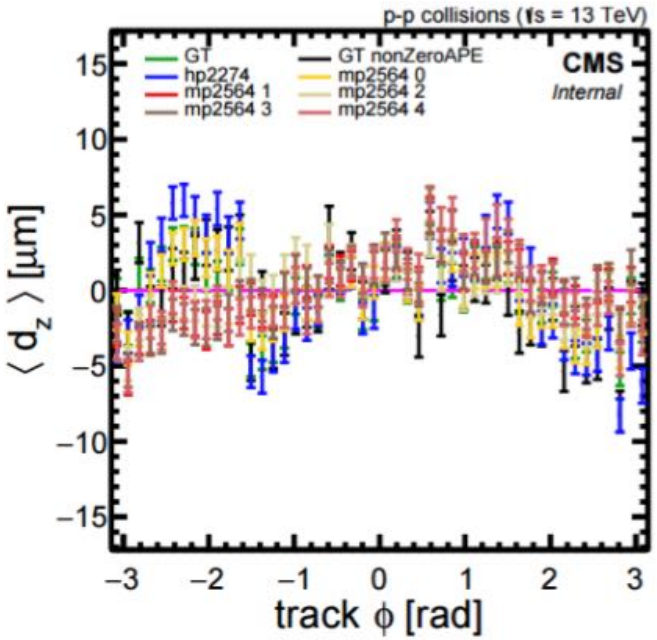




Performances: Alignment

- Primary Vertex

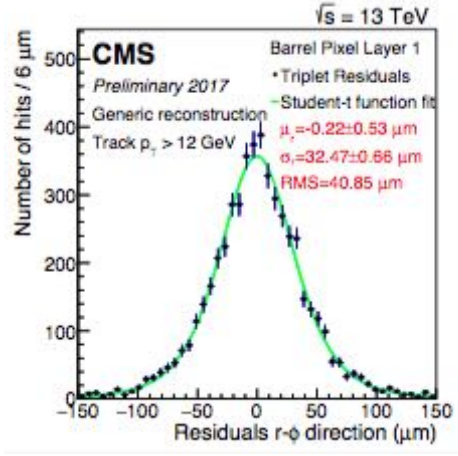


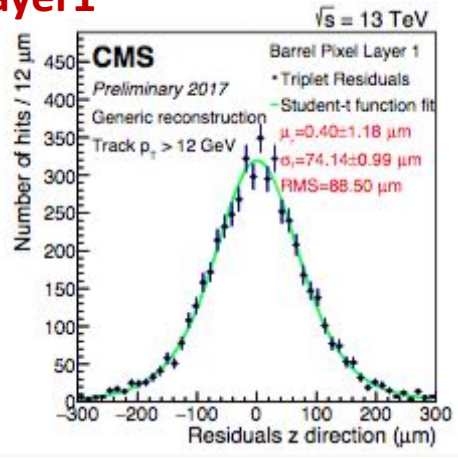


- Position of PV as a function of track coordinates is very sensible to the pixel part of the tracker
- PV performance got a lot of improvement during the year

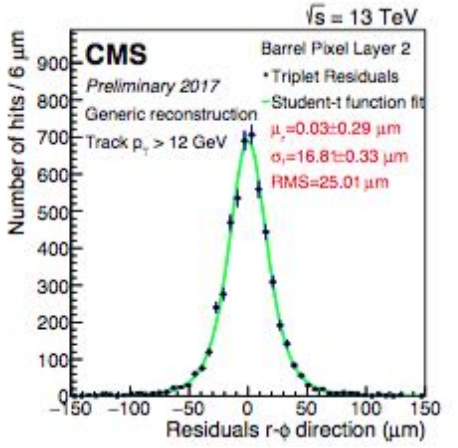
Performances: Hit Resolution

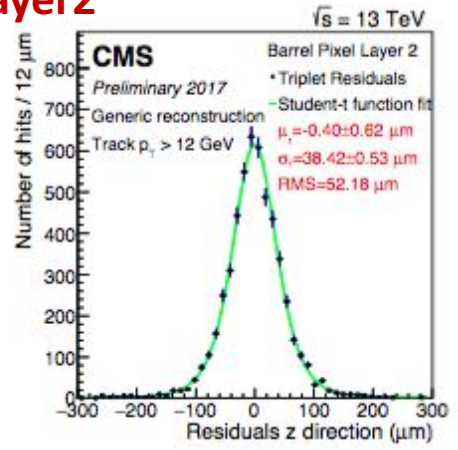
Layer1



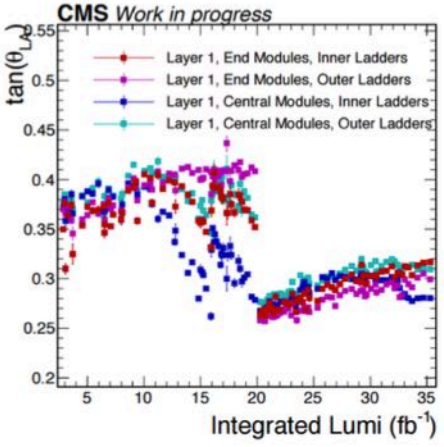


Layer2





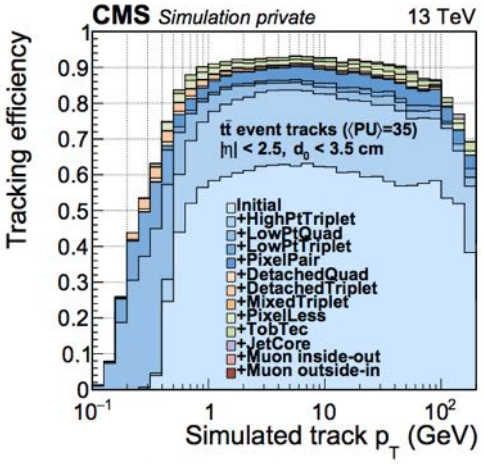
- Layer 2-4 and Fpix good MC matching and as expected resolution
- L1 ~50% worse than expected
  - Reproduced by MCv2 with increased threshold
  - Present challenge



- Changes on L1 HV affect Lorentz Angle
- Impact on clusters position

Performances:Tracking

- Despite the not optimal performance of BPIX1 and the larger than expected number of inactive components, Physics in 2017 is not compromised
  - Mitigations already in place, more foreseen
  - Performance better than 2016 even in the toughest conditions
  - Improvements expected with ultimate alignment and calibration



From 9_4_0_pre1 RelVal

MC ttbar PU=35
Run 283408 PU~35
Run 299649 PU~40
Run 302553 PU~30
Run 302597 PU~20

V. Innocente, CMS Week

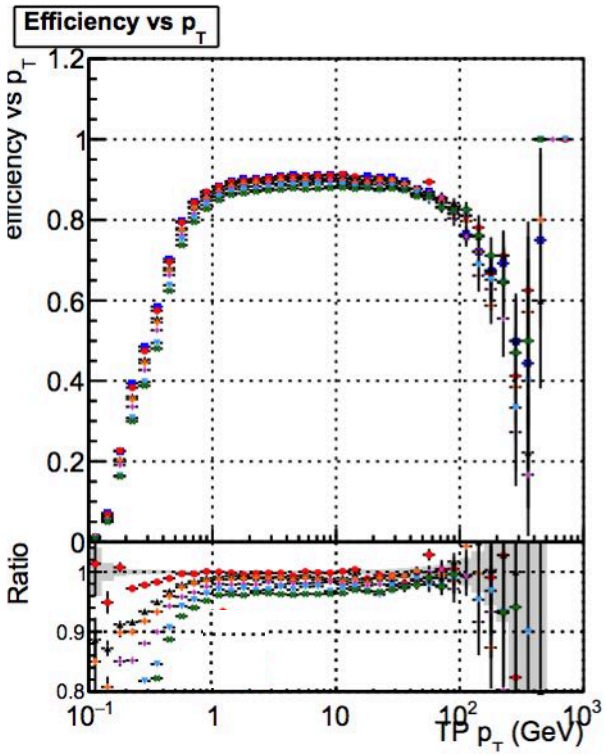
Impact of Pixel issue

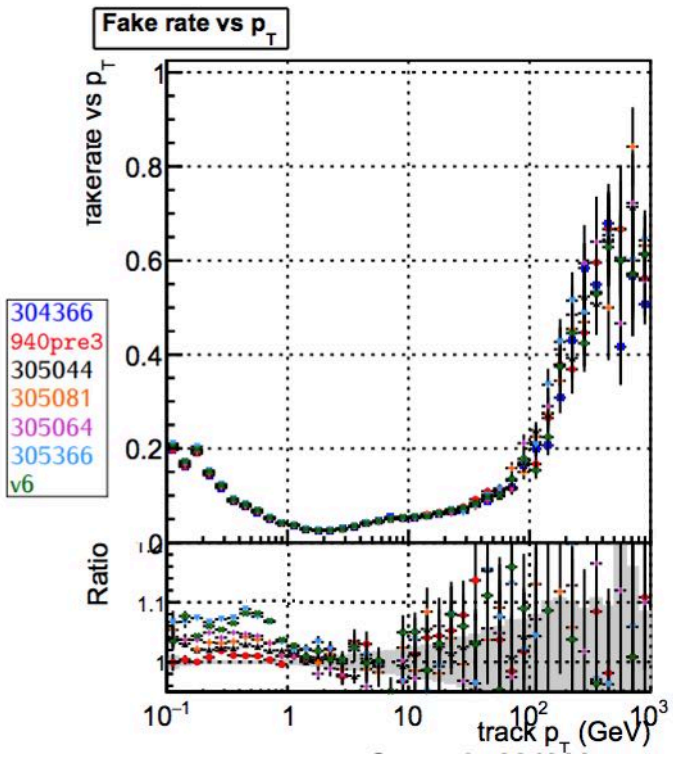
- Tracking and BTV POG are working on estimates and corresponding plots derived by simulations
  - Also others POG are working on the Pixel failure impact (not reported here)

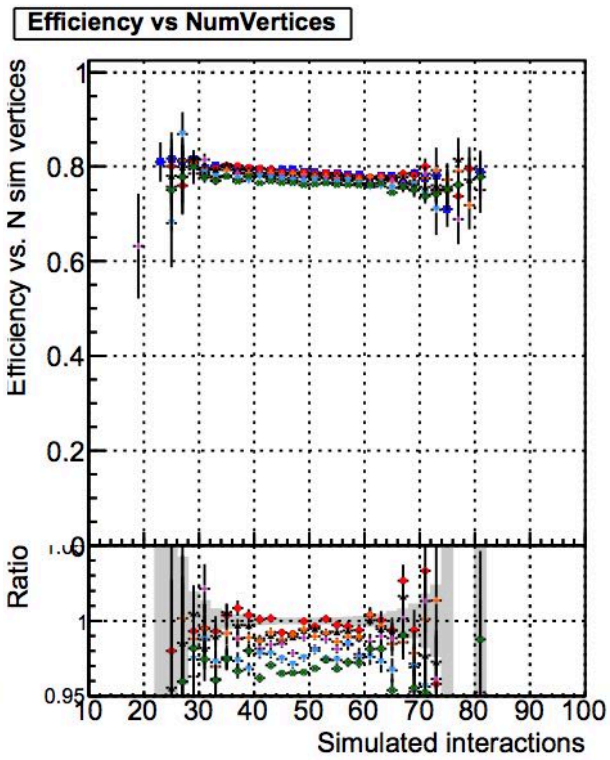
- Some preliminary results shown here
  - ttbar RelVal
  - Scenarios from data
    - Run 304366 : reference
    - Run 305044 : Permanently BAD DCDC
    - Run 305064 : Large overlap hole in Fpix
    - Run 305081 : Two FEDs with errors
    - Run 305366 : Highest number of BAD components
    - V6 : estimated 2017 end scenario

    - Maps in backup

Tracking



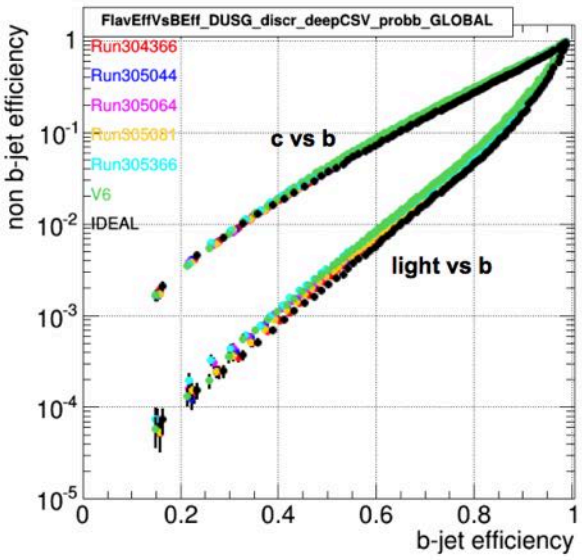




M. Kortelainen

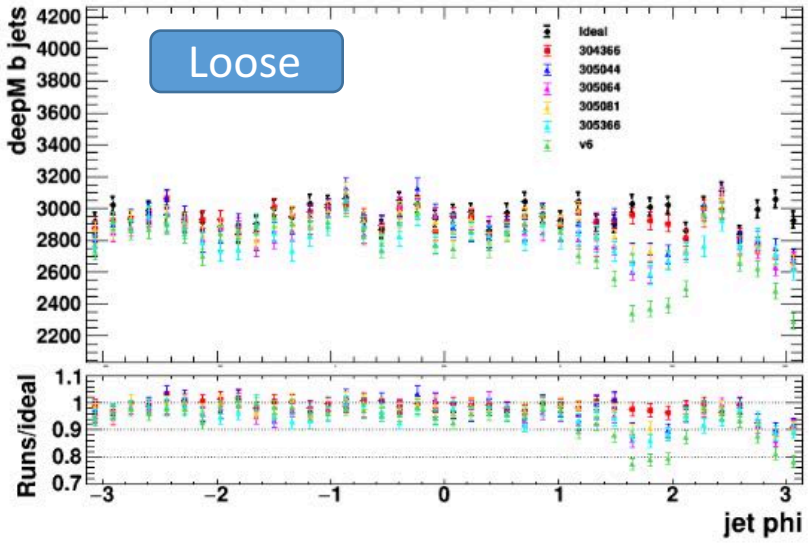
- Overall efficiency decrease by up to 4% with a increase on fake rate up to 3%
- Vertex efficiency decreases by up to 3 %
- Also IP resolution and Vertex resolution are affected

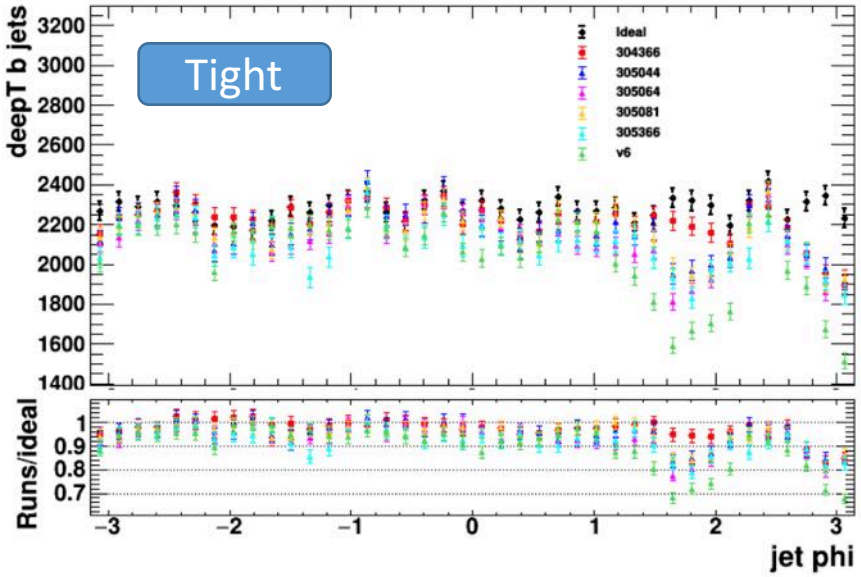
B-tagging



- Impact of DCDC issue on b-tagging efficiency is present
  - Some region on ϕ more affected

C. Collard





Intervention during YETS2017

- Needed to understand the cause of (and the solution to) the problem and repair the broken DCDC converters
- Requested one week earlier start of YETS to extract FPIX+ before Christmas
- In meantime some work on DCDC to be ready for replacement
  - Change the input fuse on DCDC spares:
    - 1.5A --> 4A (Digi) 3A (Ana)
    - Input voltage could me further decreased
  - Build new DCDC with the available componets
    - 4A/3A fuses and 25V capacitors

Conclusions

- Very challenging year for new Pixel detector
- Faced different issues from commissioning to DCDC problem
  - A working solution for almost everything has been addressed
  - DCDC converters issue is the most problematic and the most difficult to face
    - Constant work during the last 2 month
    - Cause not yet understood, tests still ongoing
    - Detector extraction during YETS with two main focus
      - Understand what has been broken
      - Apply some modifications to have a safe 2018
    - Impact on tracking, b-tagging, physics still under study
- Detector performances during 2017 have been good (at least up to October 5th) and they have a continuous improvement during the year
- Plans to replace Layer1 modules (new sensors, new TBM, new PROC600) during LS2

Backup

Commissioning : Timing Scan

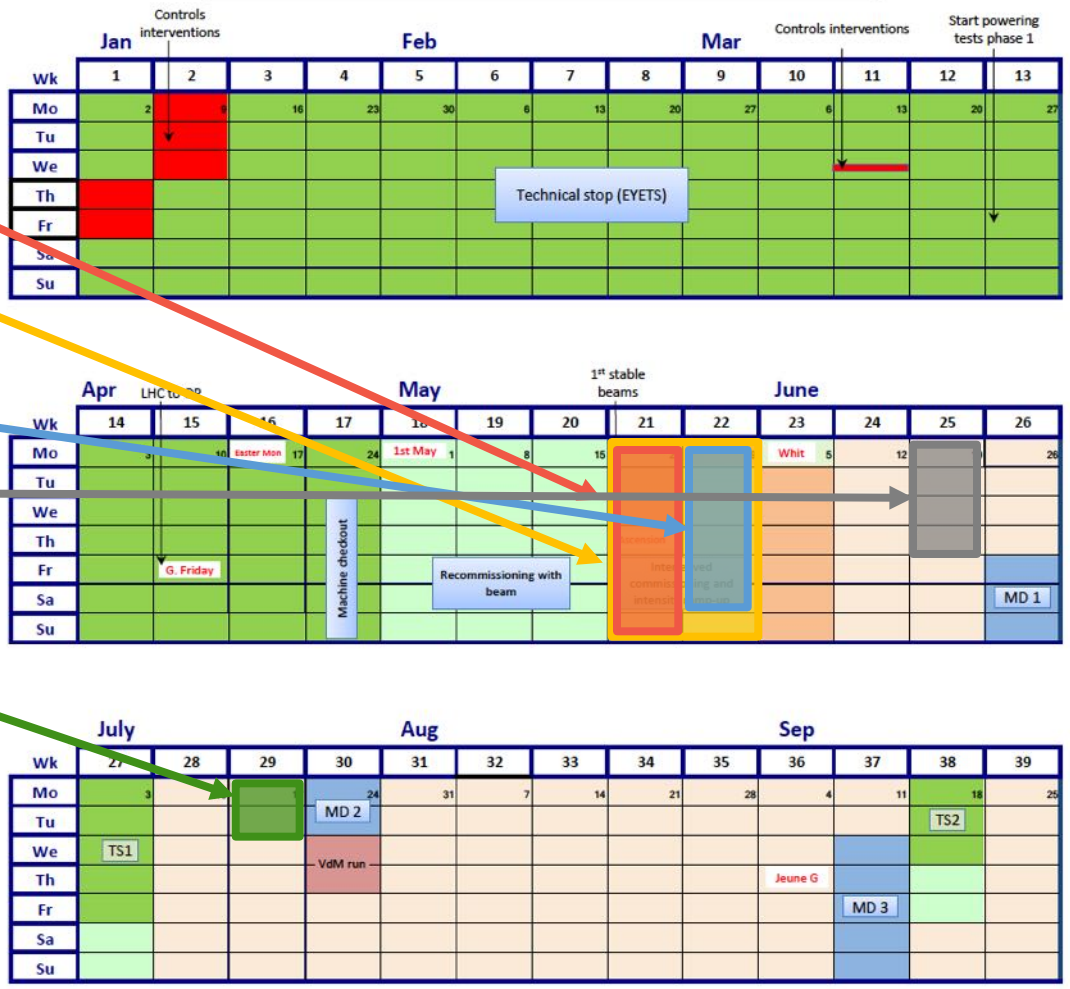
Strip time adjustment completed

BPIX L3-L4 and FPIX time adjustment completed

1st attempt BPIX L1-L2 timing

2nd attempt BPIX L1-L2 timing

Final BPIX L1-L2 timing



- Last timing scan performed at the end of October (150b fill)
  - Setting confirmed

Commissioning: Detector Tuning

BPIX L1 HV → 200V

BPIX L2 HV bias → 250V
to improve timing

Pixel HV bias increase
to compensate rad effects:
- BPIX L1 → 350V
- BPIX L3-L4 → 200V
- FPIX → 300V

FPIX thresholds retuning

BPIX thresholds:
L1 thresholds reduced by ~15%

BPIX pulse height and gain calibration

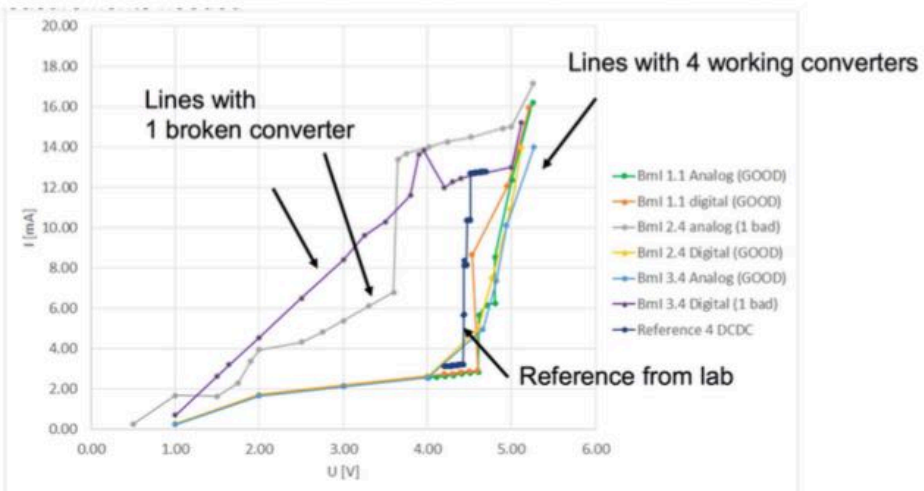
S

Dead Time

- Continuous balance between higher detector efficiency, higher uptime, and lower dead time
  - Introduced periodic (70Hz/100Hz) ROC reset to mitigate dynamic inefficiency
    - Unavoidable dead time to readout the pipelines before the reset: reduced to 0.7% from 1.3%
  - New Soft Error Recovery procedure
    - Negligible dead/downtime (at L~$10^{34}cm^{-2}s^{-1}$)
    - With old procedure about 1-2% dead time (at L~$1.5*10^{34}cm^{-2}s^{-1}$)
    - Power cycle took ~5 minutes, now ~20-30 seconds
  - Optimized detector configurations (Pixel+Strip) when HV is on
    - Reduced by 50% by performing a single pause and resum
    - Pixel configuration now in parallel: pause and resume reduced to only 5 seconds

IV measurement

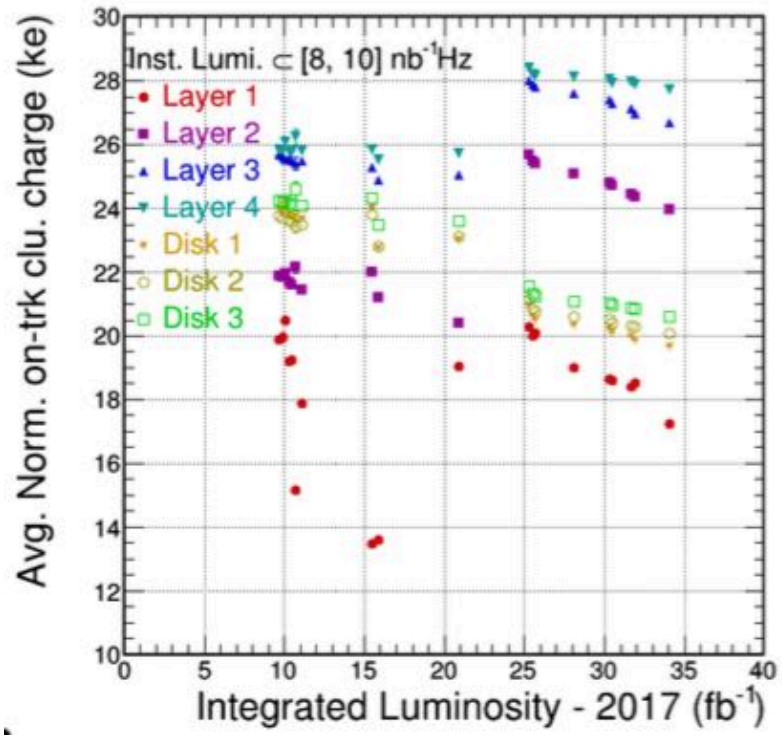
- FEAST2 designers suggested to measure the IV curve to see the DCDC linear regulator switch on
  - Voltage on DCDC from 0 to 4.7V (output not enable)
  - Every linear regulator should drain 3mA

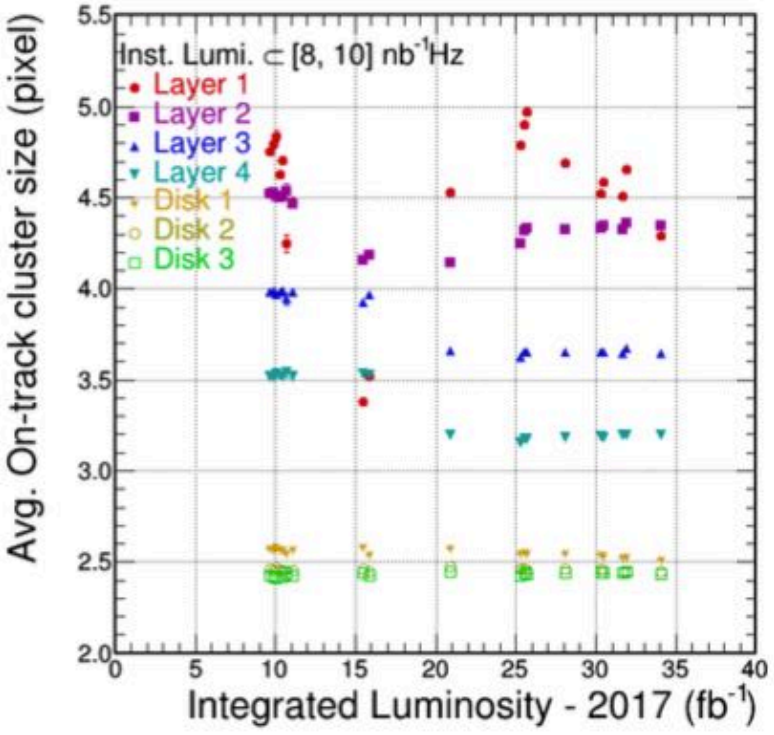


  - When all DCDC converter are good the behavior is as expected
  - When there are broken DCDC an ohmic behavior show up
    - Similar behavior of lab DCDC broken with over voltage

Performance: Charge Collection

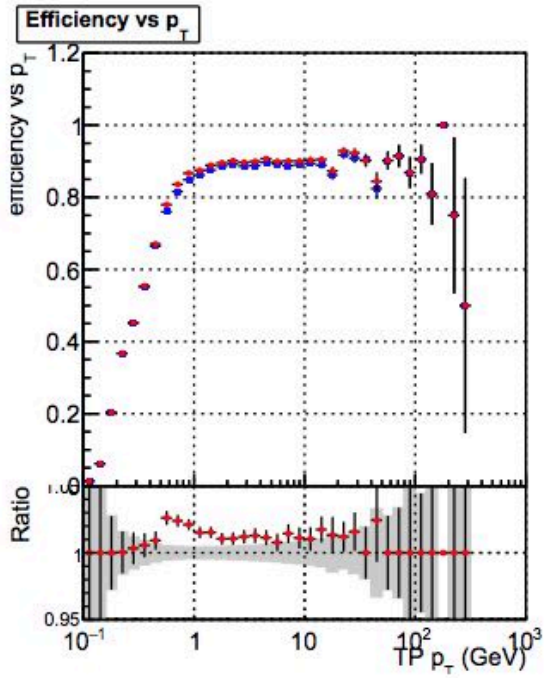
- Charge Collection
  - Loss of charge collection efficiency probably due to radiation damage

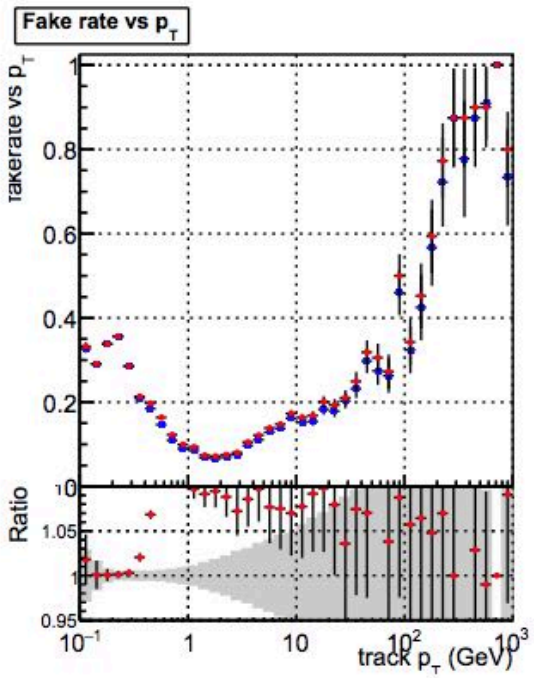




Tracking: PixelPairs

- Preliminary test to automated PixelPair mitigation
  - PixelPair originally used to cover BPix-FPix transition region covered only by 3 layers and the region with inactive areas in BPix layers 2 and 3

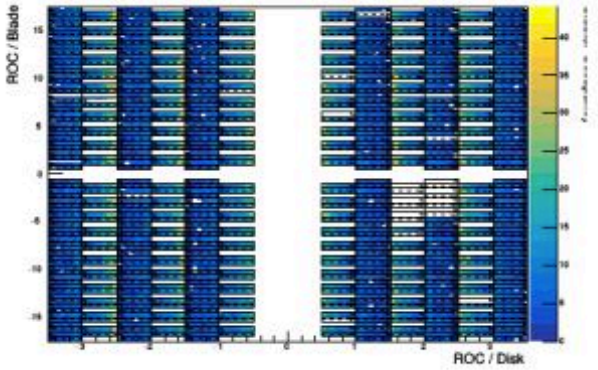


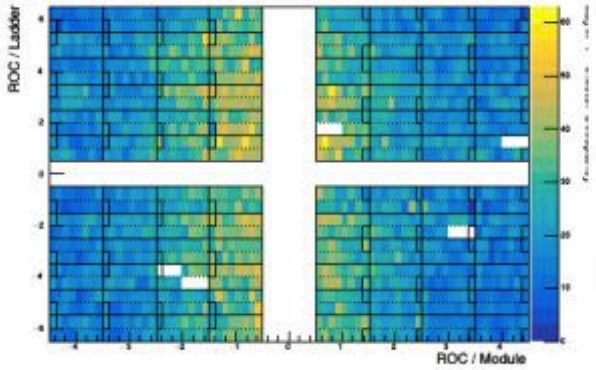


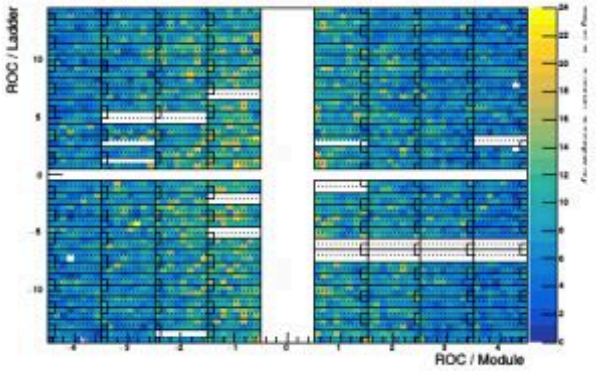
M. Kortelainen

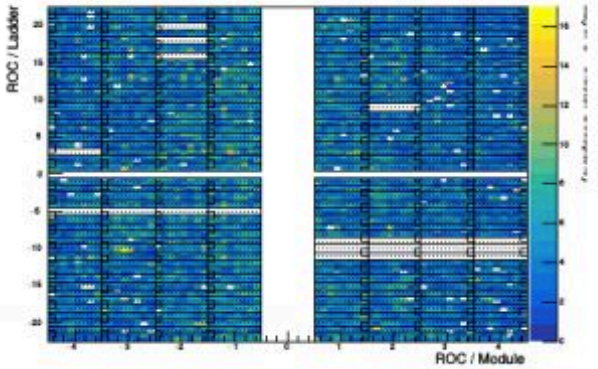
  - Noticeable improvement
    - Big part of the PixelPair improvement goes to reduction of strip seeds

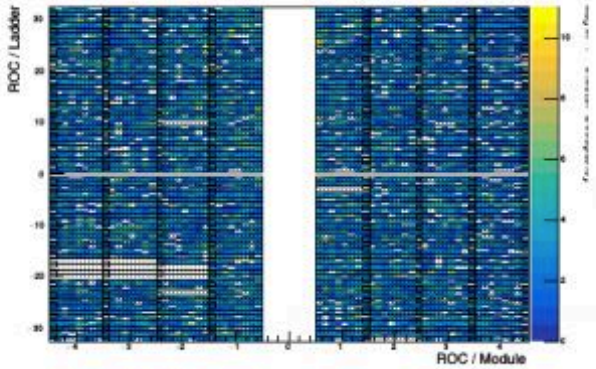
Failure Scenario Run 304366





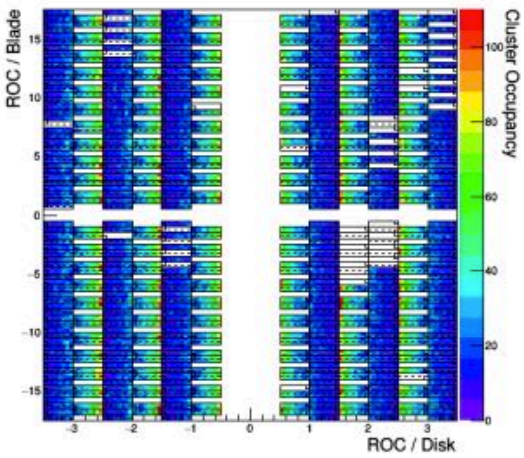


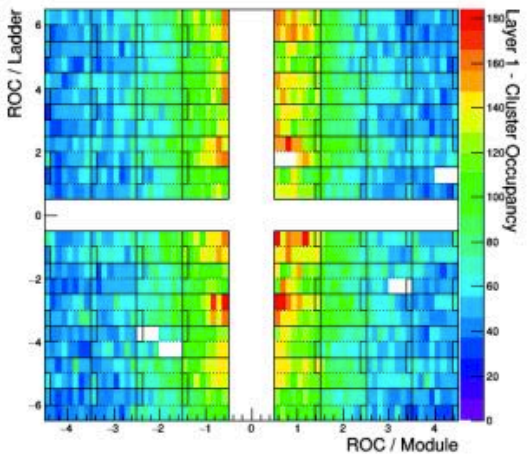


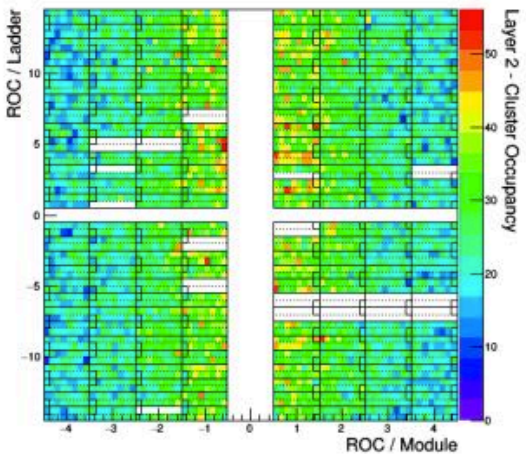


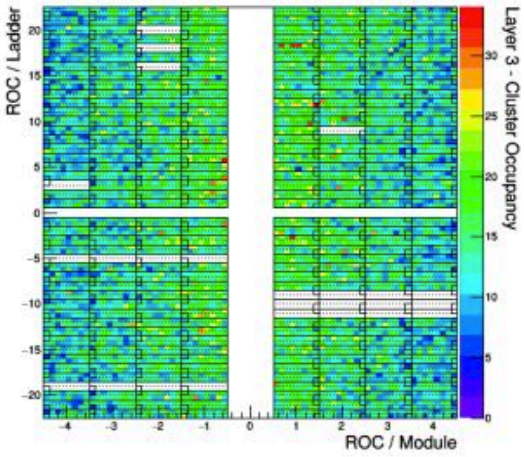
- October 4th

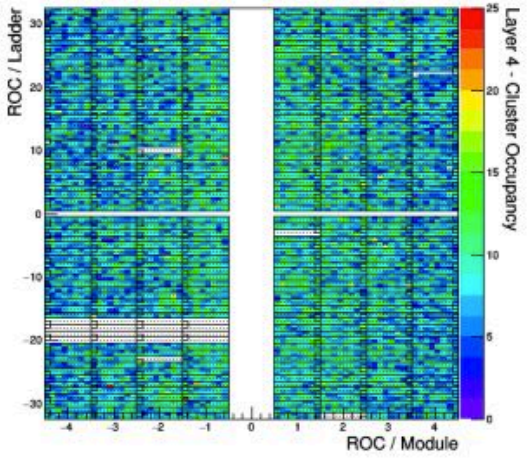
Failure Scenario Ideal





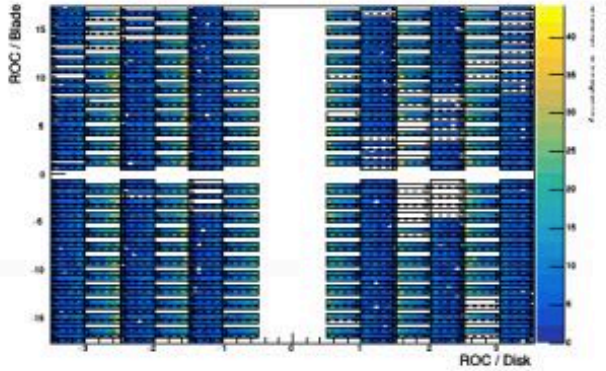


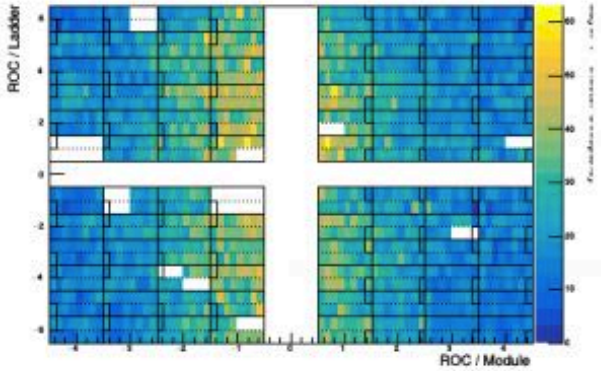


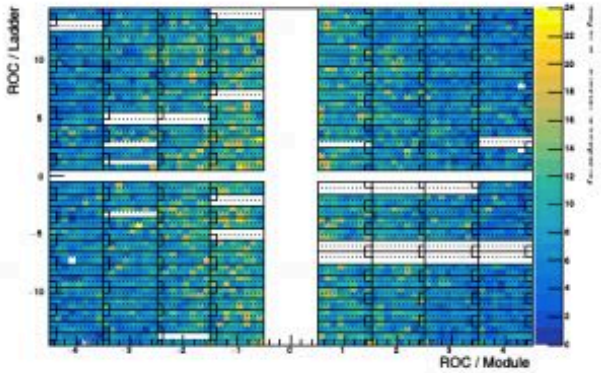


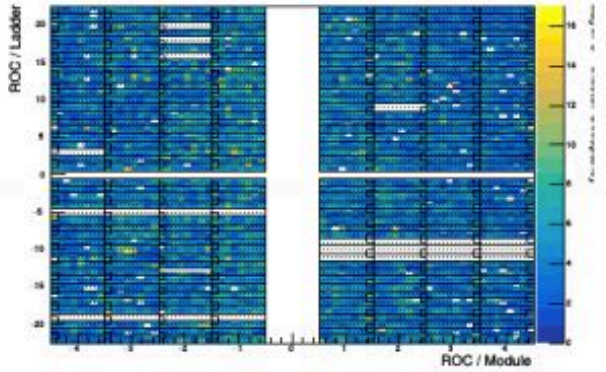
- SiPixelQuality v10

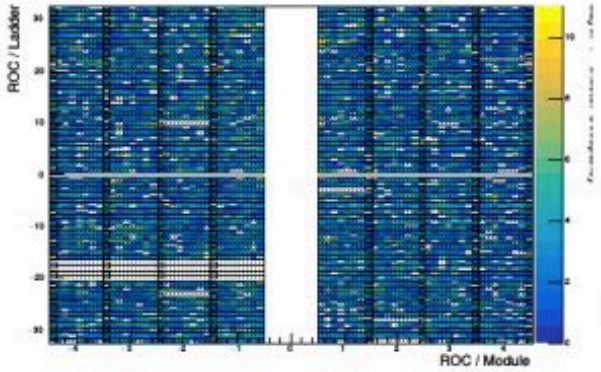
Failure Scenario Run 305044





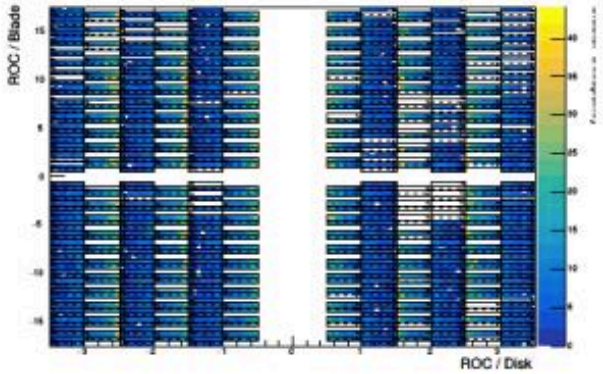


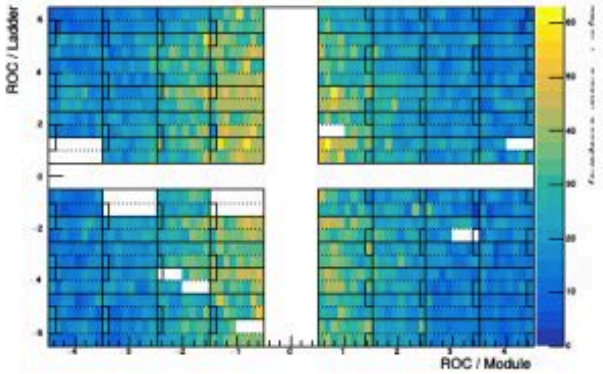


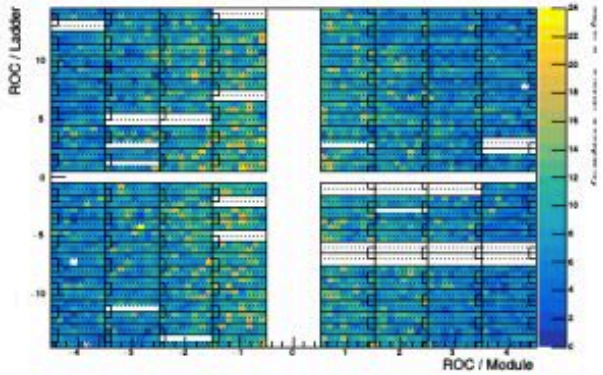


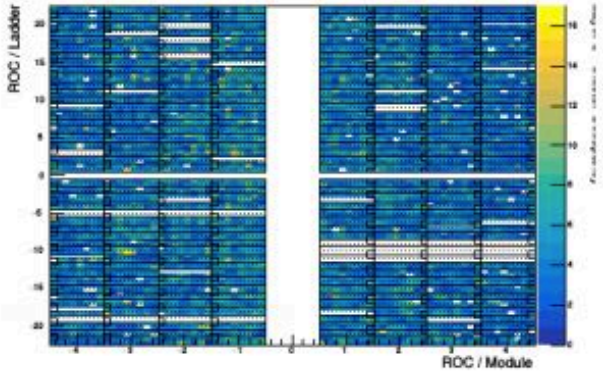
- October 13th

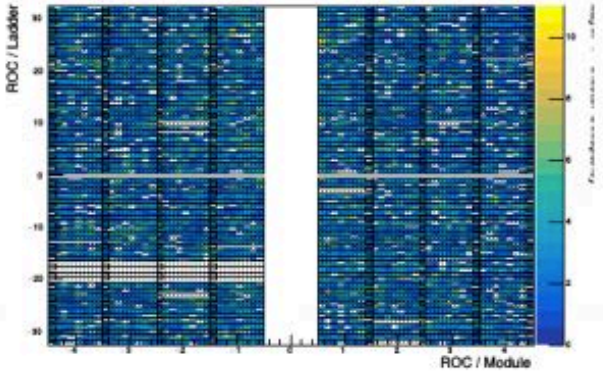
Failure Scenario Run 305081





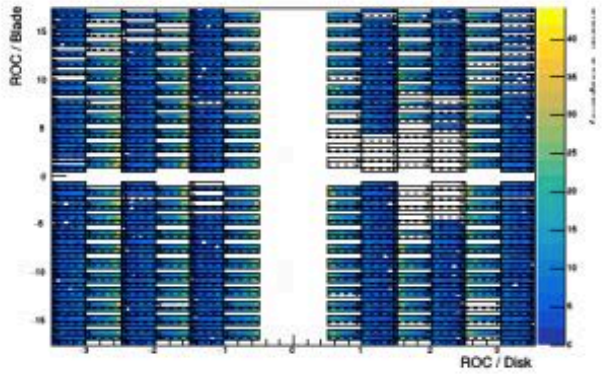


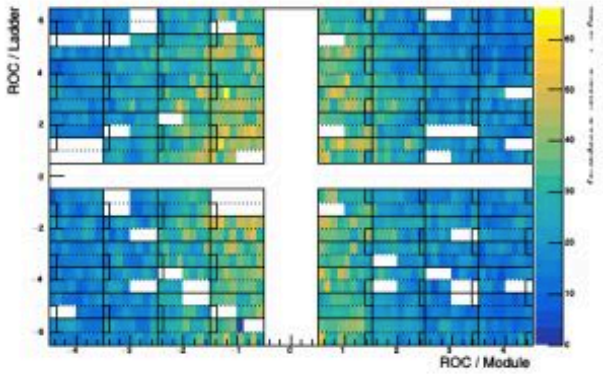


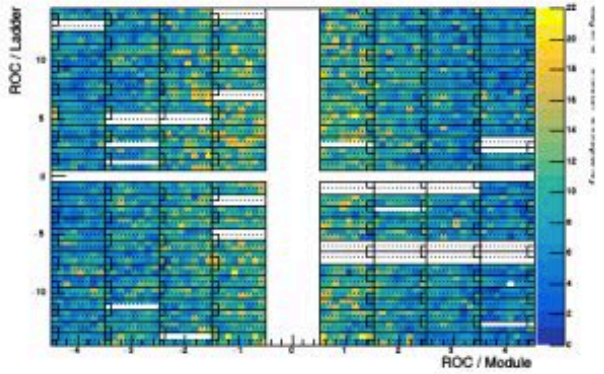


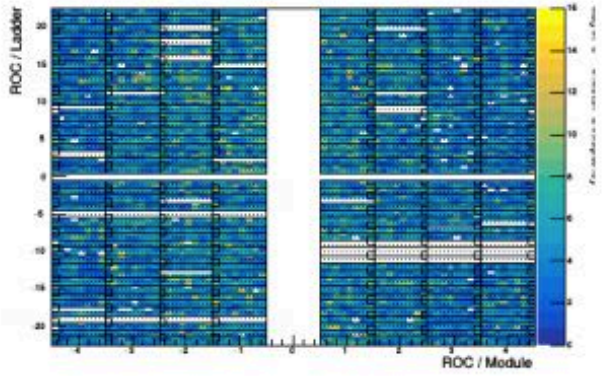
- October 15th

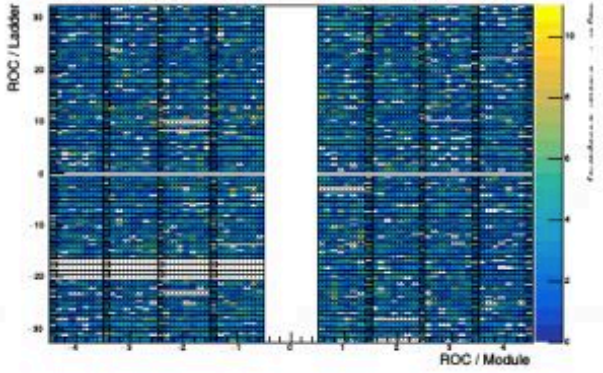
Failure Scenario Run 305064





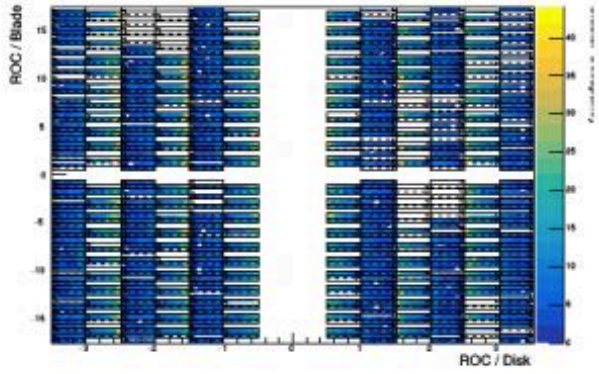


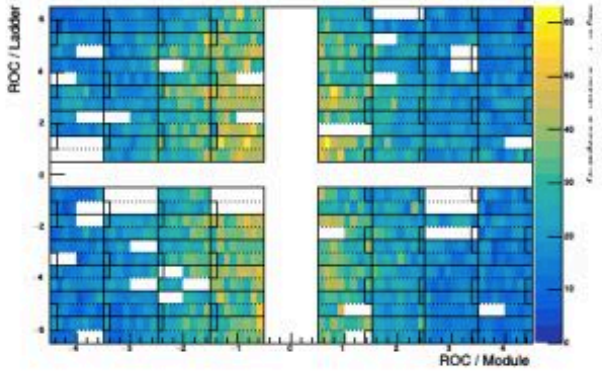


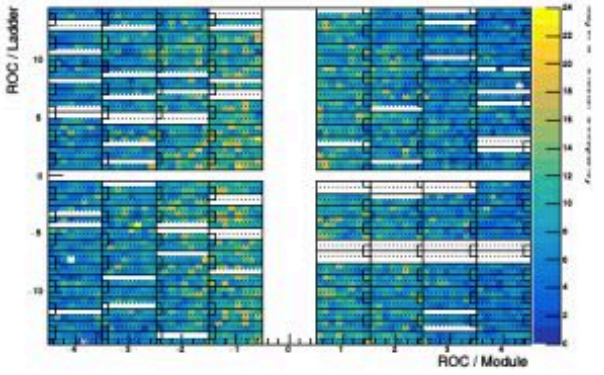


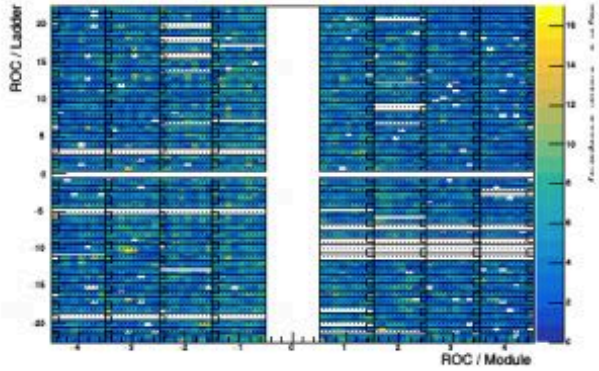
- October 15th

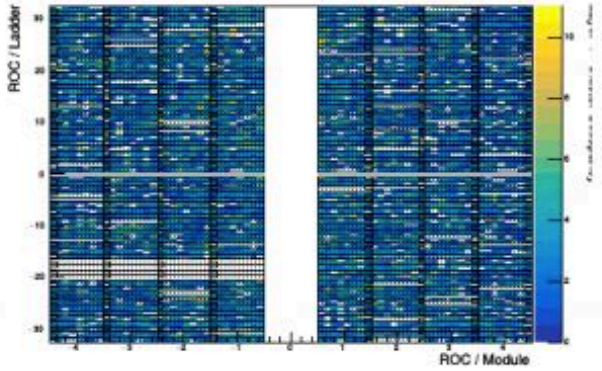
Failure Scenario Run 305366





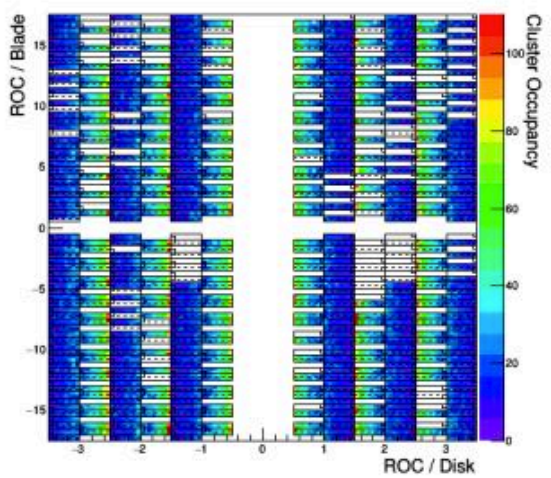


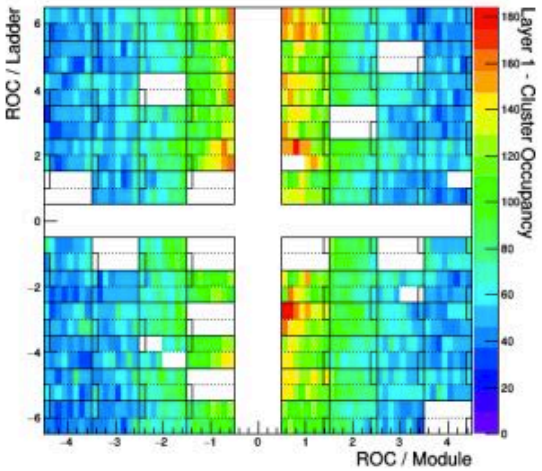


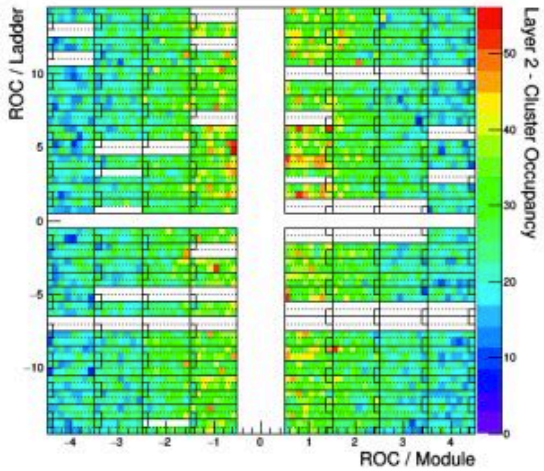


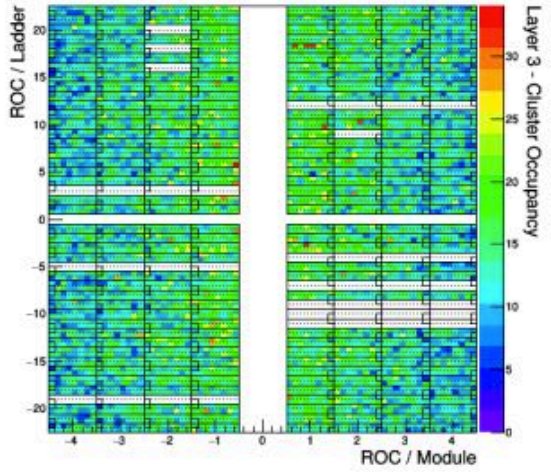
- October 21th

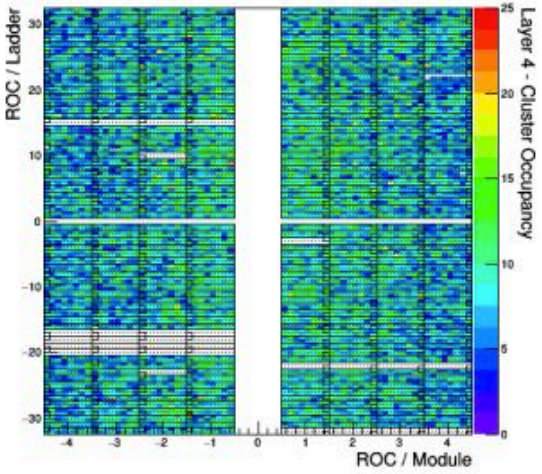
Failure Scenario v6











- (gu)Es(s)timated 2017 end

YETS Schedule

- Dec 22nd FPIX+ (2 quadrants) is extracted
  - US crew will be present
- Dec 22nd-23rd : broken DCDC converter(s) will be investigated
  - Aachen team at CERN, US crew, possibly FEAST designers
- Dec 27th-29th: tests and investigations of converters and one FPIX+ quadrant. Dismantling of the DCDC converters from 2nd quadrant
- Jan 2nd-20th: continue investigation, reworking and testing of FPIX+
- Jan 20th: BPIX and FPIX- are extracted
- ~Jan 20th: reworking of DCDC converters from the detector
  - Technician(s) from the company working at P5
- Jan 20th- Feb 4th: investigation, reworking, and testing of FPIX- and BPIX
- Feb 5th – 12th : reinstallation starts
- To be noted
  - The plan depend heavily on the findings when the first DCDC converters are available
  - BPIX and FPIX- will be repaired in parallel in the two labs at P5: second lab being prepared now.