I nostri impegni per il progetto MU FASE 2

Davide Piccolo (INFN Frascati), Cristina Riccardi (Università Pavia), Sandro Ventura (INFN Padova), Gianni Masetti (INFN Bologna)

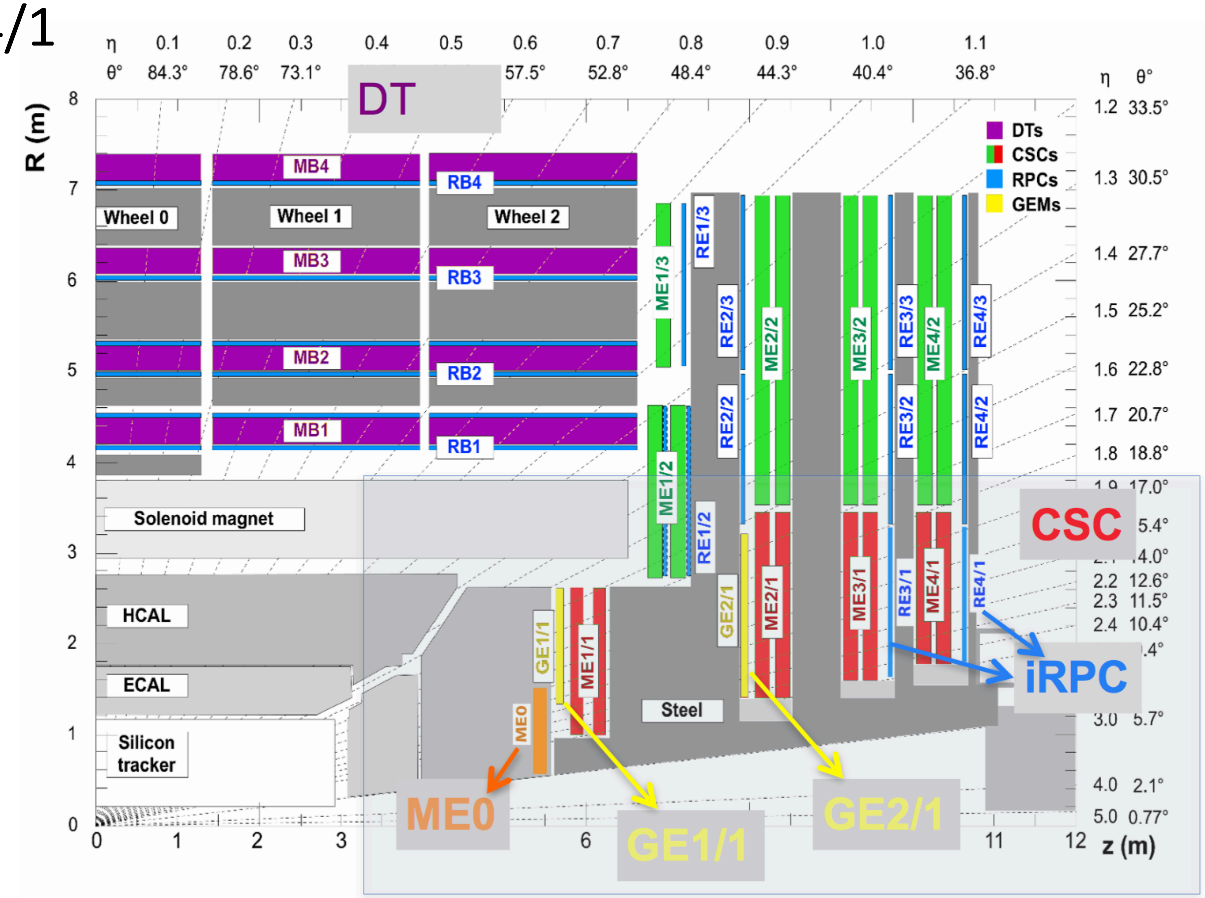
CMS Italia - Piacenza - 29 Novembre 2017

CMS muon upgrade scope

Goal: maintain excellent triggering, ID, and measurement of muons under harsher HL-LHC conditions (instantaneous and integrated L) up to |η|<3

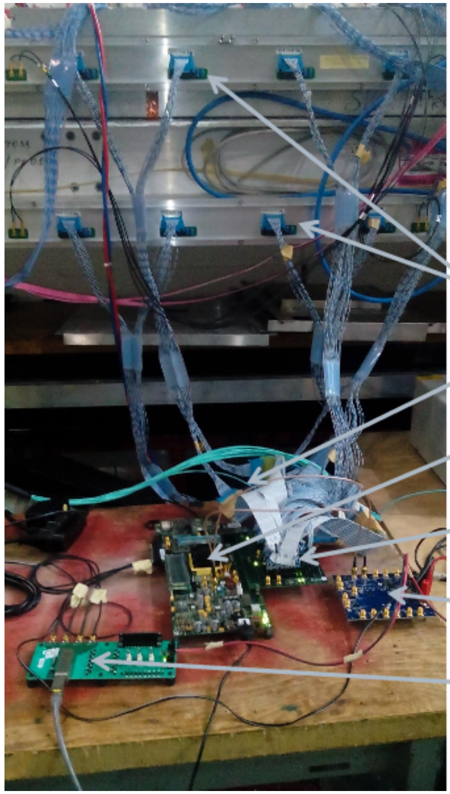
1. Existing detectors: consolidation of detector operation; DT, CSC and RPC electronics upgrade;
2. New forward muon detectors: GEM in GE1/1 (approved), GE2/1, and ME0; improved RPC in RE3/1 and RE4/1

- Consolidation of the detector operation at HL-LHC→ detector longevity from GIF++ R&D
- DT and CSC electronics replacement to handle longevity issues and L1 trigger (750 kHz) rate and latency (12.5 μs).
- Upgrade trigger/DAQ RPC system to handle longevity issues and be complaint to Phase2
- New forward detectors to handle most difficult region, with high background trigger and readout rates, and limited bending up to |η|<3

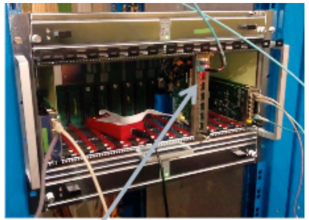


DT

Muon -DT FPGA demonstrator: firmware implementation of multichannel TDC - DT.RD.FE.1 – 5/12/2016



SX5 Setup



LVDS cables from Front End

10Gbps link to TwinMux

Virtex 7 Evaluation Board (138 TDCs)

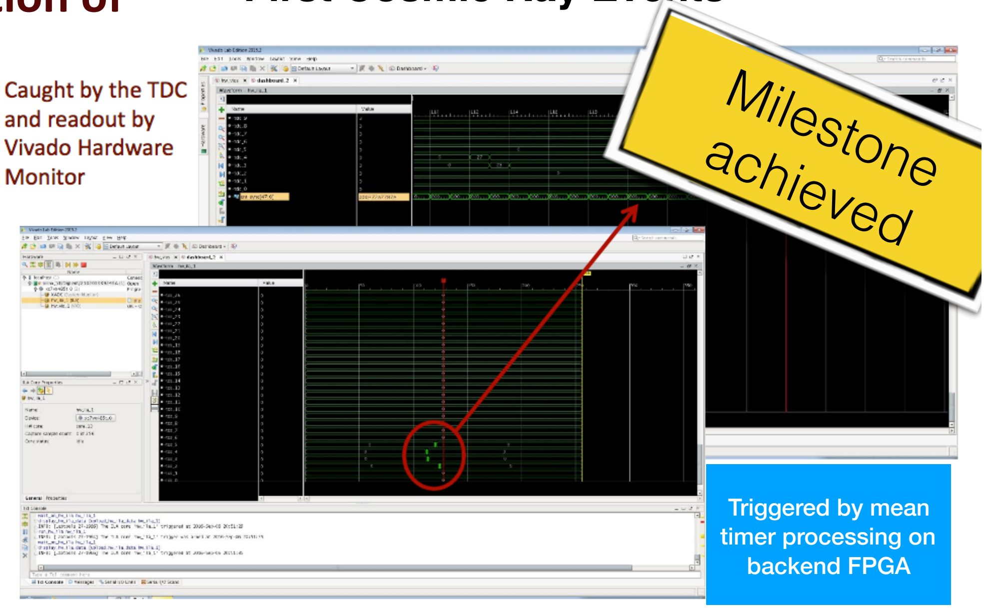
Input FMC mezzanines

LHC clock PLL (not conneted to TCDS yet)

Slow Control (Ipbus)

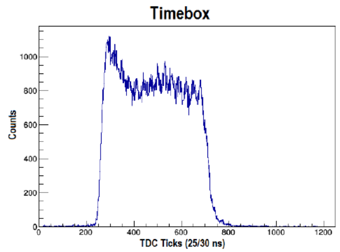
First Cosmic Ray Events

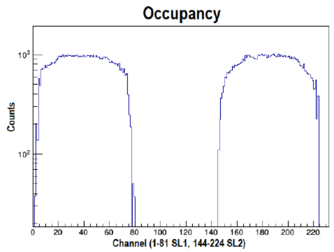
Caught by the TDC and readout by Vivado Hardware Monitor

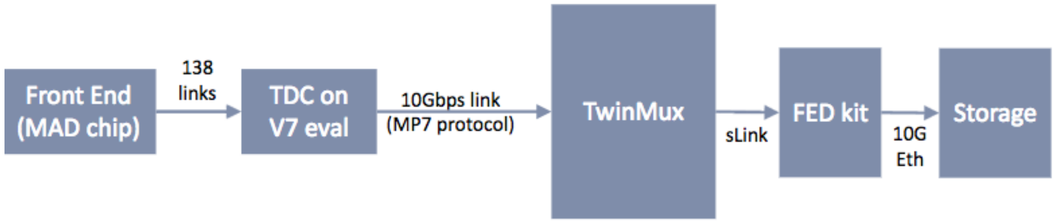


Triggered by mean timer processing on backend FPGA

CMSSW & DQM Integration



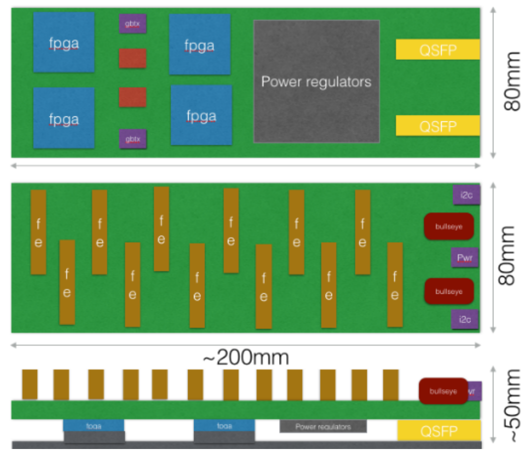




TDC on Virtex 7 architecture

An alternative firmware architecture,
based on ProAsic FPGA has also been qualified.

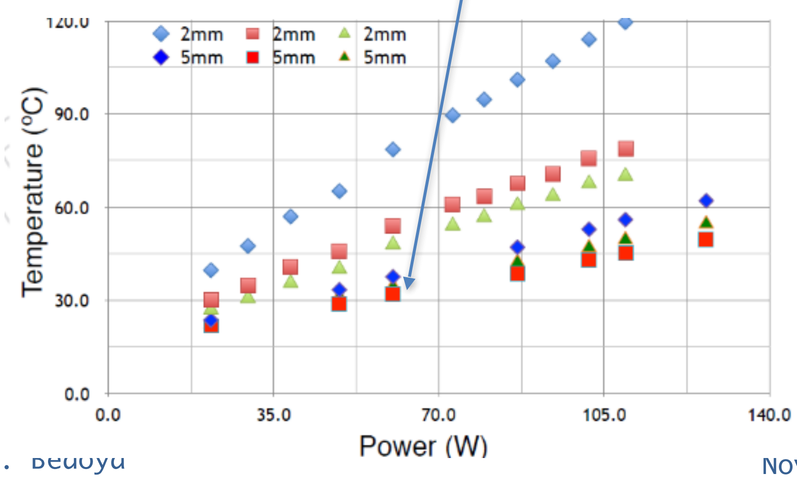
First Specs and PCB Layout for TDR

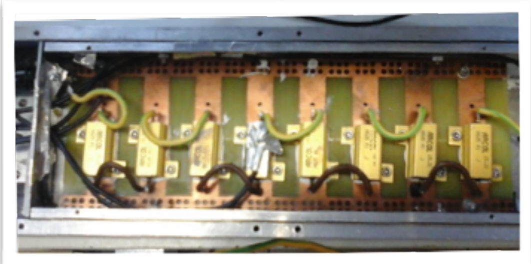


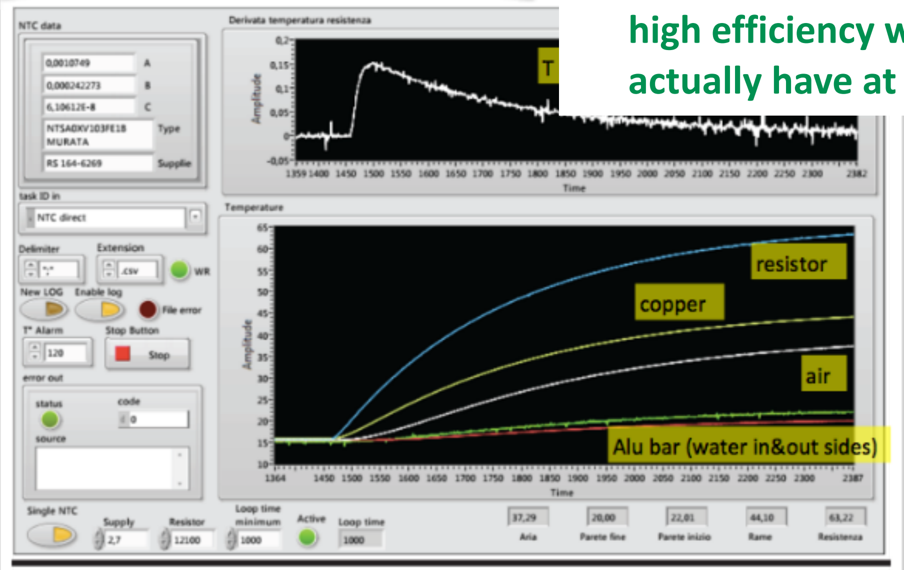
Design Evolution and optimization

COOLING TESTS

Dissipation works fine up to 90 W → good for expected 60 W power consumption







Tried different configurations (cooling flow, positions, etc)

In both cases ("Attach" & "empty" options) the old MiC extrusion can cool down the new electronic with high efficiency with the same flow we actually have at P5.

Decided to settle on Attach baseline for mechanical design

Design Evolution and optimization

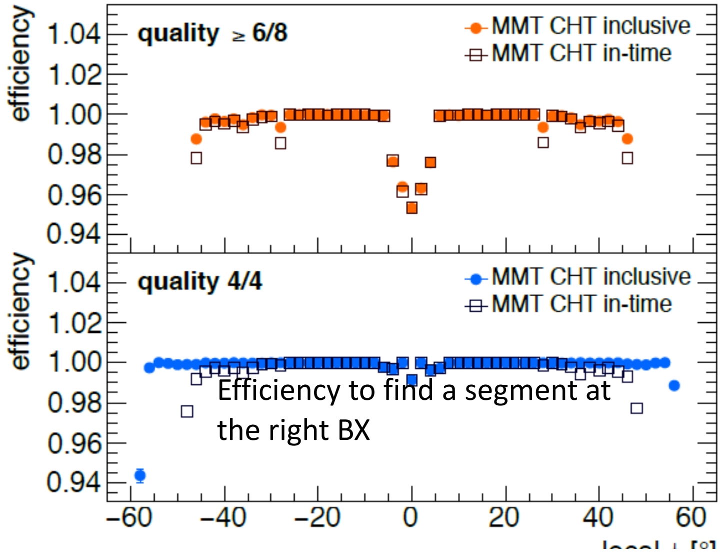
Milestone achieved

		ID	Milestone title	
Design	√	DT.RD.FE.1	DT FPGA demonstrator: firmware implementation of multichannel TDC done (HM)	5.Dec.20
	√	DT.RD.BE.1	DT simulation: demonstration of L1 trigger pattern-recognition performance from DT TDC output done (HM)	11.Jan.2017

TRIGGER SIMULATION

Various approaches under study:

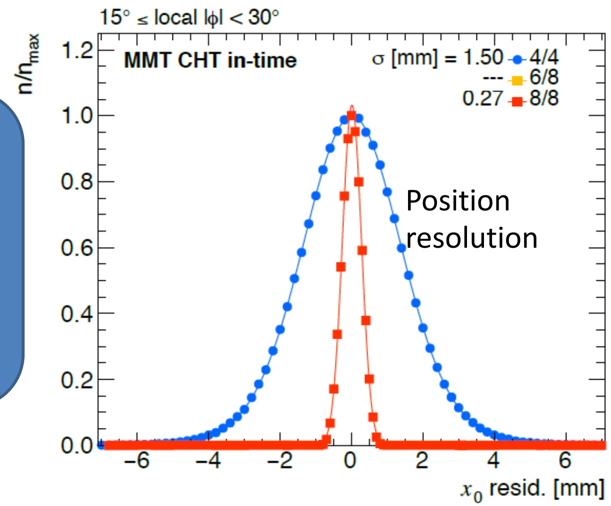
- BTI-based + expansion to 8 layers
- histogram based meantimer + chamber level track segment with Compact Hough Transform



- The algorithm matched the efficiency and resolution from current BTI-TRACO local DT trigger
- Final algorithm should evolve to include better handling of chamber inefficiency and best combination with Track Finder

Final decision will be taken by the time of the Trigger TDR in 2019, once the full trigger chain architecture is defined.

At present, activities ongoing to provide proof of BX identification and multilayer track fitting in the Phase-2 environment.



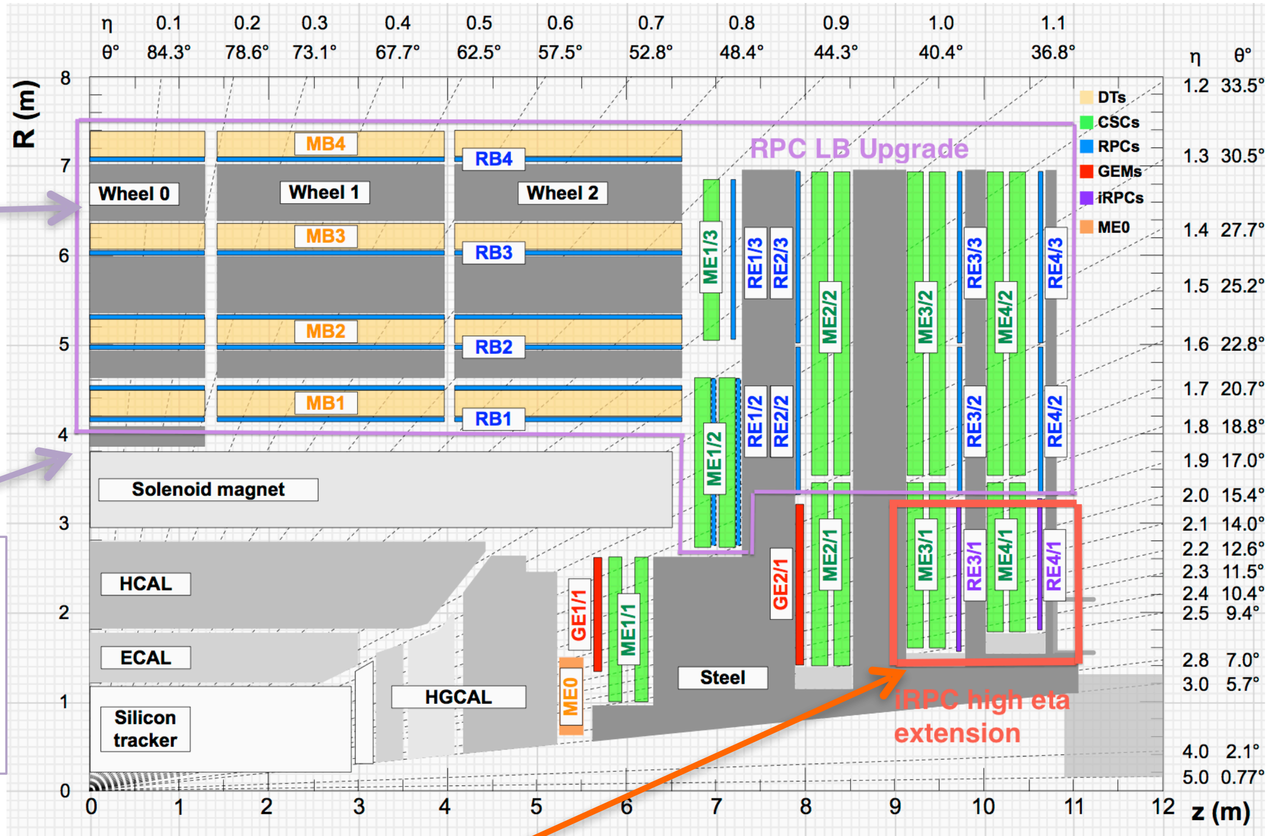
RPC

The RPC Upgrade project

Installation in LS3

Upgrade of Link System
off-detector electronics,
for present system RPC (|η | < 1.9)
- **Longevity of the electronics**
- **improved time resolution (1.5 ns)**

Longevity of the present system:
RPC (|η | < 1.9)
Max exp. rate: 200 x 3 hz/cm²
Max exp. Int. charge: 270 x 3 mC/cm²

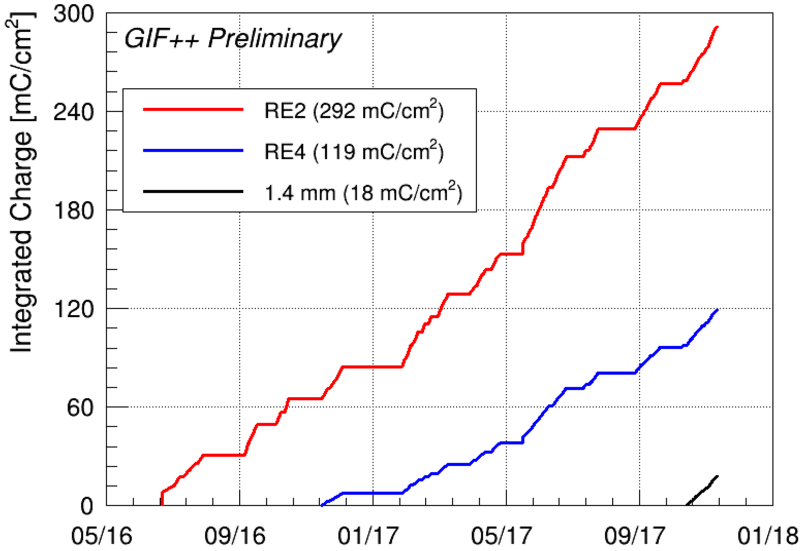


Extend the RPC coverage up to |η | = 2.4 to increase redundancy in high eta region in stations 3 and 4

Installation in YETS21 & 22

Longevity of the present system at GIF++

Integrated charge time chart

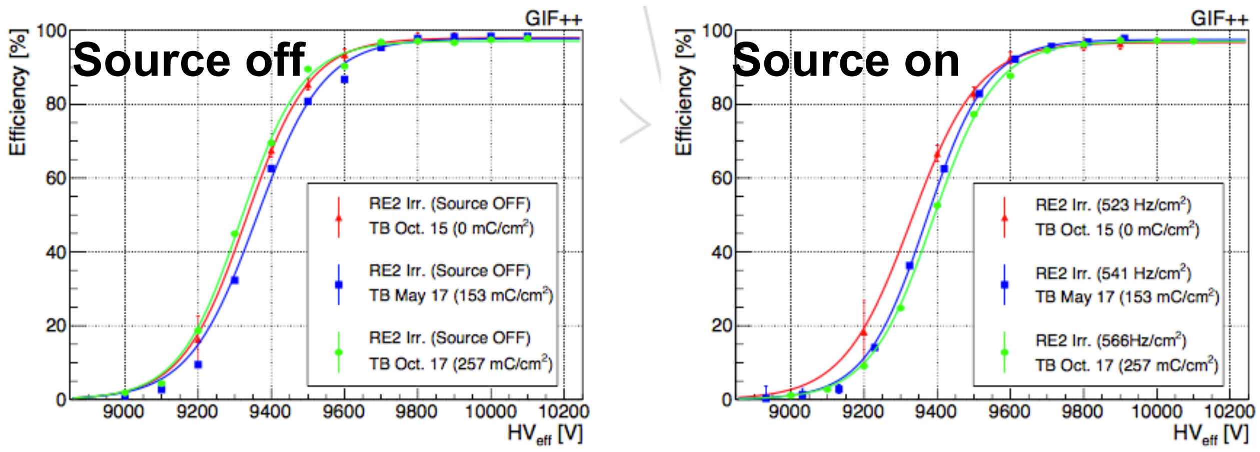


Integrated charge @ 11/2017:
292 mc/cm²

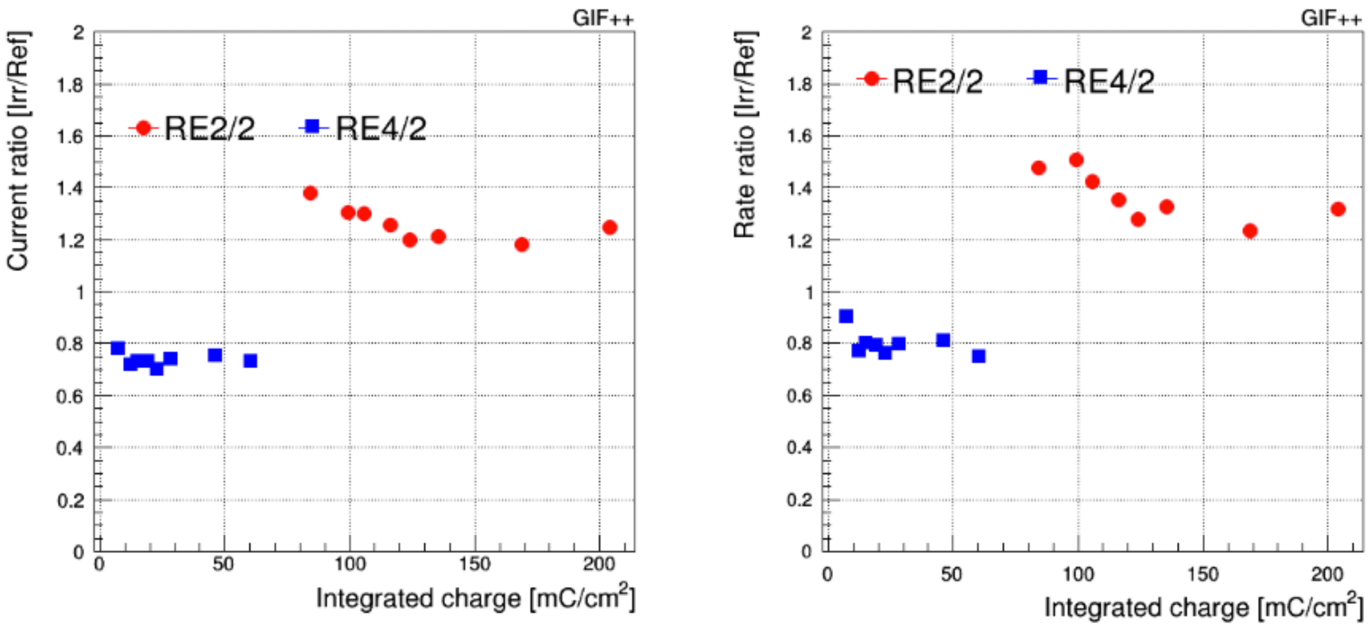
Integrated charge goal:
270 x 3 mc/cm² = 840 mc/cm²

Expected end of test:
End of 2018

Eff vs Hv_{eff} after different integrated charge



System stability vs integrated charge

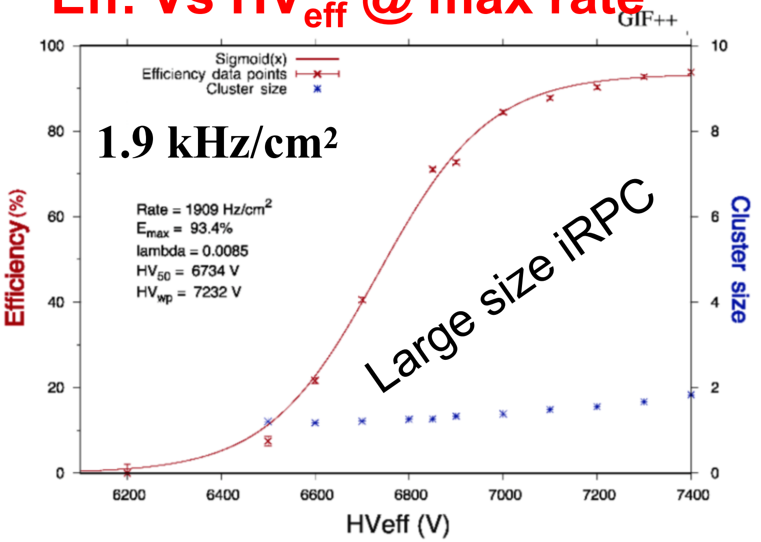


Extended RPC coverage with iRPC: RE3/1 – RE4/1

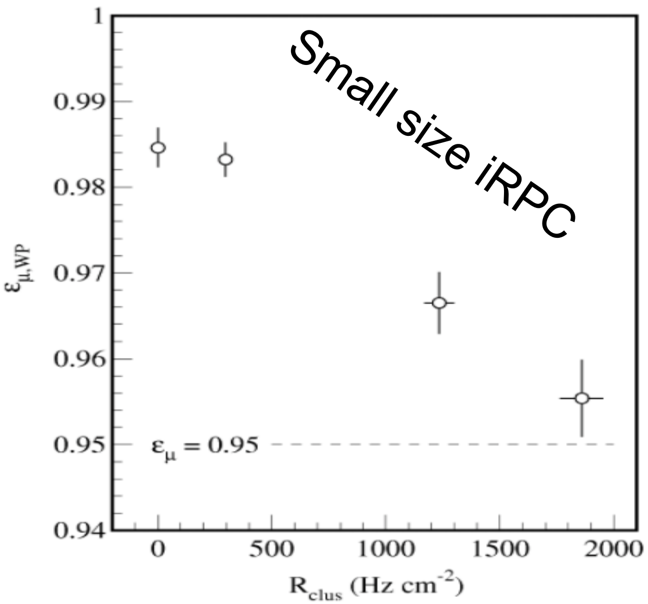
System parameters	Present system	RE3/1-RE4/1 (iRPC)
|η| coverage	0 - 1.9	1.8 – 2.5
Max. expect. Rate (Hz/m²)	3 x **200**	3 x **700**
ϕ resolution	~ 0.3 degrees	~ 0.2 degrees
η resolution	O (20 cm)	O (2 cm)

Detector parameters	RPC	iRPC
HPL thickness	2 mm	1.4 mm
Gas Gap width	2 mm	1.4 mm
Resistivity (Ωcm)	1 - 6 x 10^{10}	0.9 - 3 x 10^{10}
Charge thresh.	150 fC	50 fC
η segmentation	3 η partitions	2D readout

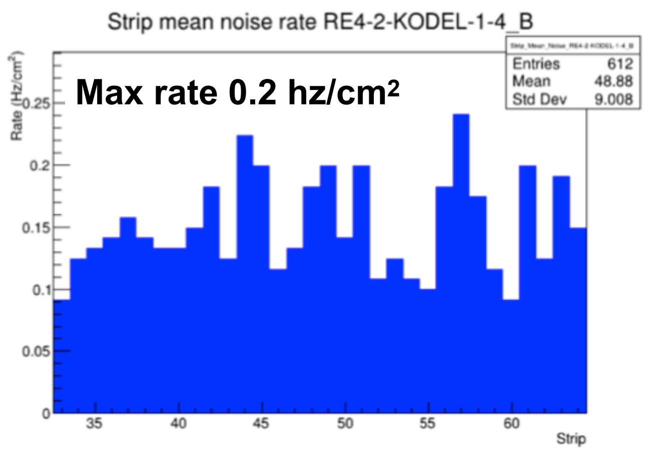
Eff. Vs HV_{eff} @ max rate



Efficiency @ W.P. vs Rate

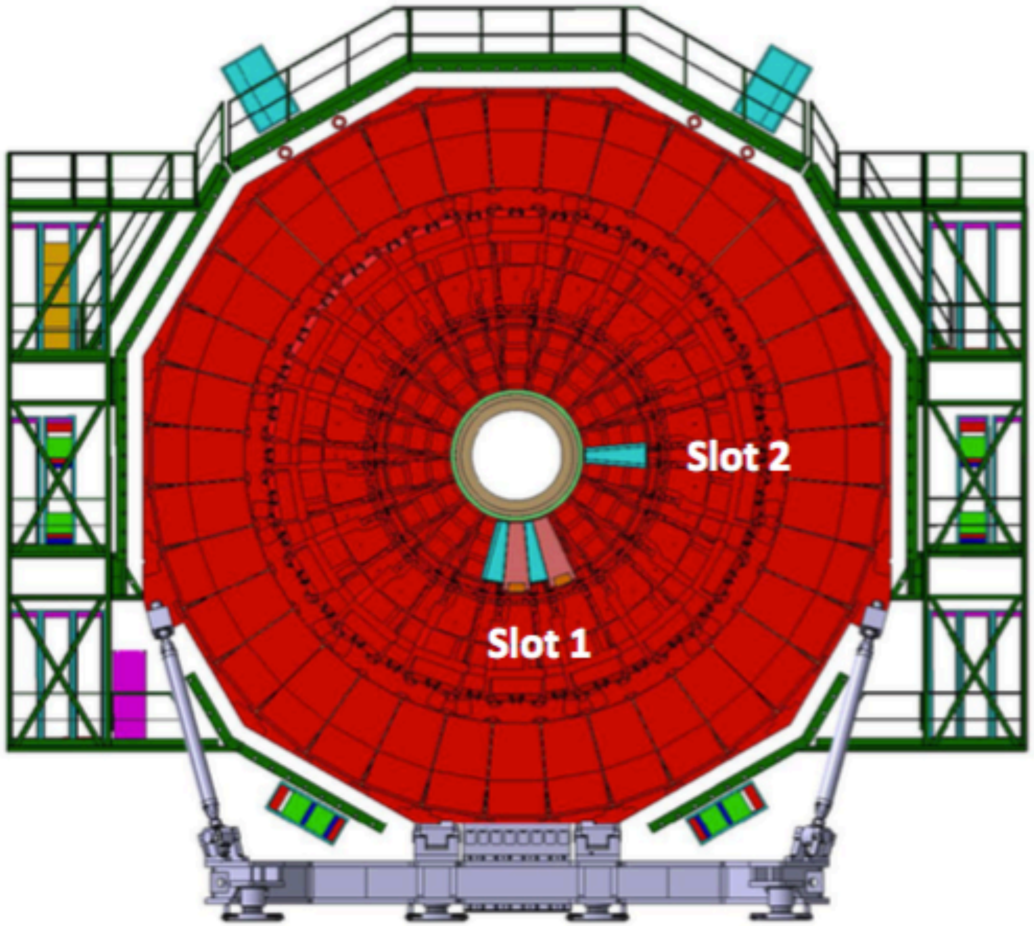


Noise rate @ W.P



GEM

GEM Slice Test @ P5



- LHC delivered ~ 50 fb^{-1}
- Total area : 3 × 10^4 cm^2

Status of the detectors:

- Gas and cooling systems fully operational and stable; HV and LV proved a stability of the order of 1% with and without beamin the automation system under test

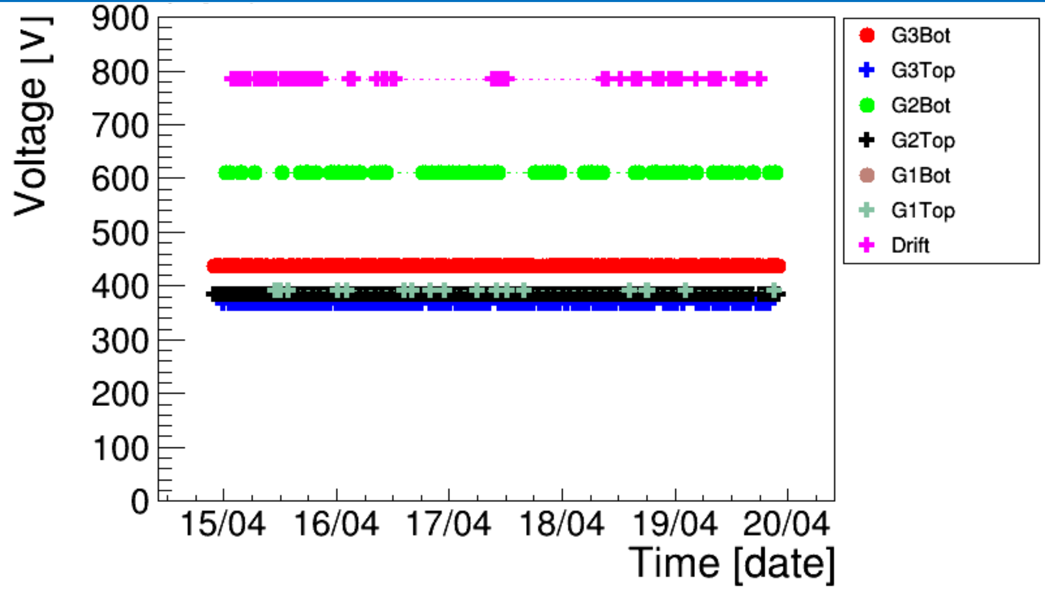
5 Super Chamber (each formed by 2 GE1/1 Triple-GEM chambers) installed in YE-1 in January 2017 and in operation since May 2017

HV and LV systems:

- **Slot1 → 4 SCs are powered with a single channel HV power supply**
- **Slot2 → 1 SC is powered with the multichannel HV power supply, with 7 channels per chamber**
- **The LV system foresees 3 LV channels for each SC: 1 to power the GEB/VFAT, 2 to power the Optohybrids**

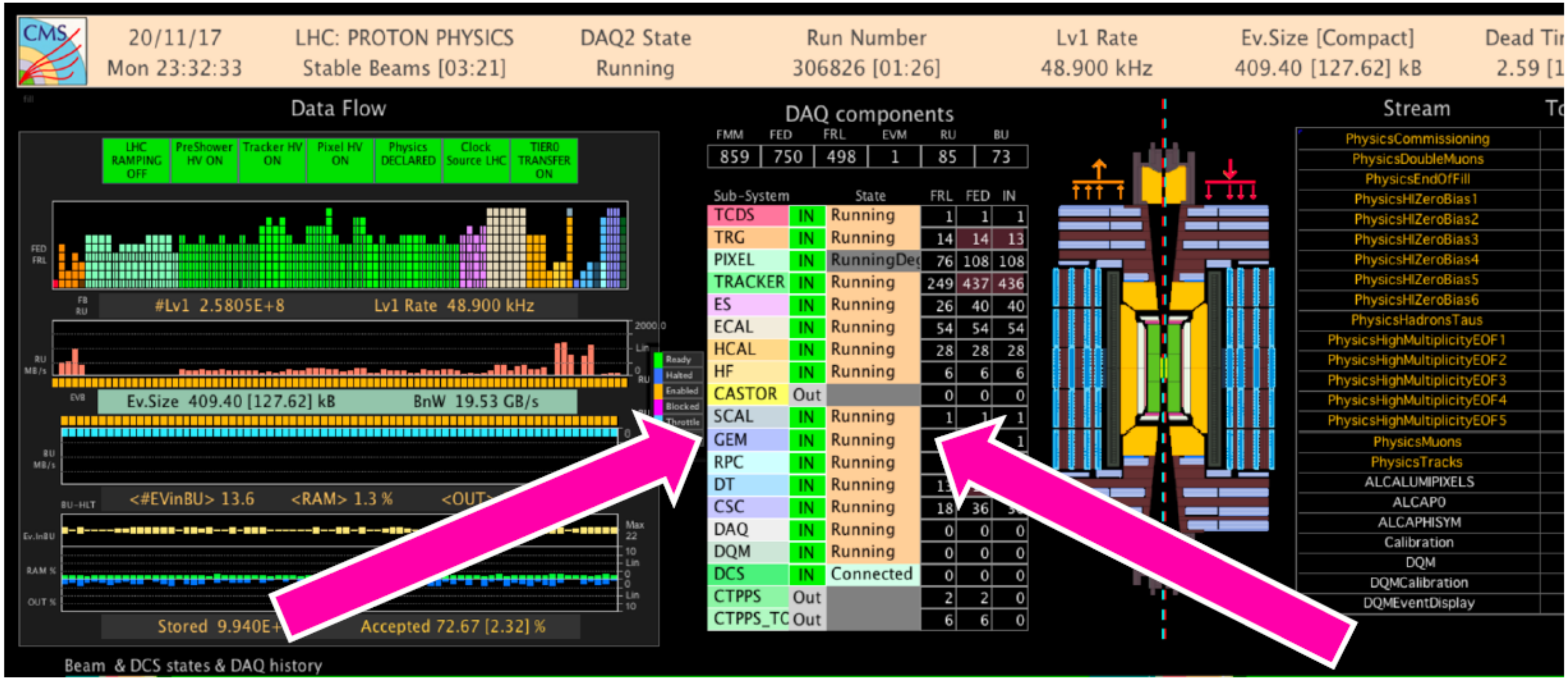
Gas & cooling systems:

- **3 gas lines with Ar/CO2 70/30 gas mixture**
- **3 lines for cooling systems**



GEM in Global Run with collisions

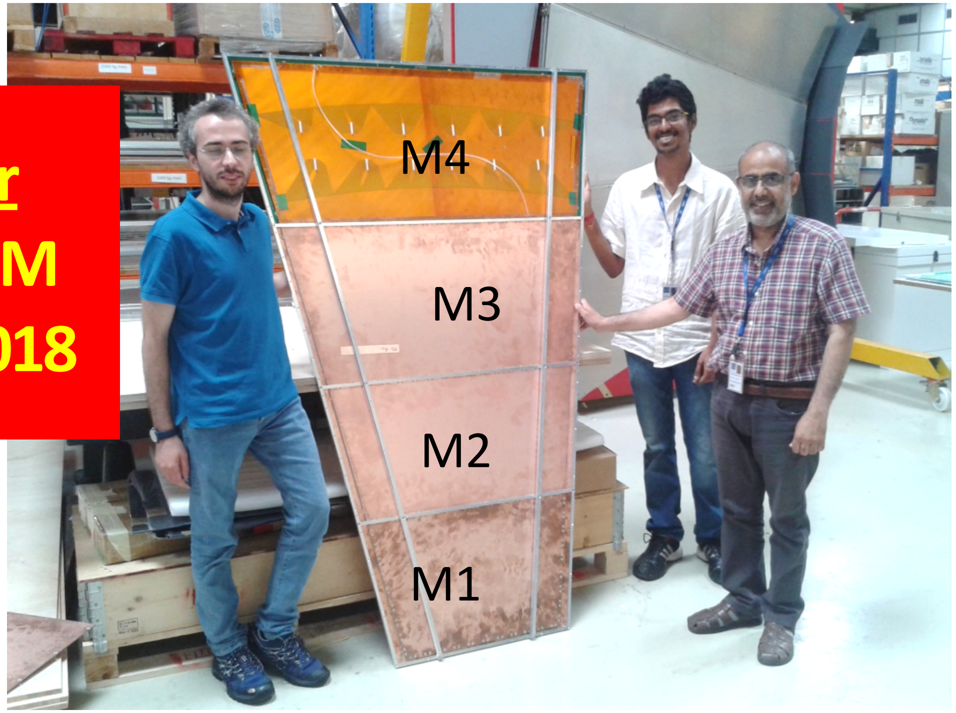
On Monday, November 21st, we were included in global during collisions (5 TeV) for the first time.



- **DAQ integration:** Local system operational; First run in Global with cosmics and with collisions in the last few days; High rate tests ongoing
- **DCS integration:** Local version of the system completely operational; Protection system, aimed at moving the system in a safe state during injection and magnet ramping, programmed (tests ongoing) ; Integration in the automation system under test

GE2/1 Prototyping

First GE2/1 <u>Chamber</u> Prototype (triple-GEM technology) June 2018



GE2/1 <u>full size</u> Prototype (triple-GEM technology) Sept 2017

1 active M4 prototype module

3 dummy modules (M1, M2, M3)

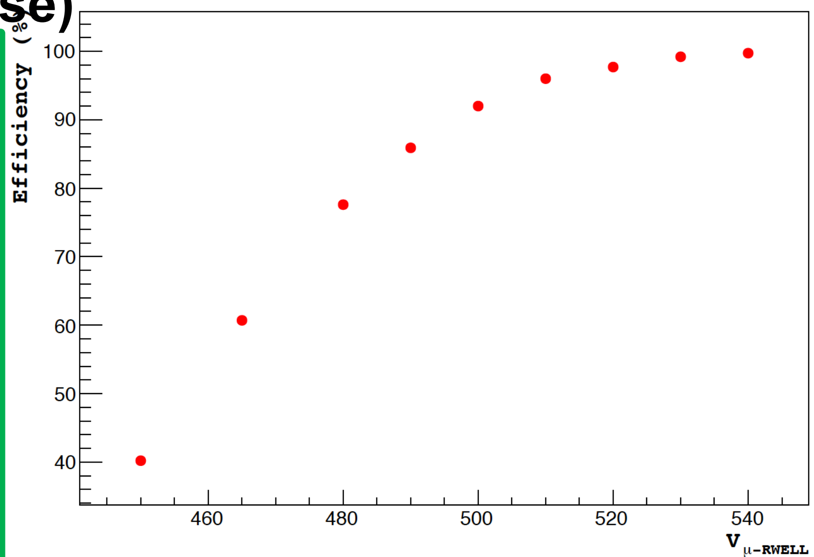
Structure proves to be mechanically stable as expected

GE2/1 20⁰ sector with M4 μRWells (July 2017)

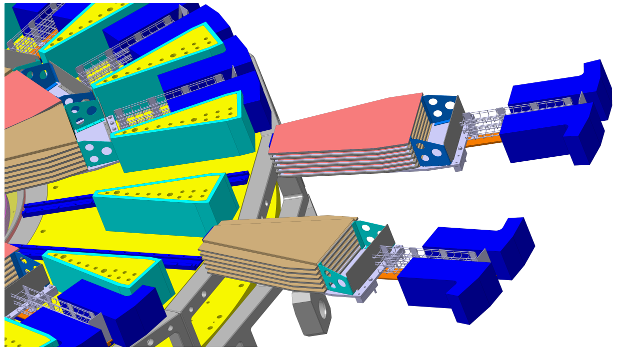
(M4: 2m height, 1.2 m base)

<u>H4 test beam with 150 GeV muons:</u>

- **Voltage scan → Efficiency 98-99%**
- **Excellent uniformity across the surface of the detector at 530 V (~10000 gain)**



ME0 design implementation



Granularity and number of layers optimized considering 200 pile-up interactions and latest evaluation of neutron background in the ME0 region

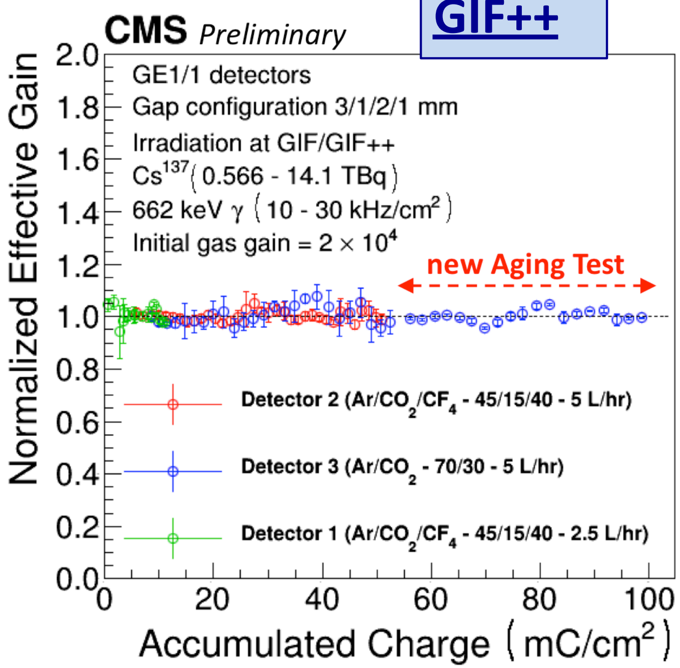
A baseline design of the ME0 detector is 6 layers of GEM chambers in Δϕ=20°

ME0 ageing test: 240 mC/cm² of integrated charge needed to fully validate ME0

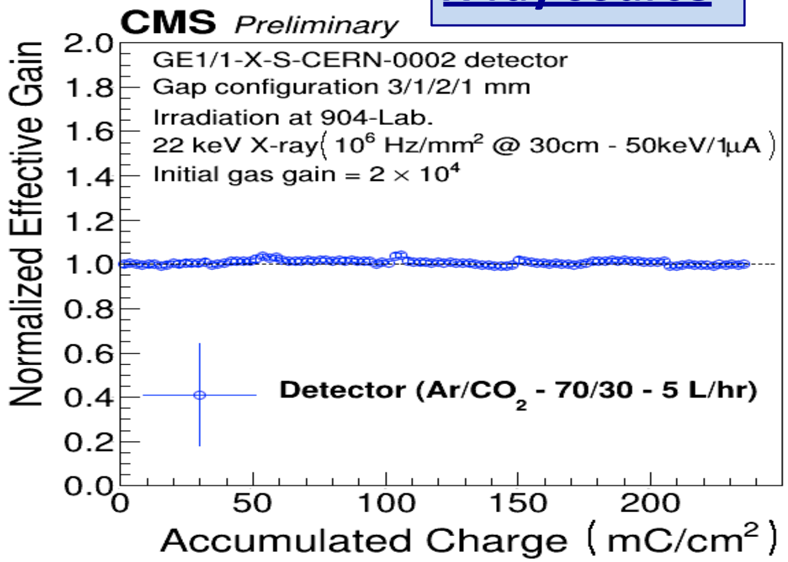
- @GIF++ no aging observed up to 100 mC/cm²
- X-ray source: ~factor 8 compared to the GIF++

in May 2018 expected integrated charge of ~ 840 mC/cm² with safety factor ~3 with X-ray

GIF++

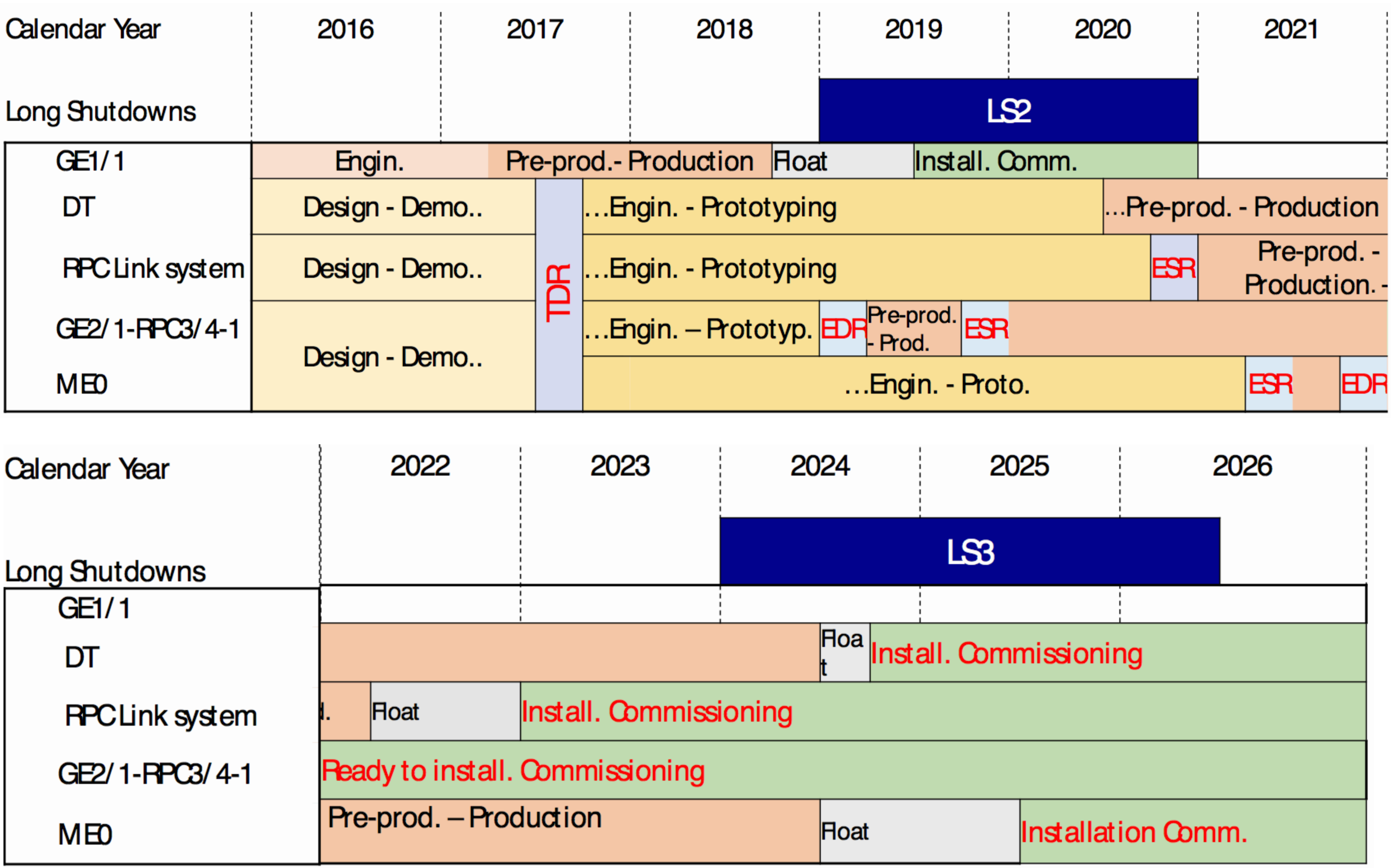


X-ray source



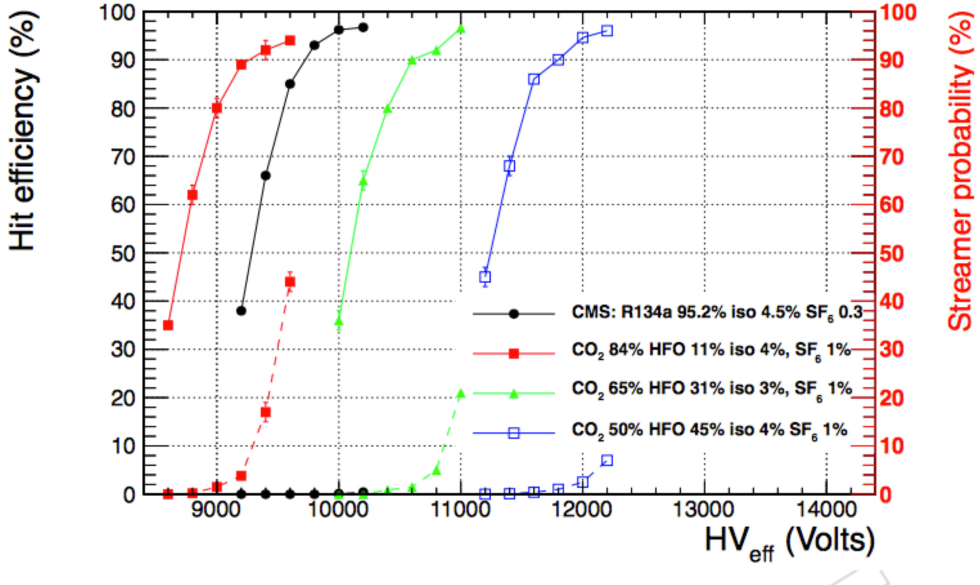
ME0 Discharge probability: test on 8-15 Nov 2017 @ CHARM – Analysis on-going

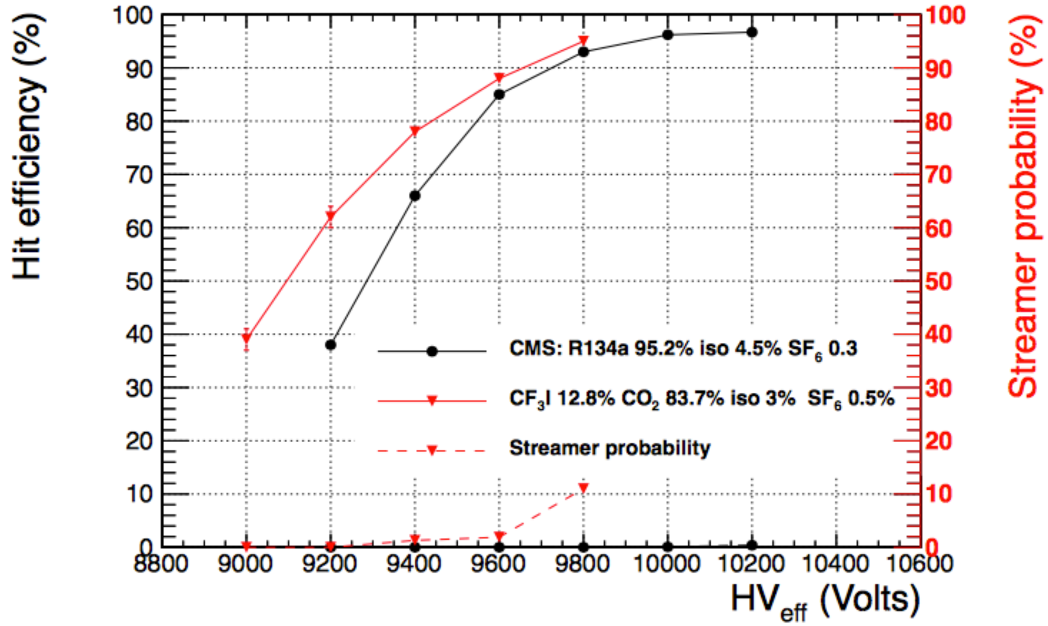
Muon upgrade timeline

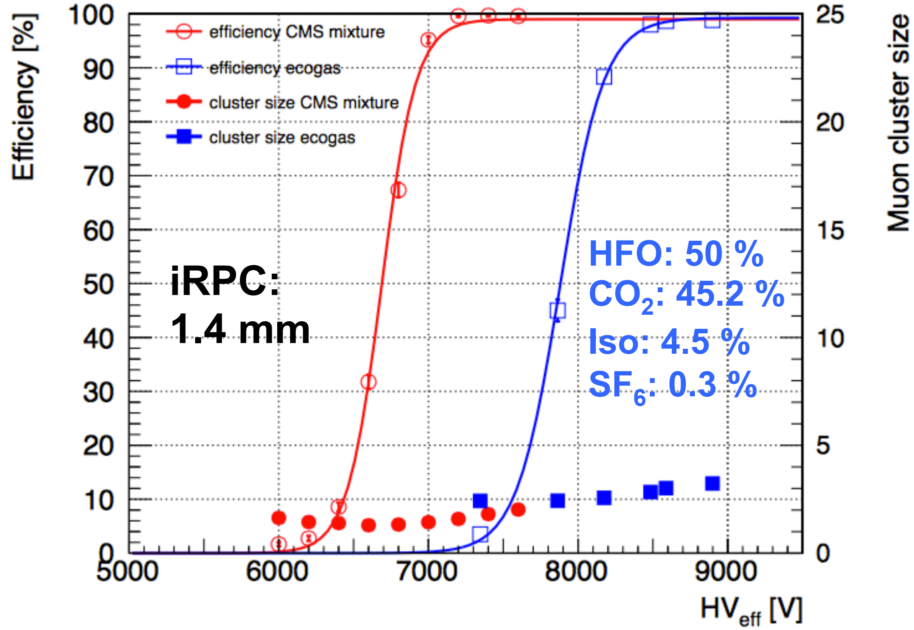


backup

Eco-gas studies







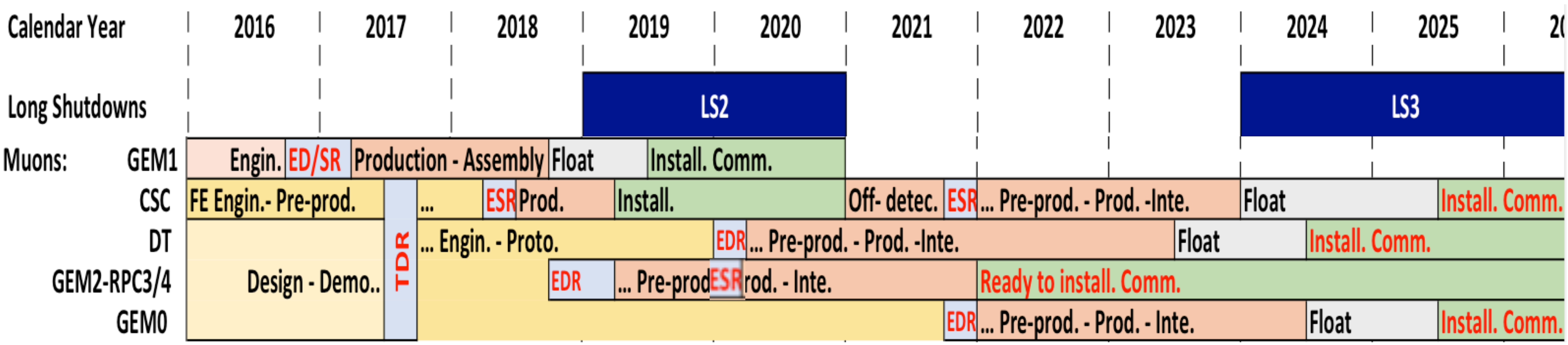
Eco-gas mixture:

Possible candidates found (blue curves in the plot):
not the best -> work in progress
GIF++ tests in preparation to study longevity

Alternative strategy:

a recuperation system for the CF6 and C2H2F4 would be developed and installed allowing re-use of the RPC exhaust gas.
A commercial abatement system to burn off the RPC exhaust gas will be considered.

Muon upgrade timeline



- GE1/1 Technical Design Report (TDR) approved as being the first CMS Phase II TDR, following the need of early operation in LS2.

- Muon TDR Q4-2017: Design and demonstration phases for Detectors and Front-end electronics Upgrade by Q4-2017

- CMS upgrade activity optimization requires
  - Anticipation of CSC Front-end upgrade in LS2
  - Installation of GE2/1 and RE3/1-RE4/1 detectors in Extended Technical Stops before LS3

- DT electronics, CSC back-end electronics and ME0 upgrade in LS3