Technologies and design solutions for tracking (in 4D) at high pileup

HL-LHC and beyond

Outline

- What we (= CMS) have invented / learned / understood from the developments for HL-LHC
 - And what we will learn in the remaining 2-3 years of developments
- What others have invented (selected topics)
- > Other new technologies on the horizon (... or beyond...)
- > What will be useful in the far future, in extreme pileup conditions?
- Some intermediate targets?

Scope of the Upgraded Tracker



- In a nutshell, the main enhancements of the Upgraded Tracker are:
- Increased radiation tolerance to survive beyond 3000 fb⁻¹ (plus margin)
 - With the possible exception of the layer/ring 1
- Increased granularity to enable fast and efficient pattern recognition up to 200 PU
 - Interplay with computing time
- Contribute tracking information to CMS L1 trigger decision, to enable effective event selection up to 200 PU
 - New trigger operation parameters: Latency 3.2 μ s \rightarrow 12.5 μ s, Accept rate 100 kHz \rightarrow 750 kHz
- Extend rapidity acceptance up to $\eta \approx 4$
 - Cover the peak production region of jets from Vector Boson Fusion and Vector Boson Scattering
 - Mitigate assignment of charged tracks to wrong vertices at high PU, affecting jet reconstruction and missing E_T



Radiation levels depend essentially on R, not much on z

The target is ~ 10× present tracker

• i.e. about 10¹⁵ neq/cm² for the Outer Tracker, > 2×10¹⁶ for the innermost pixel layer

> Challenging for silicon sensors and electronics (notably in the pixel region)

Unprecedented levels!



Sensors for Outer Tracker

- After heavy irradiation (~10¹⁵) charge from 320 µm thick sensors drops down to the same level as 200 µm
 - More trapping
 - In 200 µm the leakage current is smaller, and can be operated at smaller V_{bias}: mitigate requirement on cooling!
- In p-in-n sensors observed spurious signals (random non-gaussian noise, a.k.a. Random Ghost Hits)



N.B. Typically 25000 e- from a non-irradiated sensors 320 µm thick

Understanding RGH

- T-CAD simulations show higher electric fields at the strip edges for irradiated p-in-n sensors than for n-in-p sensors
 - ⊙ Suggests the occurrence of "micro-discharges" in p-in-n
- Increasing oxide charge...
 - ⊙ increases max. electric fields in p-in-n, reduces max. electric fields in n-in-p
 - Observation: rate of RGHs are smaller for neutron than for proton irradiation
 * less ionization, less surface damage







Outer Tracker sensors: conclusion

Basic R&D finished: the main properties of the sensors are defined

➢ Polarity

⊙ n-in-p is the selected option, as it offers robust performance

★ i.e. graceful degradation after heavy irradiation

Material

\odot MCz or FZ

★ MCz seems to have better annealing behaviour: allows for long annealing times with no adverse effects

- Could be (eventually) operated at lower $V_{\mbox{\tiny bias}}$ mitigating the requirements on the cooling

> Thickness

⊙ About 240 µm thickness seems to be the optimal value

- ★ Fine-tuning of thickness has a significant impact on longevity
- ★ Sufficient charge, good annealing behaviour, lower I_{dark} and V_{bias}

Outer Tracker input to Level-1 trigger: p_T modules



4.0 **2S module PS module**

\mathbf{p}_{T} modules

2 Strip sensors 2 × 1016 Strips: ~ 5 cm × 90 μ m 2 × 1016 Strips: ~ 5 cm × 90 μ m P ~ 5.4 W ~ 2 × 90 cm² active area For R > 60 cm Spacing 1.8 mm and 4.0 mm

Pixel + Strip sensors 2×960 Strips: ~ 2.5 cm × 100 µm 32×960 Pixels: ~ 1.5 mm × 100 µm $P \sim 7.8$ W ~ 2 × 45 cm² active area For r > 20 cm Spacing 1.6 mm, 2.6 mm and 4.0 mm

Operate sensors at about -20°C with cooling set point at -30°C

2S module





- Read out from the edges, to avoid difficult / expensive TSV technologies
- Flex hybrid circuit collects signals from both sensors
 - Supports wirebonding to sensors and bump-bonding of readout ASICs
 - Complex routing and high-density of lines
 - 8 CBC, 1016 channels per sensor per end
- > The sensors has 90 μ m pitch at the limit of the hybrid technology!





PS module





- Size limited to $\frac{1}{2}$ 6" wafer >
 - Cover the length with 2 chips connect from the sides \odot
 - \odot 25 mm long strips required at low radii anyway
- \succ Hard limit at 100 µm pitch in order to use large-volume (inexpensive) bump-bonding • N.B. 25 m² of Macro-Pixel Sensors
- Segmentation in z is a compromise between z_0 resolution and power dissipation \geq

Deploy down to ~20 cm to achieve reasonable z_0 resolution in L1 tracking \succ

• Also much less expensive and power-hungry than pixel modules!!









- Tilted mechanics more difficult and more expensive, likely heavier
 - Degraded z₀ resolution for L1 tracks
- Large reduction in number of PS modules (≈1200)
 ⇒ mass reduction, large cost saving (≥ 4 MCHF)

Small penalty in performance for L1 tracks Large cost saving and less risks















Additional considerations

- PS modules provide three layers of unambiguous 3D coordinates (plus p_T info)
 - An asset for pattern recognition
- Granularity well matched to intermediate radii
- A much more cost effective solution than extending the IT to larger radii / more layers
- Having developed three different systems pays off!
- p_T modules are an asset for tracking in high pileup: a design solution to keep in mind for future trackers

	2S system	PS system	IT system
Cost (MCHF / m²)	0.60	1.27	5.15
Cost ratios		PS/2S = 2.1	IT/PS = 4.1
Power density (W / cm ²)	0.060	0.173	1.0
Power ratios		PS/2S = 2.9	IT/PS = 5.8





Inner Tracker



Enhanced radiation tolerance \rightarrow thinner silicon sensors \rightarrow less charge available Possibly 3D sensors in the inner regions

Improved two-track separation for high-energy jets

Readout chip with small cell-size, low detection threshold, and huge data rate capability

25 PU	\Rightarrow	200 PU	
3.2 µs	\Rightarrow	12.8 μs L1 latency	×4 ×8
100 kHz	\Rightarrow	750kHz L1 rate	×7.5 ×8
300 fb ⁻¹	\Rightarrow	3000 fb ⁻¹	

Technology: 65 nm CMOS Cell size 25×100 μ m² (×6 smaller than phase-1 detector) Common development with ATLAS in RD53

- × 8 hit rates (3.2 HGz / cm² in the first layer)
- × 32 size of buffers
- × 60 bandwidth from front end
- × 10 radiation tolerance (also for sensors)

Radiation qualification of 65nm CMOS

Thorough studies of radiation degradation vs T & bias conditions Results reproduced (qualitatively) by rad damage effective model

Excellent results from small-size demonstrators

Eagerly awaiting results from large-size demonstrator RD53A!

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Sensors R&D ongoing

Pixel structures only tested to about 2E15

Higher fluences explored with strip sensors or test structures

Hints that optimal thickness should be around 150 μm

The 1E16 range is very challenging!

Developing also 3D sensors for ultimate rad tolerance (target 1st barrel layer and 1st ring in forward)

Expect to collect all the answers in the next two years Possibly a kind of final word about radiation tolerance of silicon sensors??

Another key ingredient: serial powering

Requirements for current distribution are unprecedented

Future pixel detector will consume ~50 kW @ 1V To be compared with present detector 9 kW @ 2.5 V

One order magnitude higher current

In serial distribution current flows through several (~10) FE modules Modules in the power chain have different reference ground!

Very challenging system issues!

N.B. HV distribution is parallel

Never attemped in a large-scale detector!

Common ATLAS/CMS development

Will set a new standard in HEP detector design (... especially if we make it work!)

Performance highlights

Robust track finding performance

0.05 000⁰⁰⁰ 000000 0 -4 -3 -2 -1 0 1 2 3 4 Reconstructed track η Less material x/x 1.6 Phase-2 Tracker In front of IT sensors In front of IT sensors nside IT tracking volume nside IT tracking volume 1.4 etween IT and OT ween IT and OT side OT tracking volum Inside OT tracking volume 1.2 0.8 0.6 0.4 0.2 0 2 2.5 3.5 1.5 3 3.5 4 0.5 1 2 η

0.

14 TeV

← <PU> = 140

Tracks from ti events

If beam-spot *sliced* in successive O(30) ps time exposures, *effective pileup* reduced by a factor 4-5:
~15% merged vertices reduced to 2%
Phase-I track purity of vertices recovered

VBF H→TT in 200 pp collisions

vertices

Barrel Timing Layer Outside Tracker LYSO + SiPM

Large coverage for vertexing in 4D

Endcap Timing Layer On HGCal nose Low Gain Silicon detectors

Track-vertex association – with track timing

- With timing, 'effective vertex density' down to LHC level !
 - 1. Cleaner isolation cones
 - 2. Improved primary and secondary vertex reconstruction
 - 3. Improved jet and p_T^{miss} reconstruction
- Boost performance of several observables
- Bottom line: 20÷30% enhanced statistical power in most physics channels!

- Nominal geometry: 12 x12 mm² (~ 3 mm thick) + 4x4 mm² SiPMs
- Production-like geometry qualified in test beams
- Good radiation hardness of production-ready SiPMs
- ▶ Operate SiPMs at ~ -30 °C (limit self-heating and dark rate)

Silicon detectors with embedded low-gain layer

Produce fast-rising signals for precision timing

With suitable readout chip and clock distribution

Nominal geometry: 4.8 x 9.6 cm² modules with 1x3 mm² pads

- 16 ASICs bump-bonded to sensors
- 3:1 ganging in the TDC at small η (3x3 mm² granularity)
- Single pads shown to have σ_t ≤50 ps up to 10¹⁵ n_{eq}/cm²
- Readout ASIC in development
 - Simulation underway prototype runs 2018 and 2019

The Others

Other LHC detectors and other new technologies

HV CMOS in ALICE

No bump-bonding Less mass Less cost (...maybe)

Lower radiation tolerance and rate capabilities

Ideal solution for a best-quality tracker for ALICE!

HV CMOS in ATLAS?!?

Vertical full depletion

Lateral partial depletion

Collection time < 30ns (V_{bb}=-3V)

Suitable for up to 10¹⁴ n/cm²

- Reduces charge collection time (<1ns)
- Enhances radiation hardness (~10¹⁵ n / cm²)

Foundry Standard Process

The process modification requires a single additional process mask with no changes on the sensor and circuit layout

Modified process CERN/Tower

Epi-layer fully depleted Collection time < 1ns Operational for up to 10^{15} n/cm²

	ALICE ITS	ATLAS Outer Pixel	ATLAS Inner Pixel
NIEL [n _{eq} /cm²]	10 ¹³	1015	10 ¹⁶
TID	<1Mrad	80 Mrad	2x500Mrad
Response Time [ns]	2000	25	25
Hit rate [MHz/cm ²]	10 + SF	100-200	2000

- CMOS is much higher volume than our specialty high-resistivity planar sensors
 - Significantly lower price than our present silicon sensors due to high volume and larger wafers
- CMOS Modules costs ~ factor 4 less than hybrid (no bumpbonding, no extra FE-chip)

← From an ATLAS slide

Same cost as our PS system (not counting the development cost!)

No advantage for performance

The technology is very appealing Especially if it's used where it is useful!

Futuristic silicon

Add a boron layer similar to LGAD

Fast timing HV CMOS ??

Thin Films: thin layers of materials ranging from nm to μm

- Current popular applications
 - solar cells
 - LCD screens
- Thin Films for Particle Detectors:
 - Thin Film Diodes + Thin Film Transistors

Thin film particle detectors ????

Remarks

HV CMOS and LGAD, combine and add functionalities in a piece of silicon, respectively

HV CMOS is interesting to realize low mass detectors operating at low/intermediate rates Possibly in future for large-surface implementation in not too-high rates (if indeed low cost / good yield is achieved)

LGAD is very interesting for high pileup environment, but not for use in the highest density regions

None of the two developments (nor any other I know of) improves on rad tolerance of traditional sensors ... on the contrary!

With the R&D planned in the next two years we may say a final word about radiation tolerance of silicon sensors...!

Silicon photonics

Use silicon as optical medium (transparent in the $1.3 - 1.6 \mu m$ range) Modulators can be realized as reverse-biased PN junctions

- Radiation resistance potentially as good as Si-sensors and CMOS electronics
- > Possibility of co-integration with readout electronics
- Place light source in the back-end

Tomorrow:

From 2016: radiation testing of Mach-Zender modulators

· neutron irradiation

Intriguing results!

Hint: effect from charge trapping in oxide layers, but no effect from bulk damage! Can it be improved further with custom designs?

Silicon photonics: outlook

Large R&D program needed to develop solutions adapted to HEP

- Crucial aspects are packaging and connectivity
- Learn how to optimally use these devices in system design

May open new horizons for future trackers (and particle detectors in general)

- o Large bandwidth from the front-end
 - Trackers more regularly used in L1 trigger?
- Extreme radiation hardness
- Avoid electrical links (on macroscopic scale)
- Reduction of mass and power

Draft: 06/04/2017

- Technical Proposal -

DEVELOPMENT OF WIRELESS TECHNIQUES IN DATA AND POWER TRANSMISSION APPLICATION FOR PARTICLE-PHYSICS DETECTORS

- WADAPT -Wireless Allowing Data And Power Transmission

Scope of FCC Study

International FCC collaboration (CERN as host lab) to study:

- pp-collider (FCC-hh)
- \rightarrow main emphasis, defining infrastructure requirements
- ~16 T ⇒ 100 TeV *pp* in 100 km
- ~100 km tunnel infrastructure in Geneva area, site specific
- e⁺e⁻ collider (FCC-ee) as potential first step
- p-e (FCC-he) option, integration one IP, e from ERL
- **HE-LHC** with *FCC-hh* technology (LHC Ring $8 \rightarrow 16T$, $14 \rightarrow 28TeV$)
- CDR for end 2018

Draft Schedule Considerations

HE-LHC integration aspects

Working hypothesis for HE LHC design:

No major CE modifications on machine tunnel and caverns

- Similar geometry and layout as LHC machine and experiments
- Maximum magnet cryostat external diameter compatible with LHC tunnel ~1200 mm
- Classical 16 T cryostat design based on approach gives ~1500 mm diameter!

Strategy: develop a single 16 T magnet, compatible with both HE LHC and FCC-hh requirements:

- Allow stray-field and/or cryostat as return-yoke
- Optimization of inter-beam distance (compactness)
- → Smaller diam. also relevant for FCC-hh cost optimization

FCC-pp collider parameters

parameter	FCC-hh		HE-LHC	HL-LHC	LHC
collision energy cms [TeV]	100		27	14	14
dipole field [T]	16		16	8.33	8.33
circumference [km]	97.75		26.7	26.7	26.7
beam current [A]	0.5		1.12	1.12	0.58
bunch intensity [10 ¹¹]	1	1 (0.2)	2.2 (0.44)	2.2	1.15
bunch spacing [ns]	25	25 (5)	25 (5)	25	25
synchr. rad. power / ring [kW]	2400		101	7.3	3.6
SR power / length [W/m/ap.]	28.4		4.6	0.33	0.17
long. emit. damping time [h]	0.54		1.8	12.9	12.9
beta* [m]	1.1	0.3	0.25	0.20	0.55
normalized emittance [µm]	2.2 (0.4)		2.5 (0.5)	2.5	3.75
peak luminosity [10 ³⁴ cm ⁻² s ⁻¹]	5	30	25	5	1
events/bunch crossing	170	1000 (200)	~800 (160)	135	27
stored energy/beam [GJ]	8.4		1.3	0.7	0.36

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1 MeV neutron equivalent fluence for 30ab⁻¹

Technologies for Tracking at \rightarrow 1000 pileup

- > Outer layers a few 10¹⁵: LGAD and HVCMOS promising
 - LGAD: timing will be precious
 - HVCMOS: low cost for large surfaces easy mass production
 - \circ Both combined?
- > Intermediated layers a few 10¹⁶: standard Si sensors still the option
 - With readout chips in advanced technologies
- Innermost layers a few 10¹⁶ per year: is this silicon???
 - More than one replacement per year is going to be very unpractical...
 - Stay tuned for the results of the next two years
 - Maybe need to consider more creative solutions here!

Readout links: silicon photonics

- p_T modules (useful at all stages!)
- Tracking information at Level-1
 - ✓ (e.g. everything from outer layers, stubs from intermediate layers)
- Serial powering

From a meeting of the CERN EP department on future R&D:

We should formulate the needs for an FCC detector, but place the detector R&D inside the existing CERN programs e.g.

- Change of ATLAS CMS pixels during the HL-LHC period
- Possible further upgrades of ATLAS, CMS during HL-LHC period
- LHCb Phasell upgrade, ALICE Phasell upgrade
- Fixed target experiments (existing, Ship ...)

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Pixel phase-3?

Technologies for pixel phase-3

Silicon photonics

- Get rid of IpGBT boards and DC/DC converters
- All functionalities integrated in (serially powered) modules
- Reduce complexity and remove mass from service cylinders
- Rad hard enough for layer 1? Timescale?

More advanced ASIC technology

• Reduce power (by a large factor)

Technologies for pixel phase-3

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More advanced ASIC technology

• Reduce power (by a large factor)

> Maybe LGAD for more timing layers?

- Extend acceptance of timing measurements in rapidity and p_T
- Rad hard enough?
- High granularity? Tracking performance? Power?

Concluding:

... all that might be very fancy, but now we have to build the phase-2 upgrades!