Prospettive sulle alimentazioni per il tracciatore di CMS a HL-LHC

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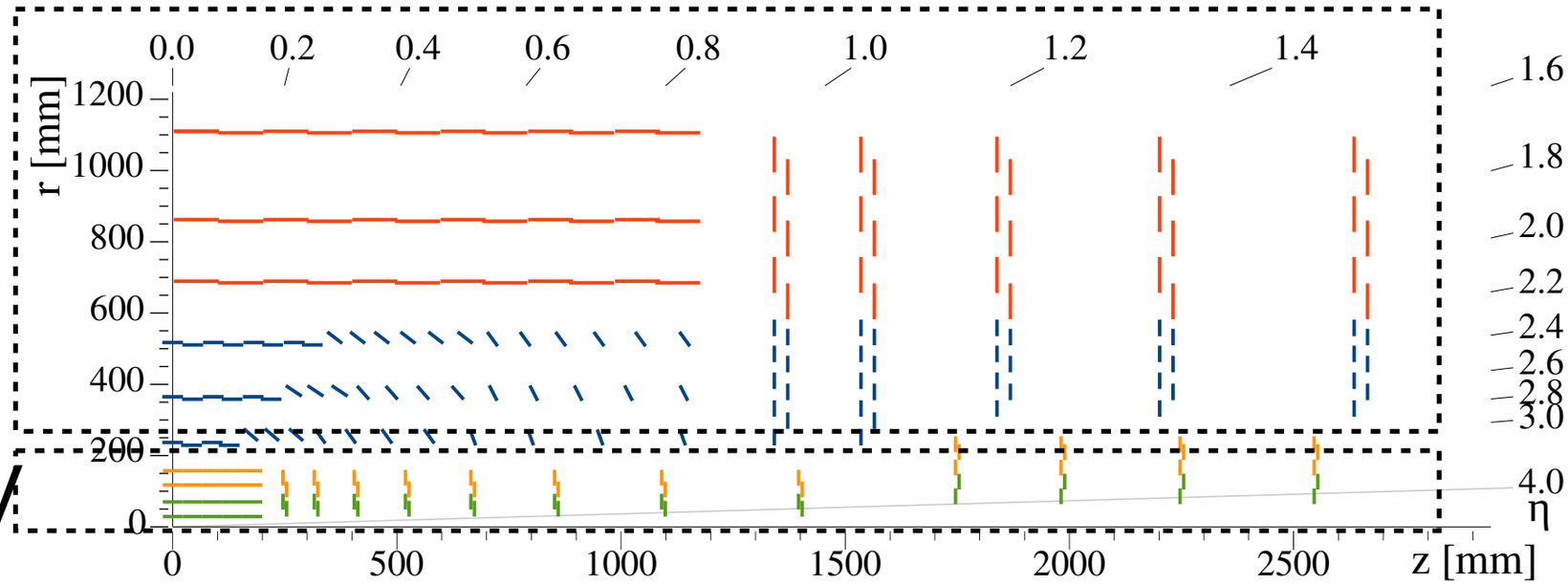
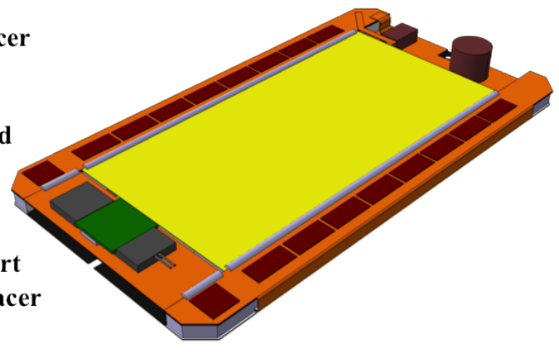
Il tracciatore per HL-LHC

~100 kW @ ~11V

~40 kW @ 1.2V + 0.8 V



1. PS-s silicon sensor
2. PS-p silicon sensor
3. MPAs
4. Al-CF sensor spacer
5. CFRP base plate
6. FE Hybrid
7. Opto-Link Hybrid
8. Power Hybrid
9. SSA
10. CIC
11. Hybrid CF support
12. Al-CF Hybrid spacer



2.5 V, 1.00 V, 1.25 V

Outer Tracker:

~ 8200 2S modules

~ 5300 PS modules

~ 6 W per PS module

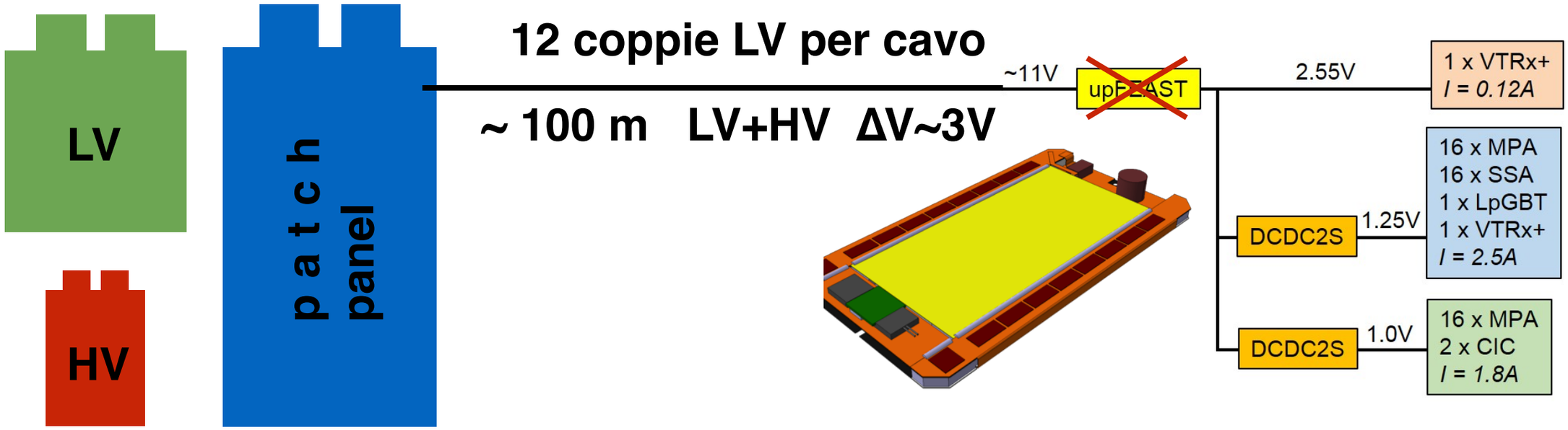
~ 3 W per 2S module

Pixel:

~ 4000 modules

~ 13 000 R/O chips (RD53)

Alimentazione moduli OT



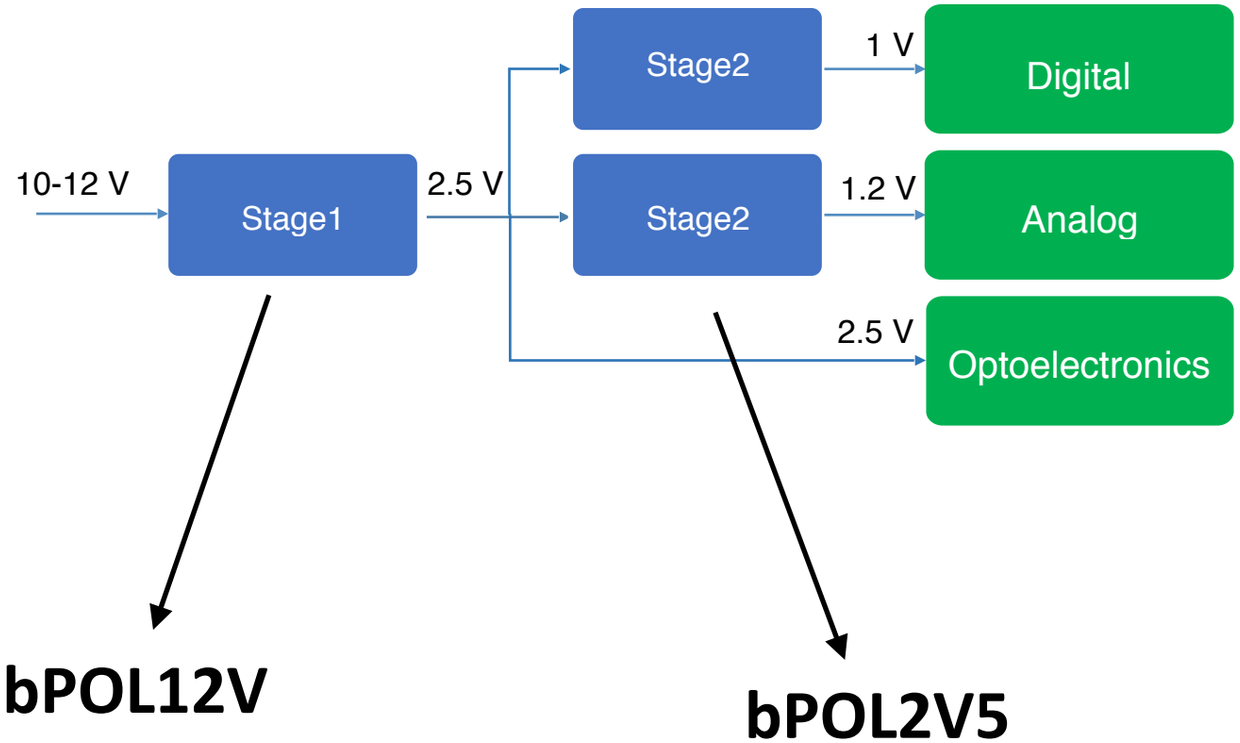
- No power → no communication to module
- ~ 13 000 fili LV da back-end a detector da gestire
- Alimentazione di DC/DC (carico non Ohmico)
- ! Gestione transienti (power-ON, power-OFF etc.) → specifiche del DC/DC converter
- Efficienza dopo irraggiamento
- Interplay LV ↔ HV

? Ubicazione ? (Area ostile o USC ?)

? Sezione dei cavi ?

? Current compensation ?

F.Faccio, MAR 2017



bPOL12V

(“~~upFEAST~~”)

Input voltage	6.0 V ÷ 12 V
Output voltage	0.6 V ÷ 5 V
Output current	≤ 4 A
Switching frequency	1.5 ÷ 3 MHz
Inductor value	200 ÷ 500 nH

bPOL2V5

(“~~DCDC2S~~”)

Input voltage	2.0 V ÷ 2.5 V
Output voltage	0.6 V ÷ 1.5 V
Output current	≤ 3 A
Switching frequency	≥ 4 MHz
Inductor value	< 120 nH

<u>Radiation environment without safety factors</u>

TID: 100 Mrad

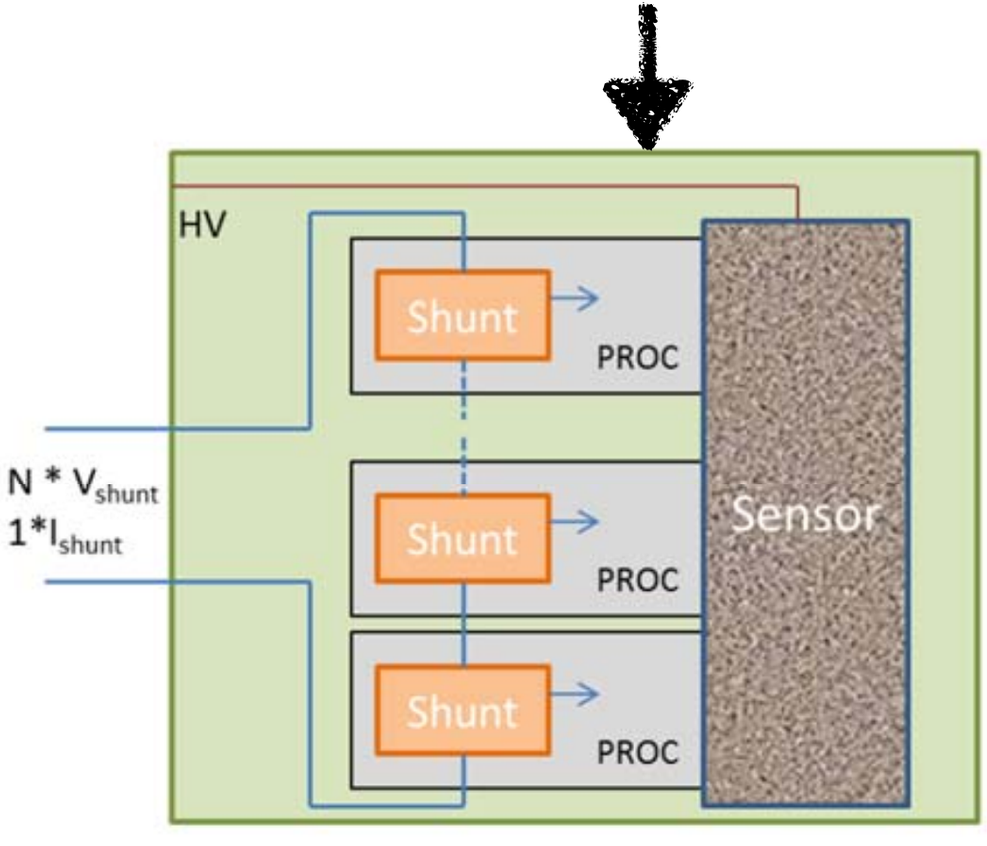
DD: 1.5e15 n/cm^2

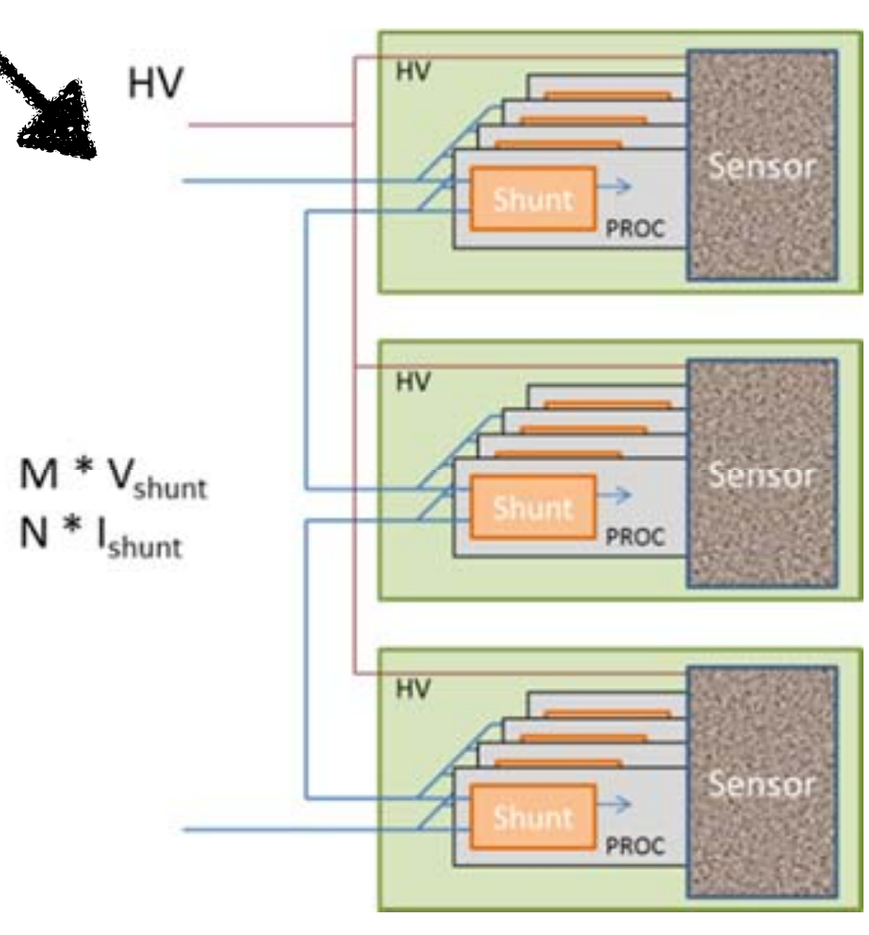
SEEs : no destructive event to LET < 40MeVcm^{2}mg^{-1}

No reset, negligible SETs in hadron environments

Inner Tracker: Serial Powering

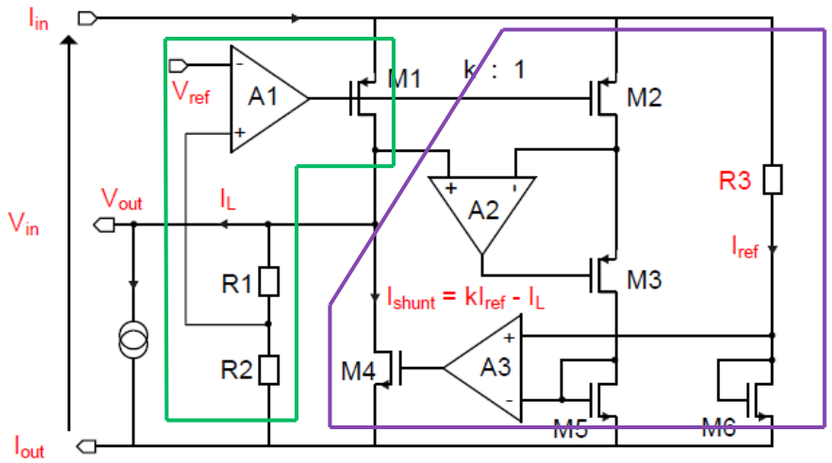
- Serial Powering is the baseline choice for CMS to power the px phase2 detector
- space, rad. levels → on-module DC-DC conversion currently excluded
- Two options: in-module, across-module serial powering





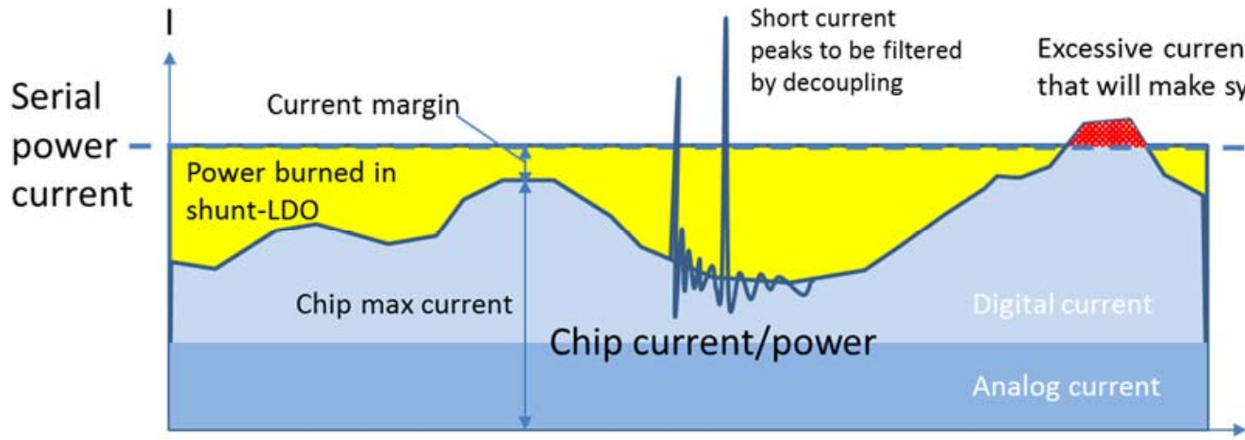
collaborazione tra ATLAS e CMS

- ATLAS ha già fatto esperienza col serial power nel corso del progetto IBL
- FEI3, FEI4 sono dotati di circuito “shunt-LDO” e possono essere configurati per S.P.
- in corso studi su SP utilizzando FEI4
  - ➡ sistemi USBPIX3
  - prossimi tests su 65nm ShuntLDO testchip irraggiati
  - r/o chip fase2 → RD53

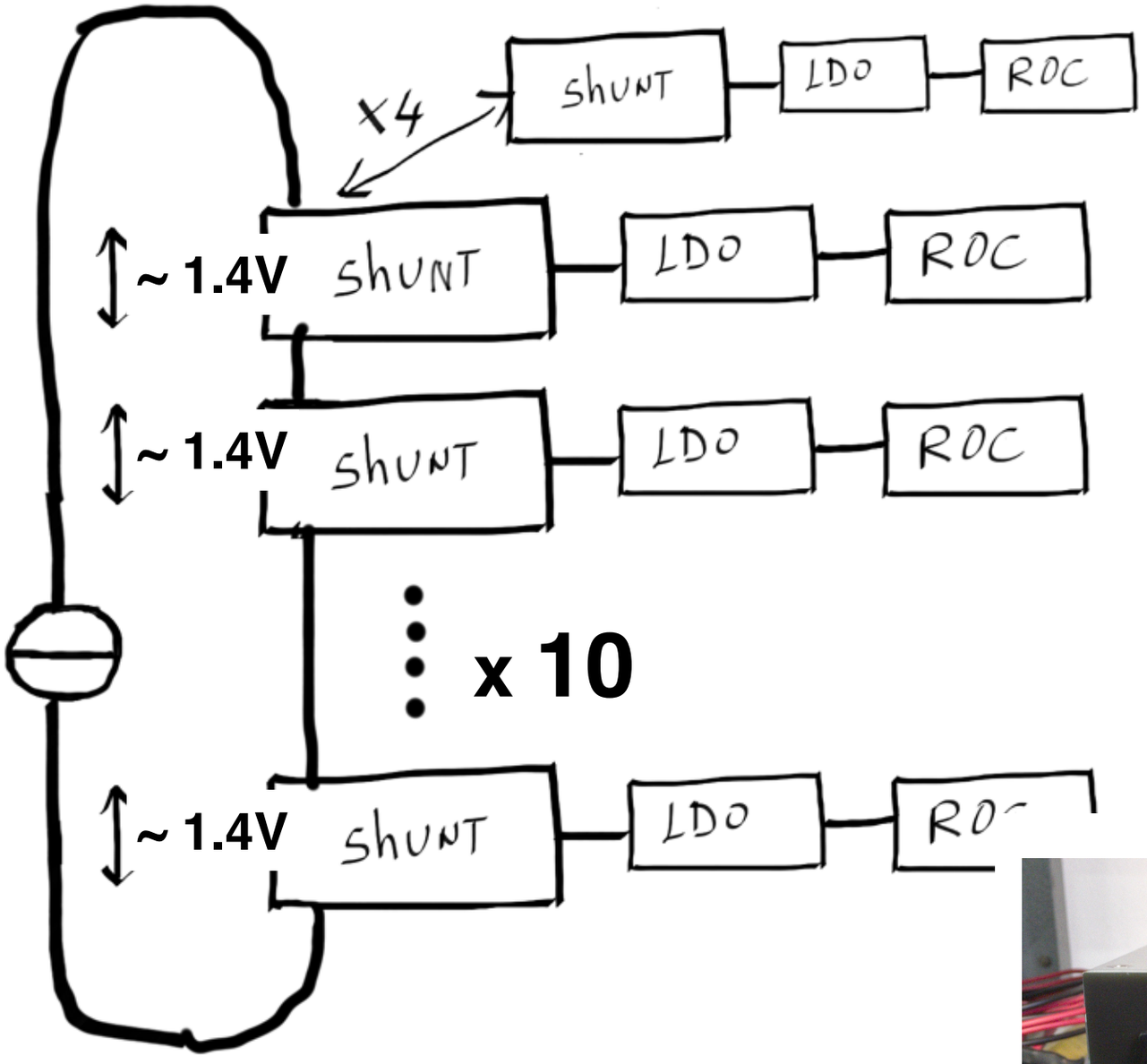


Distribuzione di HV in parallelo

Studio di transienti, power-ON/OFF e variazione dei consumi



Possibile proiezione sul back-end



I ~ 10A

V ~ 10-20 V

~ 500 power loops

- AC/DC + 2-stage DC/DC
- Current and voltage regulated
  - ➡ I and V comparators controlling the final PWM circuitry)
- Imax 2.3 A
- Vmax 10.5 V