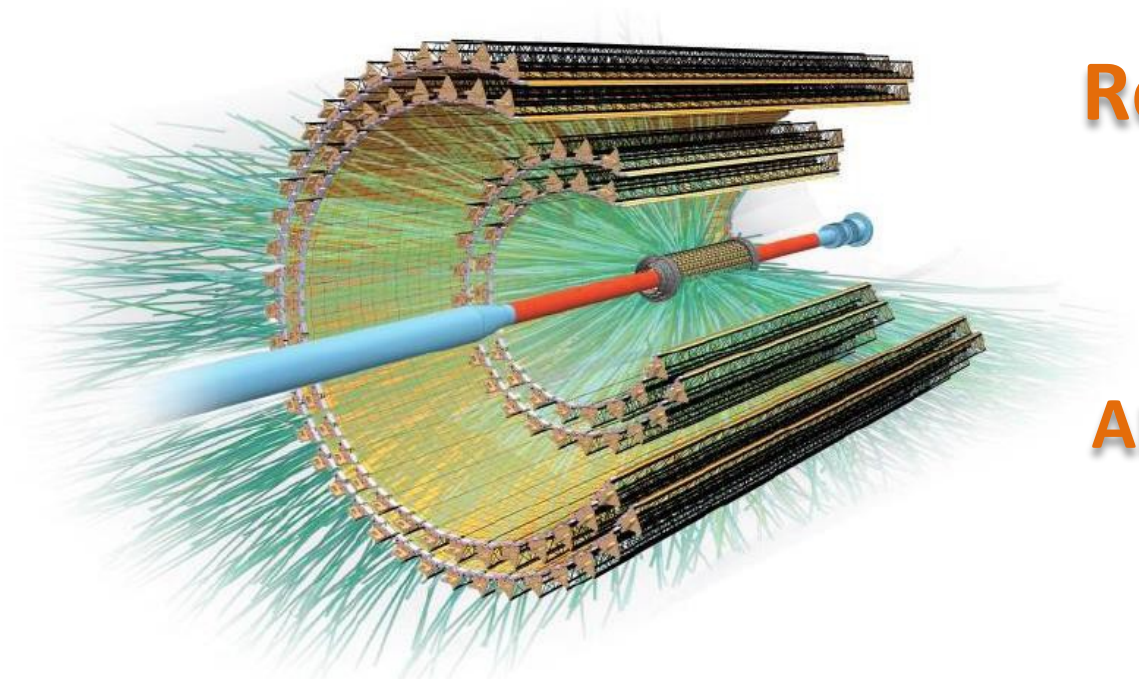


Recent developments in MAPS detectors.

The upgrade of the ALICE Inner Tracking System

Paolo Camerini
Università degli Studi di Trieste & INFN

on behalf of the ALICE collaboration

Outline

- Introduction to Monolithic Active Pixel Sensors
- Motivations, requirements and design goals for the upgrade of the ALICE tracker (ITS-Upgrade)
- Development and characteristics of the ITS-Upgrade and of the ALPIDE chip
- Characterization for the chips and modules prototypes.
- Final considerations

TRACKING IN HIGH ENERGY PHYSICS

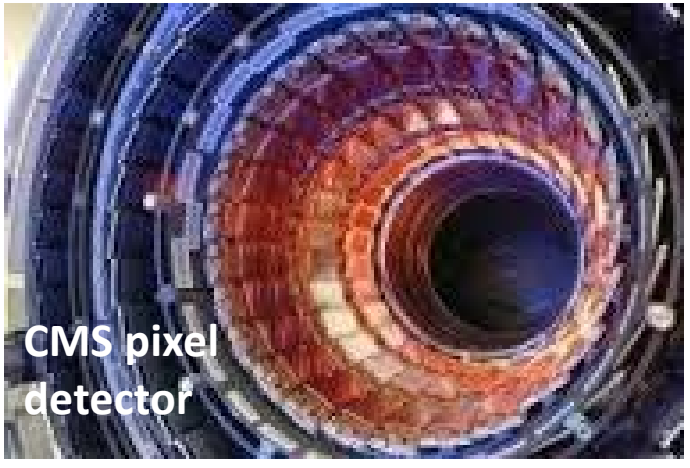
Trackers in High Energy Physics experiments are required to

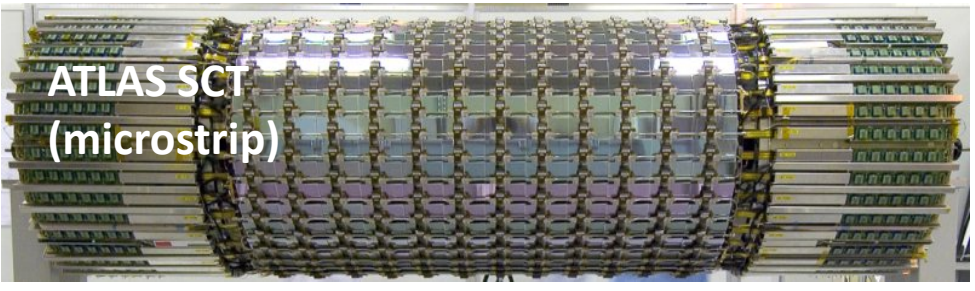
- provide high momentum resolution (often to low pT and in high track density)
- provide high resolution measurements of impact parameter and secondary vertices
- operate in very harsh environment and with high efficiency
- handle high rates of data

This imposes very tight requirements →

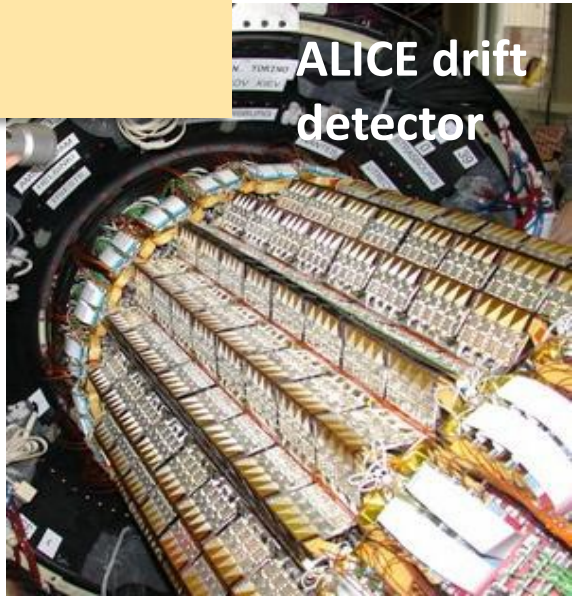
HEP trackers requirements

- **minimal material budget**
- **low power**
- **high granularity**
- **high rates handling capability**
- **low noise**
- **~100 efficiency**
- **radiation hard**





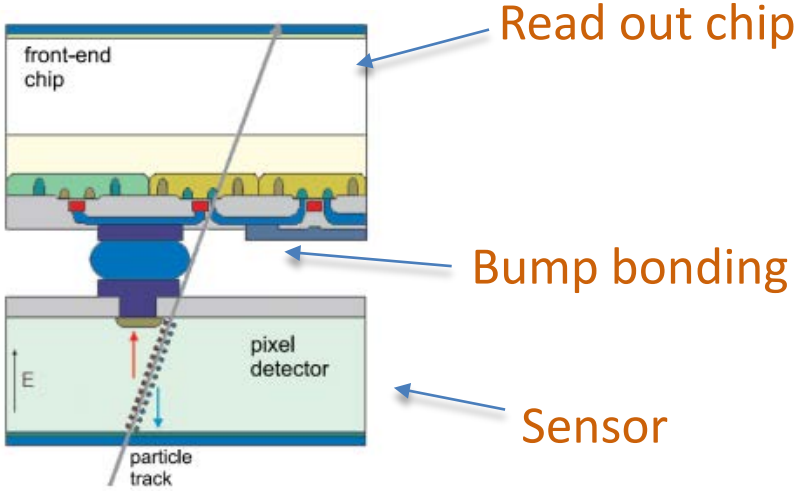
Silicon detectors standard choice for HEP trackers



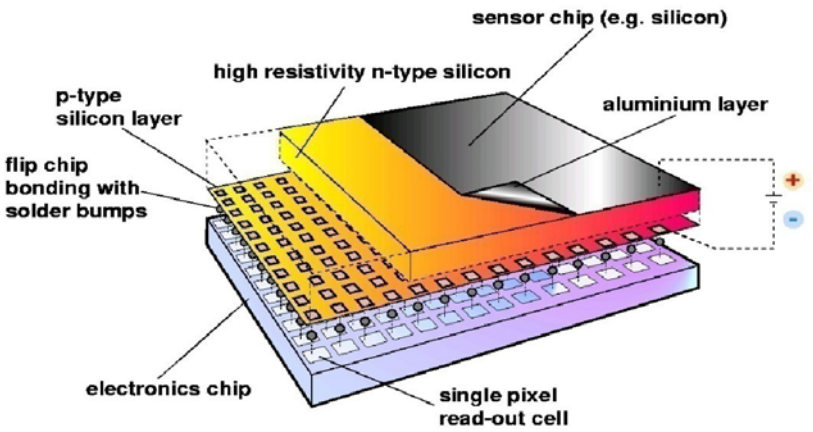
TRACKING IN HIGH ENERGY PHYSICS

Pixel detectors

- usually **inner layers** of trackers
- **Hybrid pixel** detectors instrument all major LHC detectors



Hemperek (U. Bonn)



Hibrid pixel detectors

Separate sensor and ASIC

➢ each pixel connected to a readout channel in the ASIC → flip chip + bump bonding and wire bonding

Pros

- Fast
- radiation hard (full depletion, high voltage)
- high S/N
- fully depleted sensor
- complex read out electronics possible (zero suppression)
- **optimize sensor and read-out chip independently**

Cons

- complex assembly
- 'thick'
- granularity and power limitations
- costly

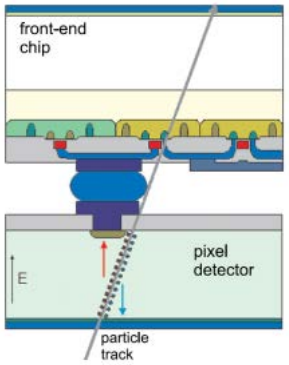
MONOLITHIC ACTIVE PIXEL SENSORS (MAPS)

- Goal: overcome hyrid pixels limitations
- Method: readout and sensor in a single chip

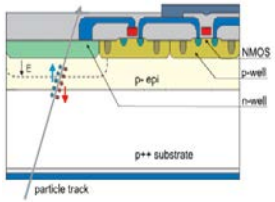
Monolithic Active Pixel Sensors (MAPS)

- Sensor and readout **integrated** on same substrate
- CMOS image sensors industrially developed for photographic applications.
- Sistematically developed as particle detectors since ~2000

Hybrid



Monolithic

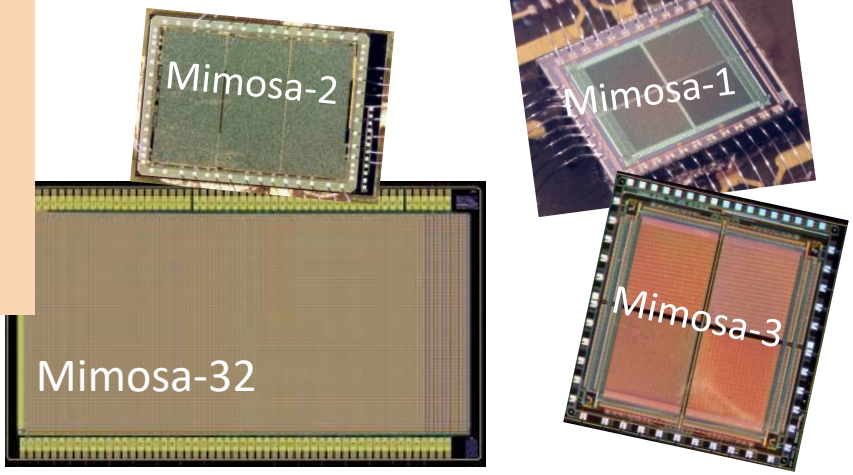


Hemperek (U. Bonn)

Advantages of CMOS Monolithic Active Pixel Sensors

- ❑ Thin sensors (50 um)
- ❑ High Granularity (<30x30μm², ALICE)
- ❑ Ease of assembly
- ❑ Low power
- ❑ Low noise
- ❑ Commercial process, cheap

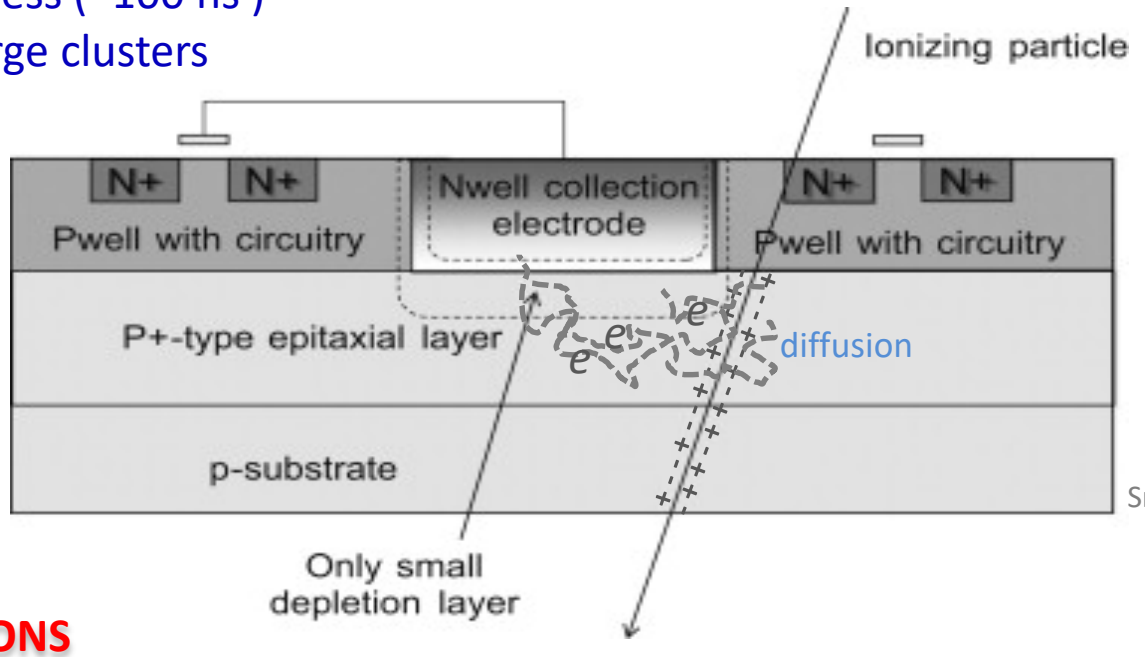
MIMOSA family developed by IPHC



MONOLITHIC ACTIVE PIXEL SENSORS (MAPS)

Standard CMOS monolithic active pixel sensors: principles of operation

- **low resistivity** epi layer typically ~**15um** thick (only nMOS transistors)
- **depleted region** @ sensor diode very **limited**; C~10fF [Deputch, NIMA 465 (2001) 92–100]
- mips realease **~60 e-/um** [Bischel, Rev. Mod. Phys. 60 (1988) 663]
- charge collection @ electrode after random walk (thermal **diffusion**)
- **slow** process (~100 ns)
- large charge clusters



Snoeys, NIMA 765 (2014)

LIMITATIONS

- **low radiation tolerance (slow thermal diffusion in epi)**
- **small S/N**
- **slow readout (no complex circuitry)**

Not suited to HEP environments…

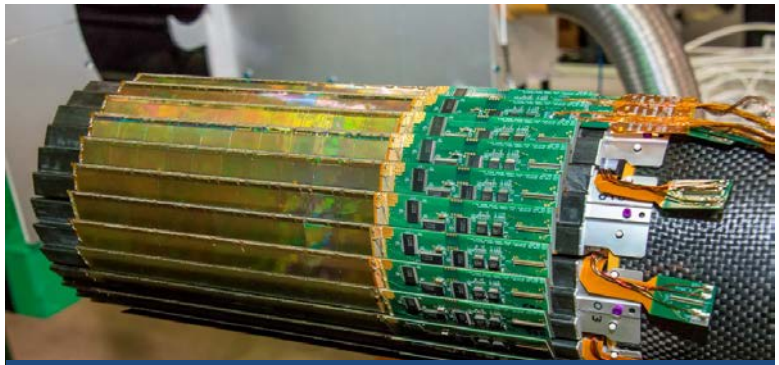
FIRST TRACKERS BASED ON MAPS

Availability of new processes and novel solutions
→ Full MAPS vertex detectors developed:

STAR @ RHIC (ULTIMATE* chip), ALICE@LHC (ALPIDE chip)

* based on MIMOSA-26/22AHR

Upgrade of the STAR HFT
first CMOS MAPS vertex detector at a collider



STAR HFT: first CMOS MAPS tracker

Parameter	ULTIMATE chip	ITS-UPGRADE Requirements
Chip size	20.7 μm X 20.7 μm	15 mm x 30 mm
Chip thickness	**50 μm**	50 μm
Spatial resolution	**~4 μm**	~5 μm
Detection efficiency	>99%	> 99 %
Fake hit rate	**10^{-4} pixel^{-1} event^{-1}**	**10^{-6} pixel^{-1} event^{-1}**
Integration time	**190 μs**	**< 30 μs**
Power density	**150 mW cm^{-2}**	**< 100 mW cm^{-2}**
TID radiation hardness	**150 krad**	**2700 krad**
NIEL radiation hardness	**3x10^{12}** 1MeV n_{eq}/cm^2	**1.7×10^{13}** MeV n_{eq}/cm^2

ALICE TRACKER UPGRADE MOTIVATIONS

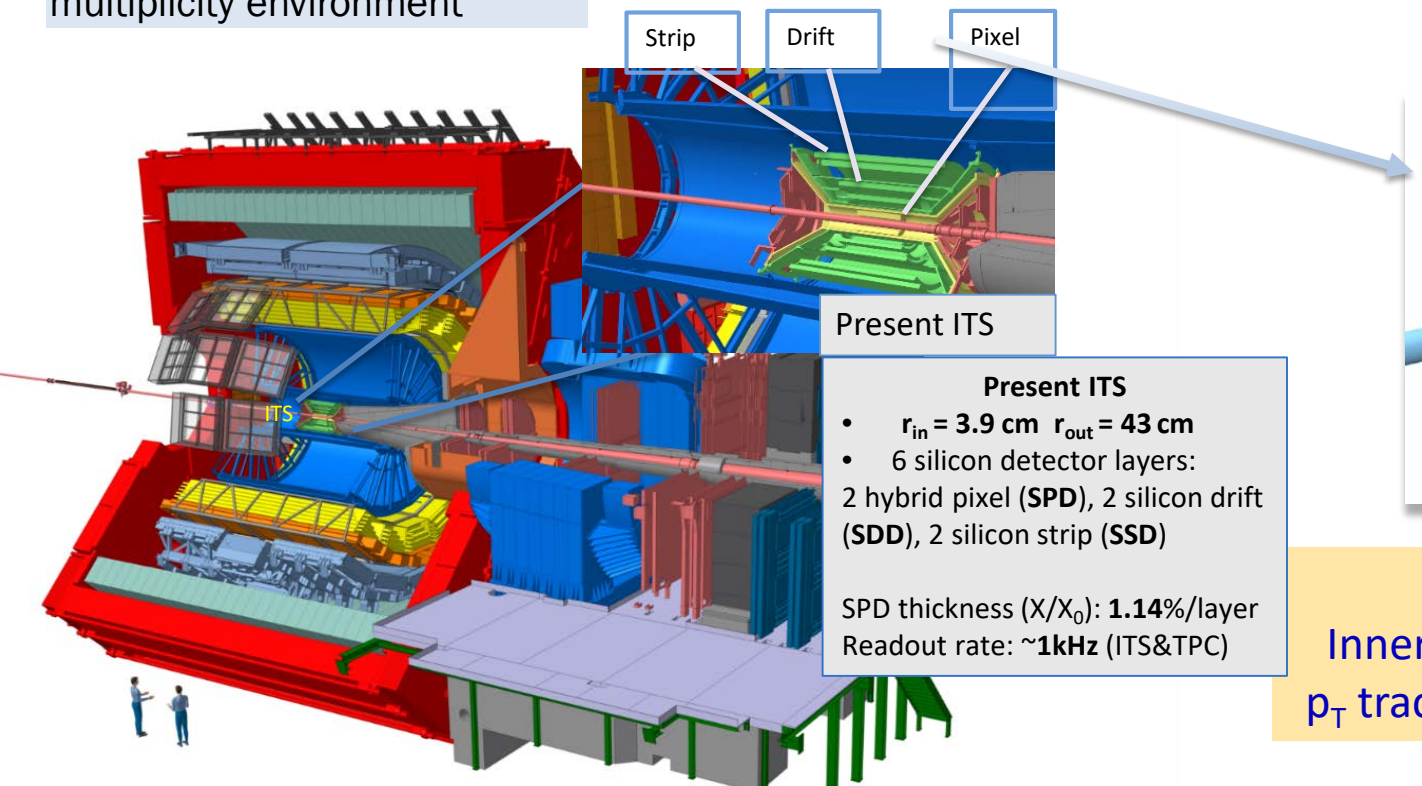
Major upgrade of ALICE forseen during Long Shutdown 2 (2019/20)
Expected Run3&4 Pb-Pb luminosity 6×10^{27} cm^{-2}s^{-1} (10nb^{-1} integrated, factor 100 gain in statistics wrt Run1-2)

Physics Goal: Study of Quark Gluon Plasma properties via high-precision measurements of rare probes

- identification of secondary vertex of short lived particles **@ low p_T**
- large minimum bias data sample needed (no hardware trigger possible)

ALICE detector:
optimized for high resolution tracking and p.i.d. in very high multiplicity environment

To cope with the increased luminosity and improve the tracking performances, several upgrades planned: new Inner Tracking System, new Muon Forward Tracker, TPC, Readout electronics, Trigger, Online/Offline



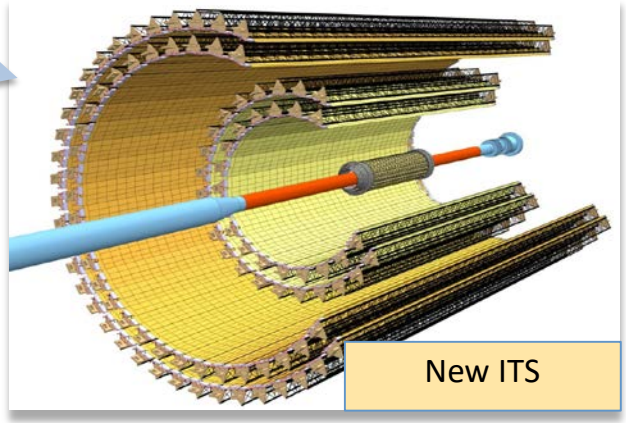
Present ITS

Present ITS

- r_{in} = **3.9 cm** r_{out} = **43 cm**
- 6 silicon detector layers:

2 hybrid pixel (**SPD**), 2 silicon drift (**SDD**), 2 silicon strip (**SSD**)

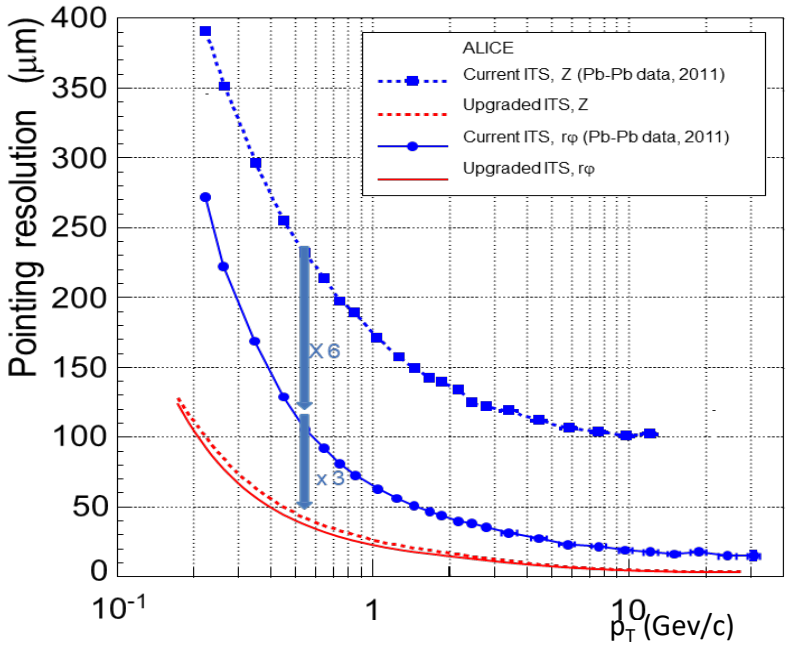
SPD thickness (X/X_0): **1.14**%/layer
Readout rate: **~1kHz** (ITS&TPC)



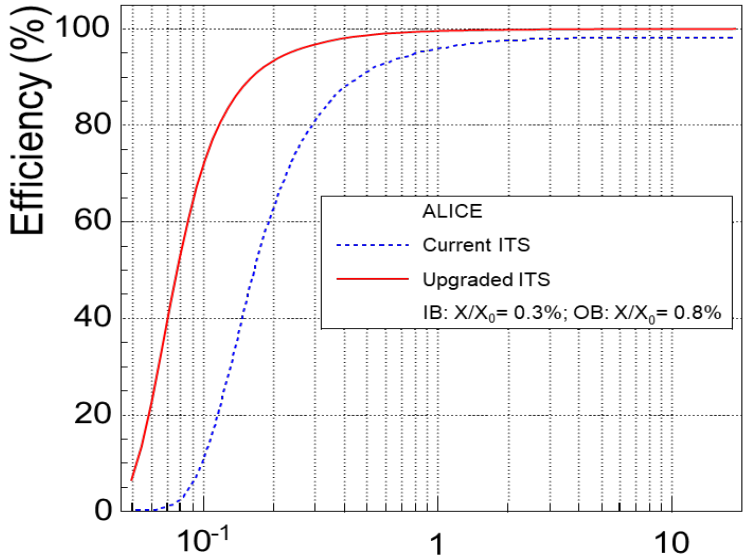
New ITS

Major Upgrade of the Inner Tracking System to improve low p_T tracking and data rate performances

ITS UPGRADE KEY REQUIREMENTS



~40 μm resolution at 500 MeV/c



>60% efficiency at 100 MeV/c

Improve impact parameter resolution

- Get closer to IP: 1st layer 39 mm → 23 mm (new beam pipe)
- Reduce material budget: 1.14% X_0 → 0.3% X_0 (Inner Barrel stave)
  Constraints on chip thickness, power density, support structures
- Reduce pixel size: 50 μm x 425 μm → O(30 μm x 30 μm)

Improve low pT resolution and tracking efficiency

- Pixel, drift, strip detectors → pixel detector
- 6 layers → 7 pixel layers

Improve readout to exploit increased luminosity

- Interactions readout rate (2x LHC expected interaction rate):
  Pb-Pb ~100kHz, minimum bias

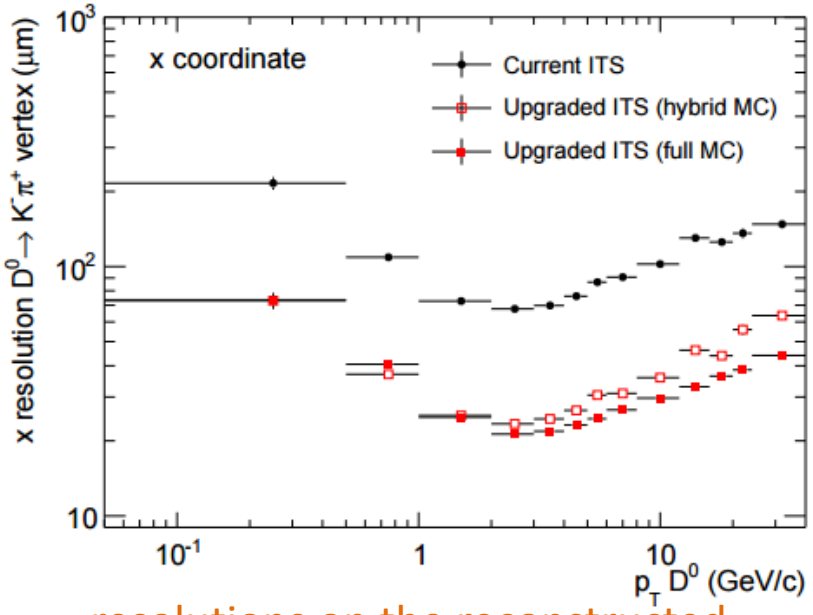
Capability of fast insertion and removal during end of year shutdown

- possibility to replace non-functioning detector modules

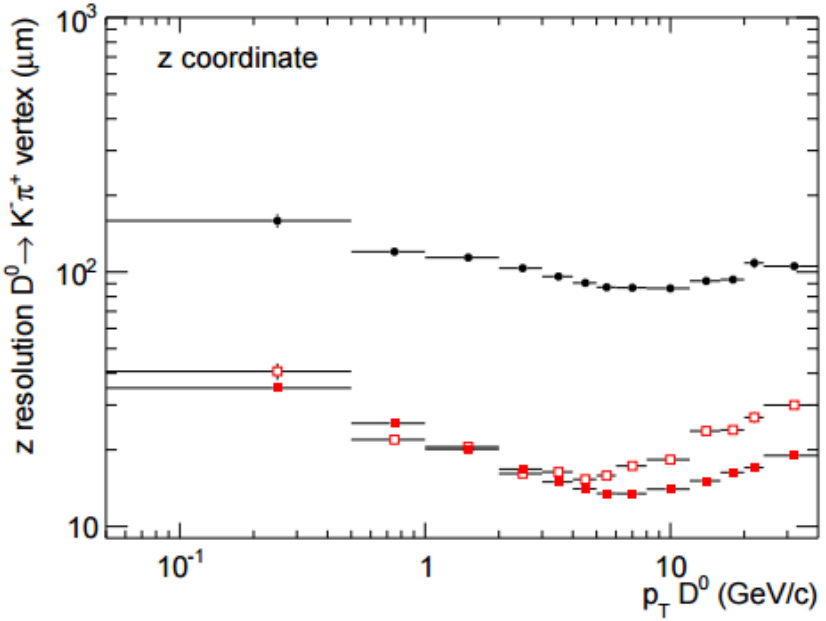
Expected radiation load (10 yrs + safety factor, innermost layer):

- TID: ~ 2.7 Mrad; NIEL: ~1.7×10^{13} 1MeV n_{eq} / cm^2

ITS UPGRADE KEY REQUIREMENTS



resolutions on the reconstructed position of the $D^0 \rightarrow K^-\pi^+$ vertex



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ALPIDE CHIP DEVELOPMENT

Pixel sensor R&D

2012	Explorer	20 µm x 20 µm and 30 x 30 µm pixels (**analogue** readout), 1.8 x 1.8 mm², study of pixel **geometry**, starting **material**, **radiation**
2013	pALPIDEss-0	Matrix with 64 columns x 512 rows, 22 µm x 22 µm pixels, 11 x 1.8 mm², in-pixel **discrimination** and **buffering**, **zero suppression**
2014	**pALPIDE-1**	First **full scale** prototype. 28 µm x 28 µm pixels, 15 x 30 mm², four sectors with **variants**, 1 register/pixel, no final interface
Apr 2015	**pALPIDE-2**	Full scale prototype, four sectors with **variants**, **optimisation** of **circuits**, integration in modules, no high speed serial output
Oct 2015	**pALPIDE-3**	Full scale prototype, eight sectors with variants, all communincation features, no ADC, no temperature sensor)
Aug 2016	**ALPIDE**	**Final chip**

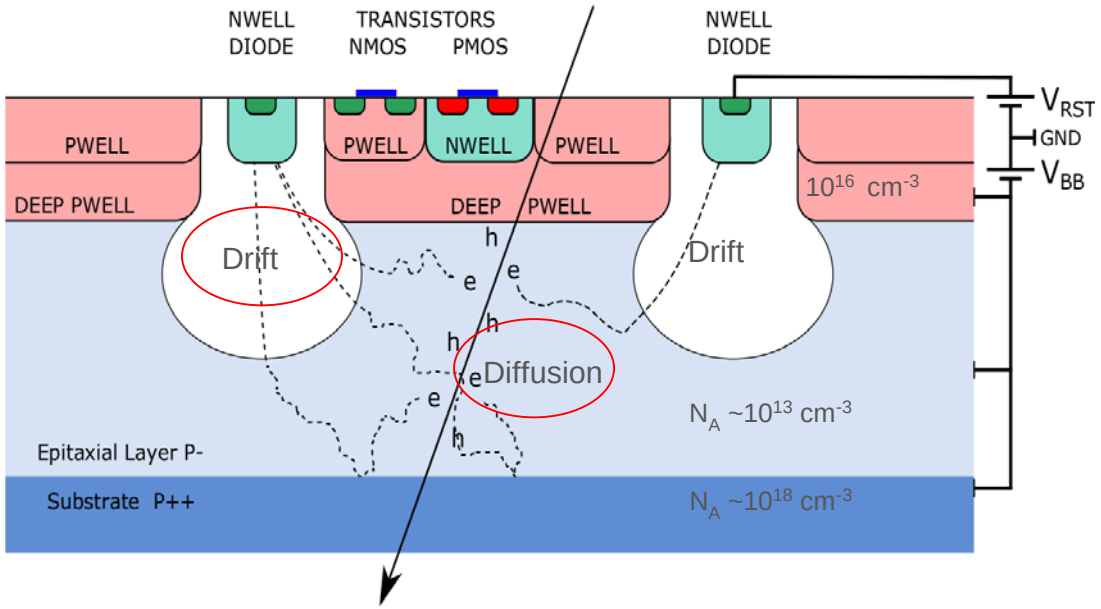
Long R&D with several engineering productions to implement and verify design solutions [Snoeys, NIMA765(2014)167–171]

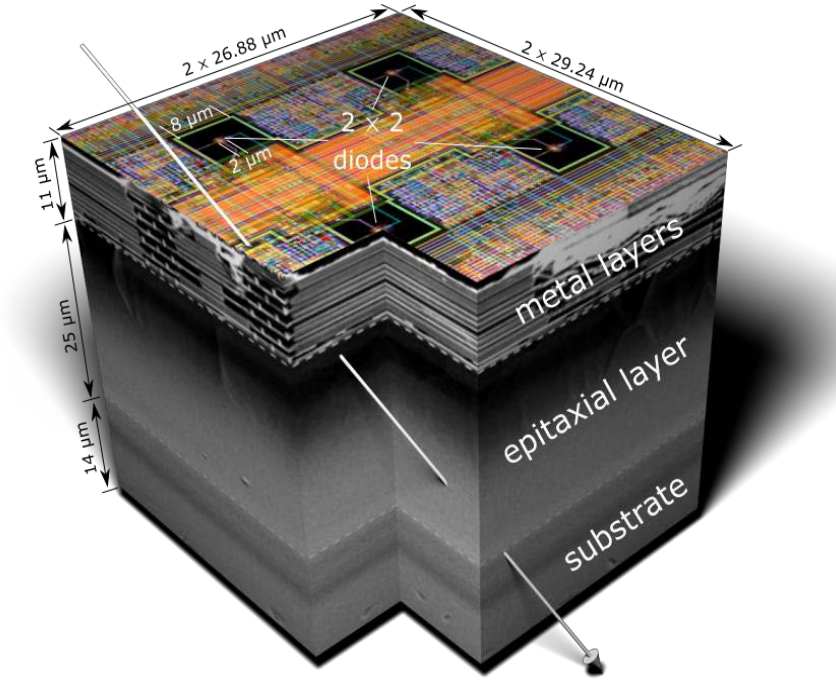
Main design goals

- maximize collected charge over input capacitance ratio (Q/C)
- minimize power consumption
- Improve readout rate
- Improve radiation tolerance

ALPIDE: THE MONOLITHIC ACTIVE PIXEL SENSOR

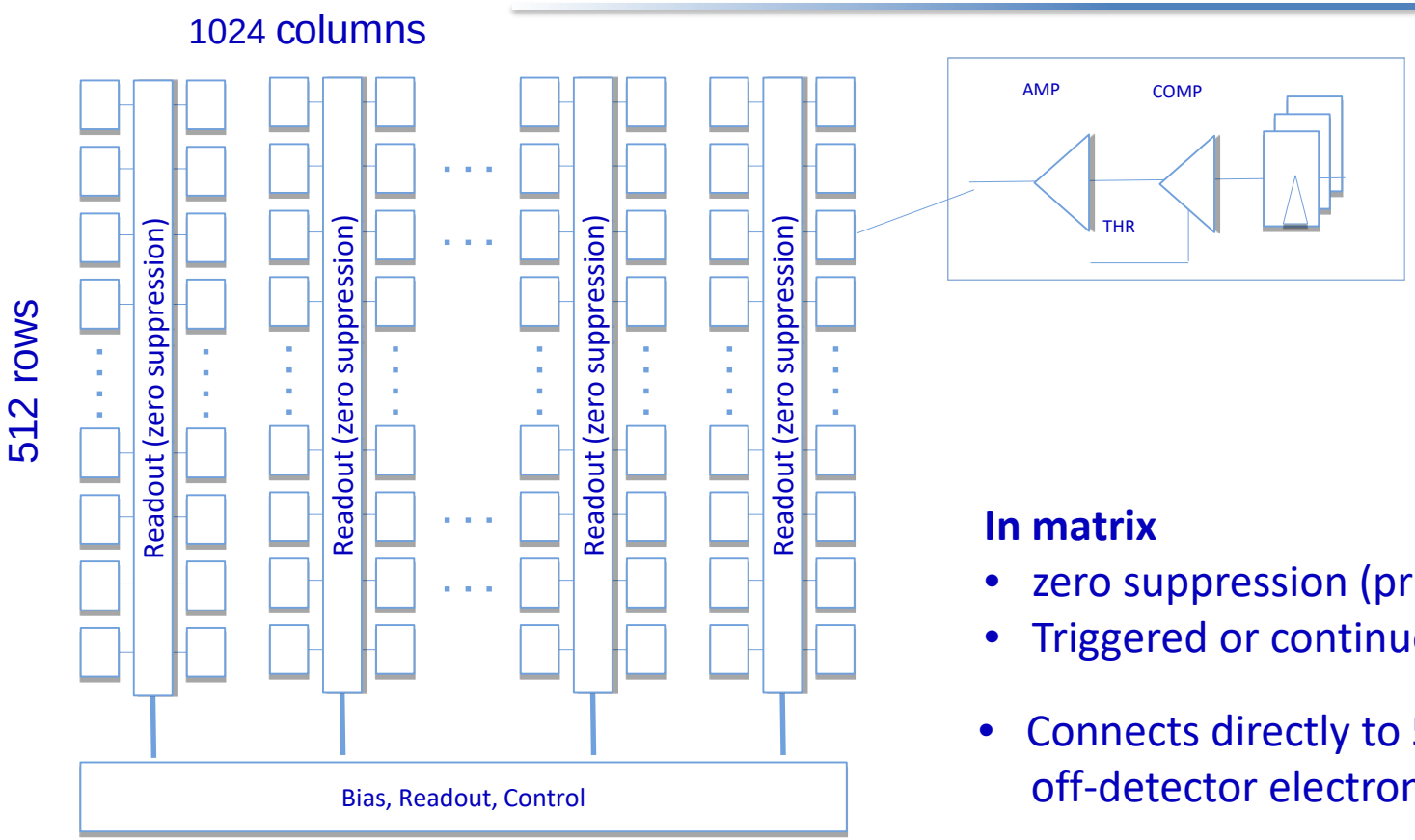
Pixel Sensor produced using TowerJazz 180 nm CMOS Imaging Process





- Deep p-well shielding n-well allows in-pixel PMOS
  - complex in-pixel circuitry without charge loss
  - Key to enable low-power read-out.
- High Resistivity (>1 kΩ·cm) **p-type** epitaxial layer (**25 µm**) on p-type substrate;
- Small n-well diode (2 mm diameter) => low capacitance(~2fF), higher gain and speed (low power)
- Possibility of (moderate) reverse biasing to increase depleted region
  - → Smaller clusters -> more charge collected by seed pixel
  - → Lower input capacitance (→ better S/N ratio)
  - → Short collection time
  - → Better (non ionizing) radiation tolerance
- Gate oxide 3 nm thick (better TID tolerance)

ALPIDE: THE MONOLITHIC ACTIVE PIXEL SENSOR



Main features

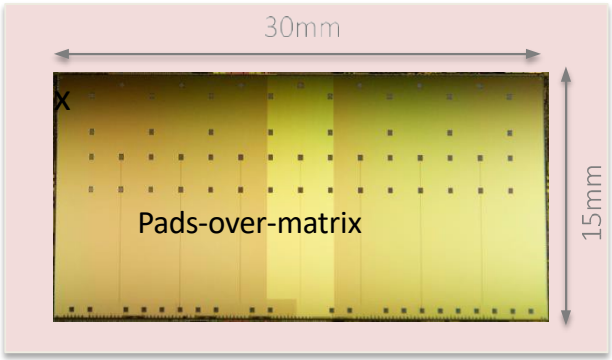
In pixel

- Amplification
- Discrimination
- Multi event buffer

In matrix

- zero suppression (priority encoding)
- Triggered or continuous readout (global shutter)

- Connects directly to 5-m away off-detector electronics via high speed link

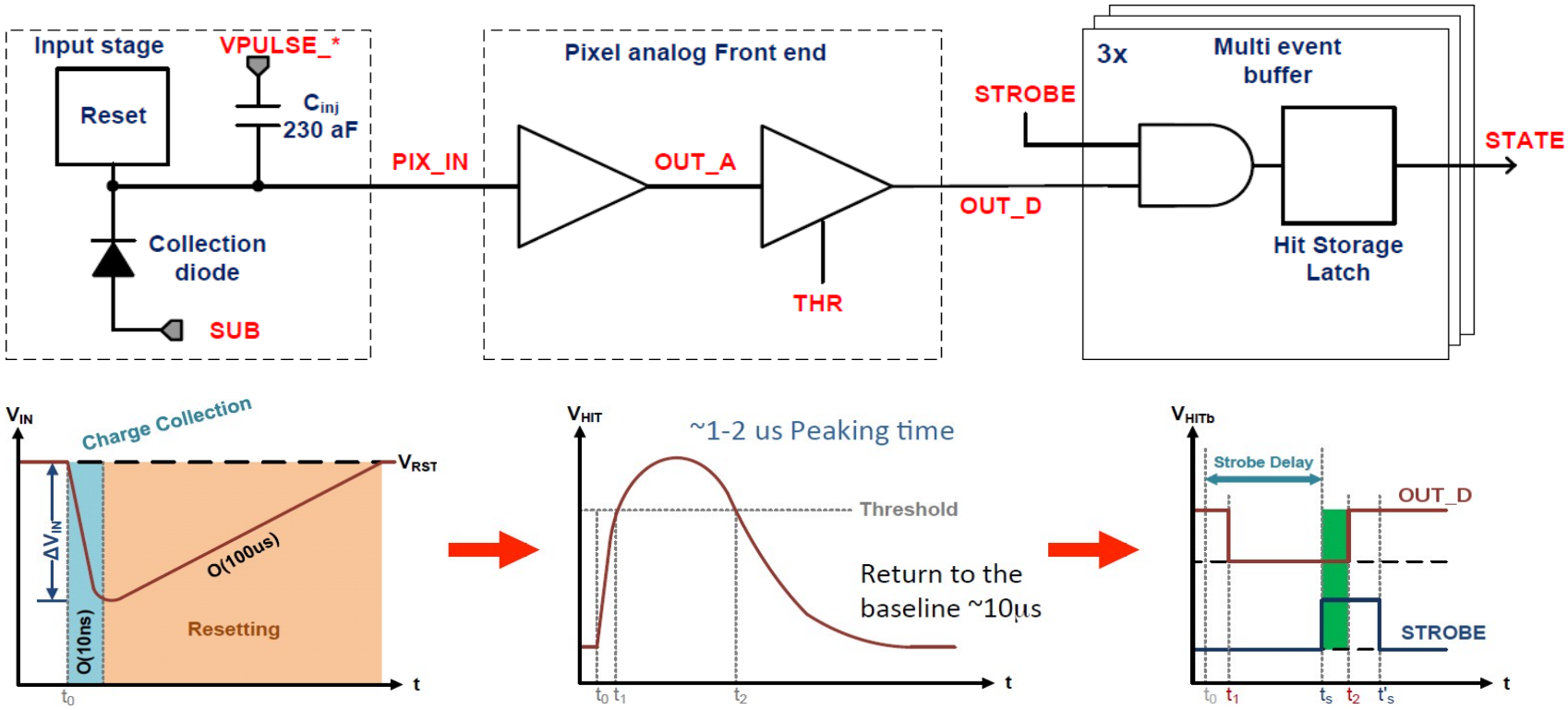


Chip size:
30 mm x 15 mm

Pixel size:
27 μm x 29 μm

No free running clock over matrix.
No activity if there are no hits.
Very low power front end (<40 mW/cm²)

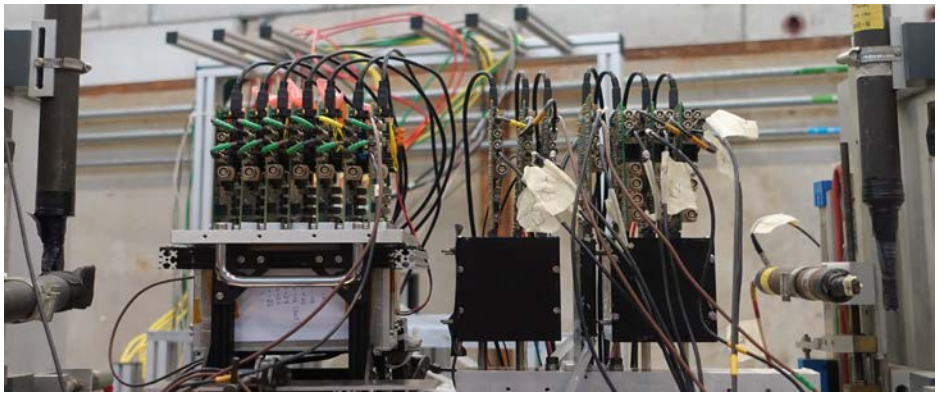
ALPIDE: THE MONOLITHIC ACTIVE PIXEL SENSOR



- Charge created in epitaxial layer is collected
- Signal is shaped and compared to threshold
- Signal is strobed into an in-pixel memory (**Global shutter** latches the discriminated hits in next available register)
- Hit pixels are read out asynchronously (priority encoding)
- Test pulse charge injection circuitry
- Global threshold for discrimination: binary output

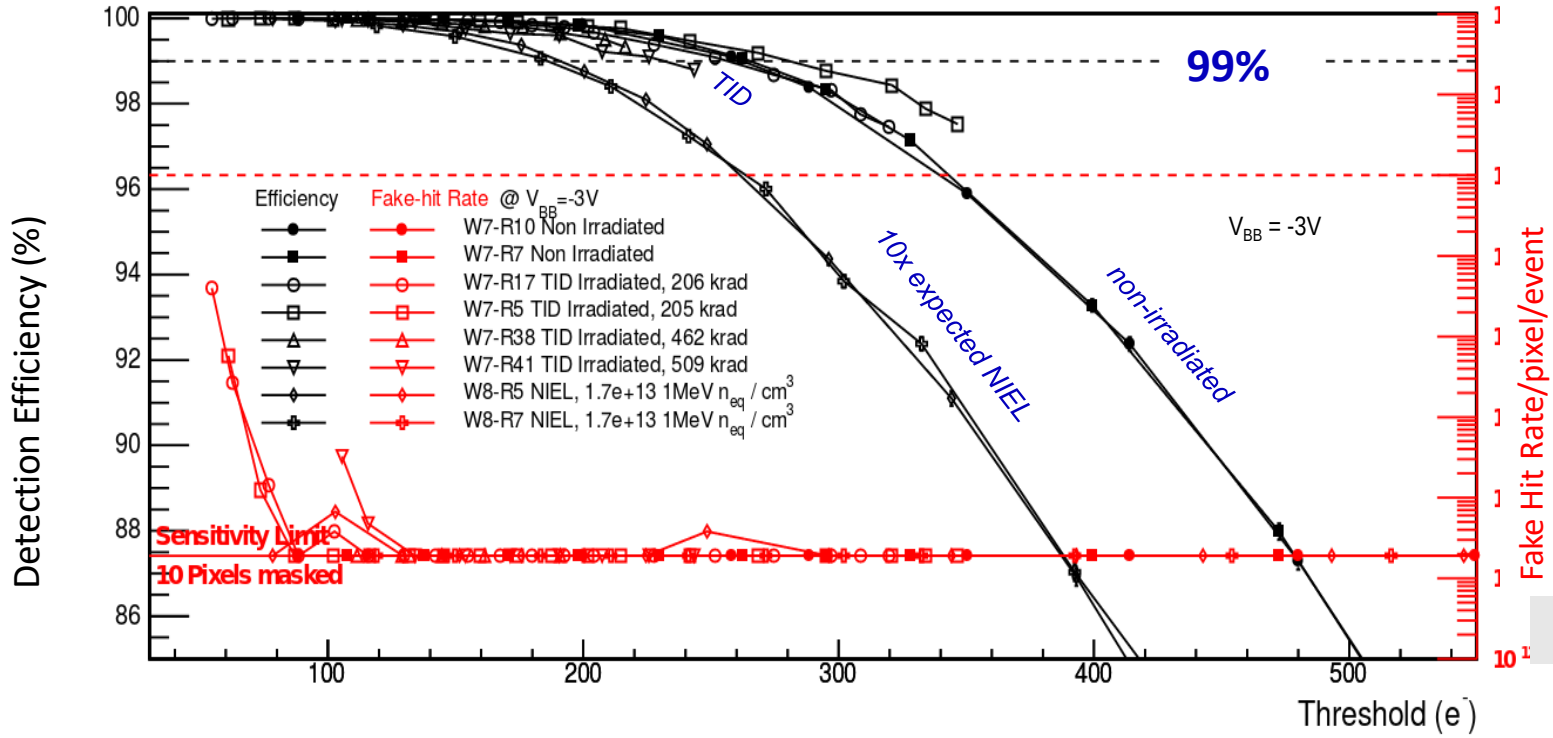
ALPIDE CHARACTERIZATION

- Extensive chip qualification campaign of laboratory and test beam measurements performed on irradiated and non irradiated sensors.



- Studies performed at various **dose rates** and various **doses**
- At doses up **to 500 krad** the chip remains **fully functional** without degradation of performance (Safety factor ~50 for Outer Barrel, Safety factor ~2 for Inner Barrel)
- At **dose rates >20 times** larger than max expected in experiment, no effect of TID observed on digital and analog supply currents up to 320krad
- Single Event Upset and Single Event Latchup cross section measured using proton and heavy ion beams(wide range of LET)
- **SEU** and **SEL** cross sections **not** considered to be a **risk** for the operatonal stability of the ITS

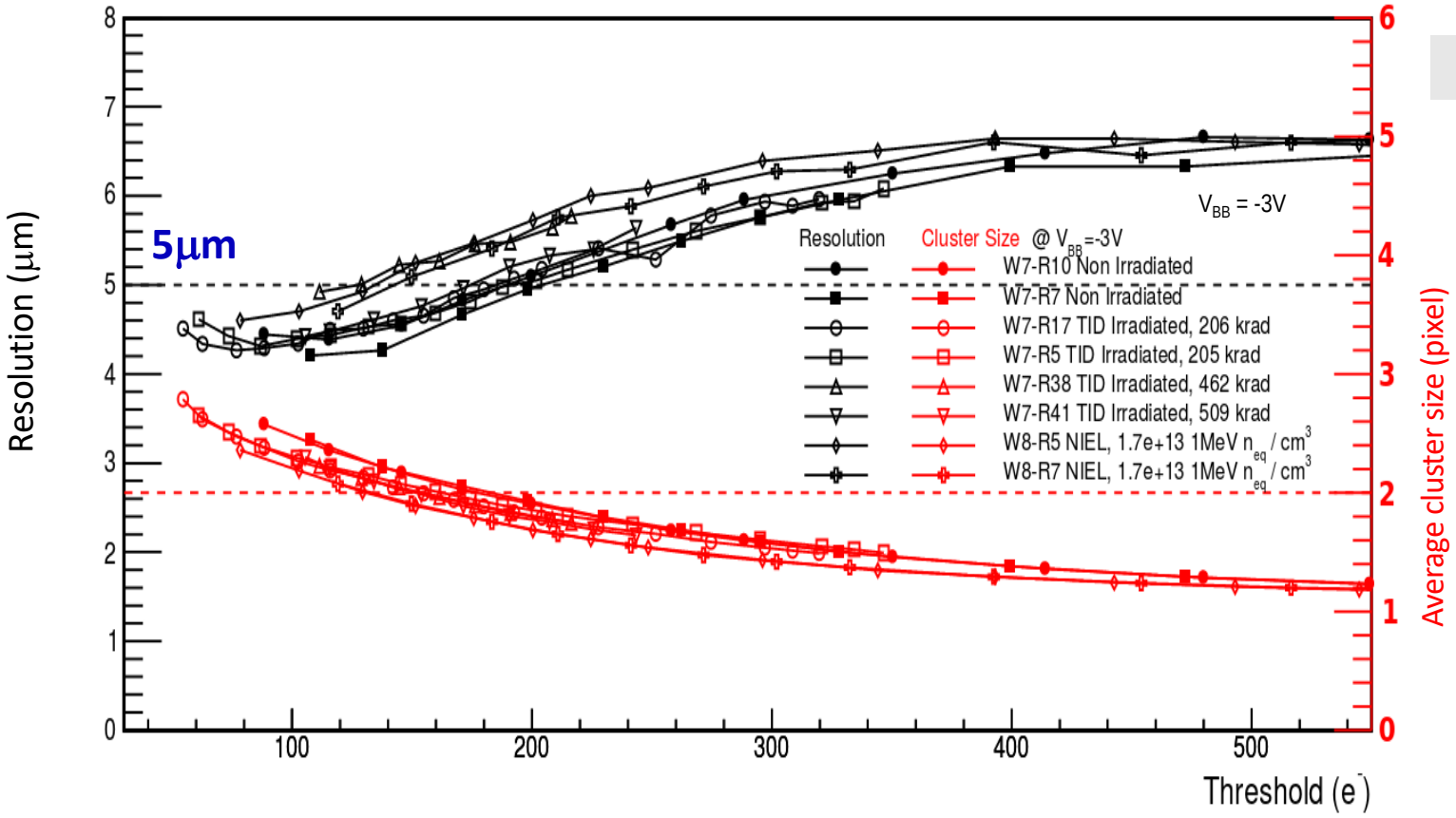
ALPIDE PROTOTYPES: TESTS AND QUALIFICATION



- Negligible chip-to-chip fluctuations
- Sufficient operational margin after 10x lifetime NIEL dose
- efficiency **>99%** up to ~200 electrons threshold
- fake-hit **rate < 10^{-10} /pixel/event** (10^{-6}required) → Big operational margin (only 10 masked pixels)
- **NIEL irradiated chips show no significant degradation of operation margins**

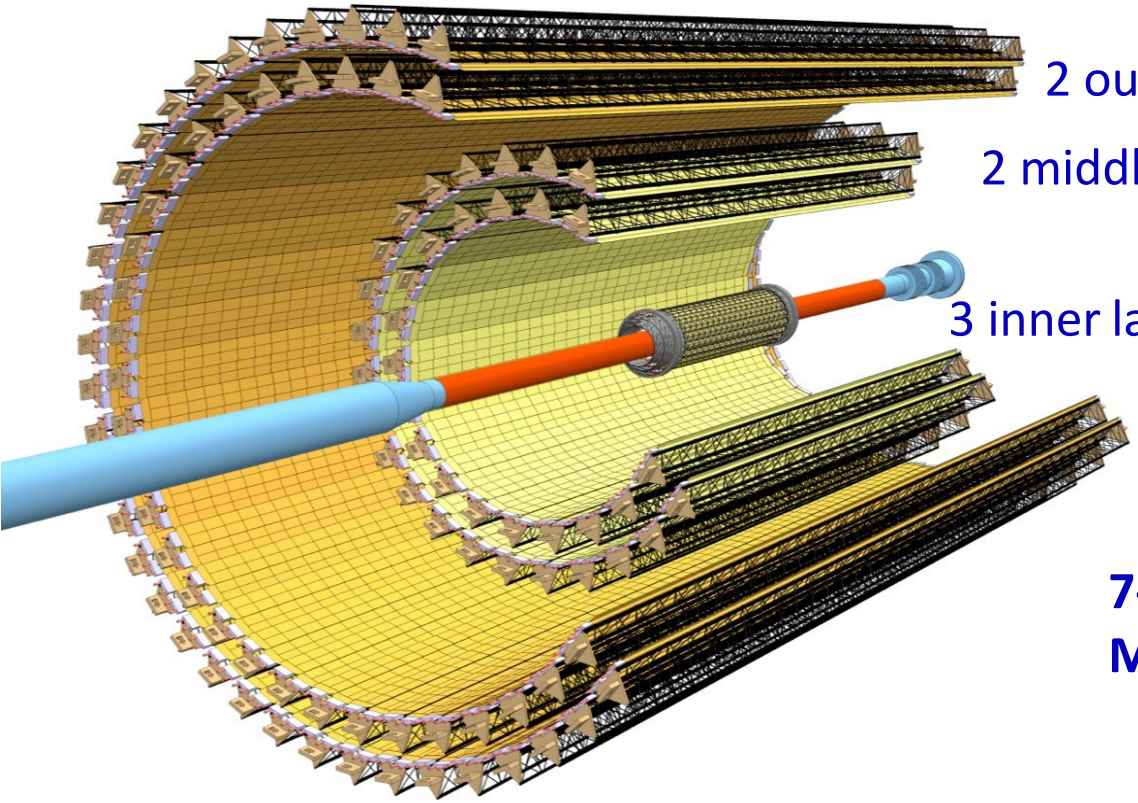
Large margin for efficiency > 99% even after irradiation

ALPIDE PROTOTYPES: TESTS AND QUALIFICATION



- Negligible chip-to-chip fluctuations
- Sufficient operational margin after 10x lifetime NIEL dose
- Resolution of about **5µm** @ threshold of 200 electrons
- **NIEL irradiated chips show no significant degradation of operation margins**

Inner Tracking System Upgrade layout



2 outer layers (90 staves)
2 middle layers (54 staves)
} Outer Barrel (OB)

3 inner layers (48 staves) Inner Barrel (IB)

7-layer barrel geometry equipped with Monolithic Active Pixel Sensors

- 12.5 Gigapixels
~24000 pixel chips
- binary readout
- ~ 10 m^2 active area

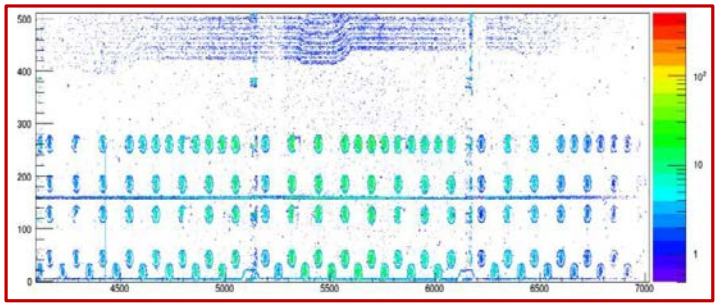
η coverage: $|\eta| \leq 1.22$

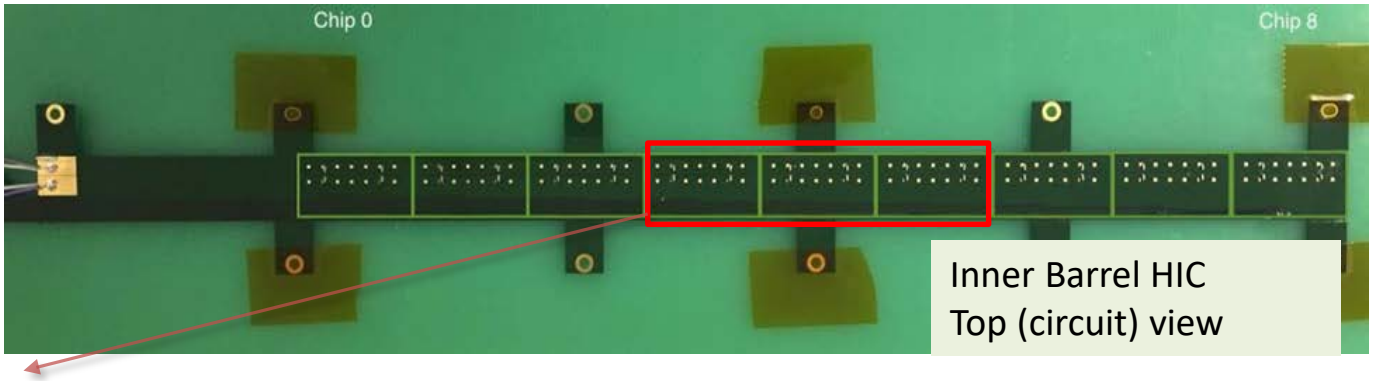
IB **Radius** (mm) ~ **23**, 31, 39
IB stave **length** (mm): ~290

OB **Radius** (mm): ~196, 245, 344**, 393**
Middle layers stave **length** (mm): ~900
Outer layers, stave **length** (mm): ~1500

ITS-Upgrade hybrid integrated circuit

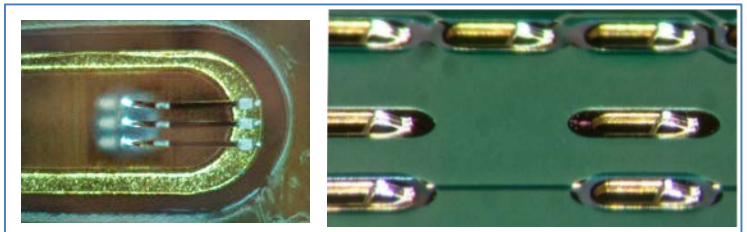
X-ray (^{55}Fe) image of IB HIC



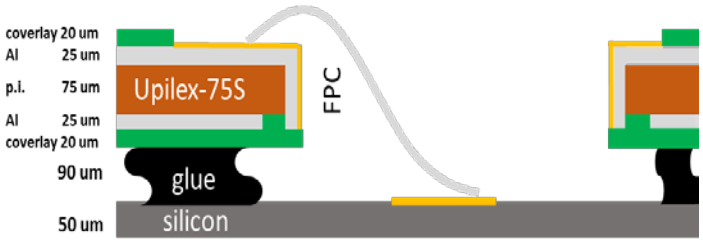


Low mass Hybrid Integrated Circuits (HIC)

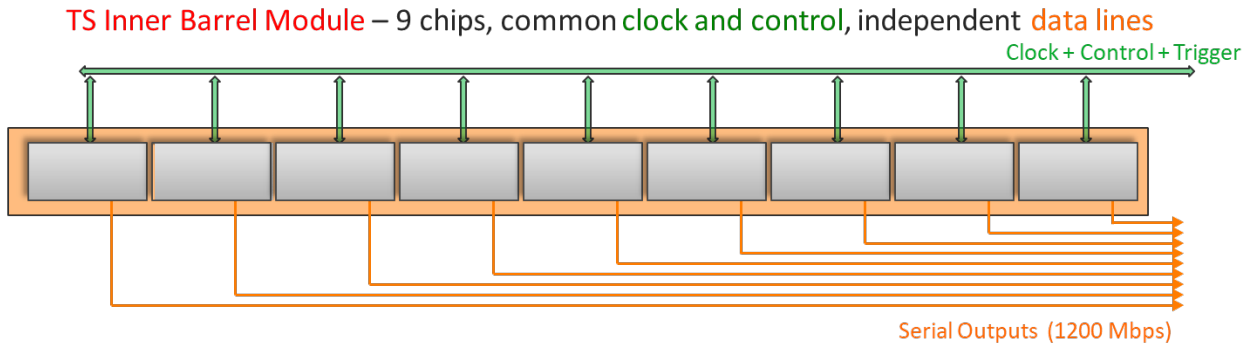
- IB-HIC: **9** master chips (50 um);
- OB-HIC: **2x7** (1 master, 6 slaves) chips (100um)
- IB (OB): double sided Al(Cu)/polyamide Flexible Printed Circuits (FPC)
- Interconnection based on flip chip and wire bonding technology



FPC to Chip interconnection

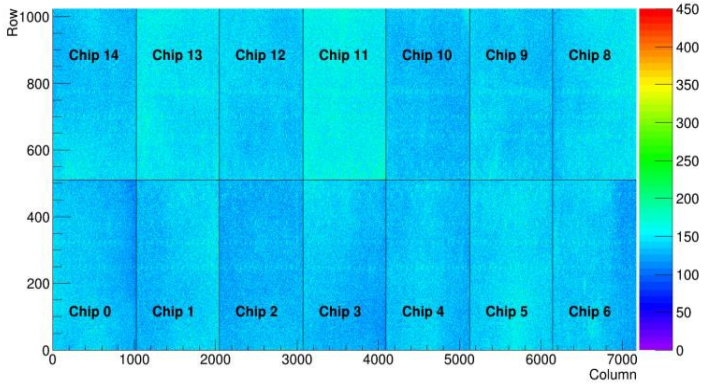


IB HIC cross section scheme

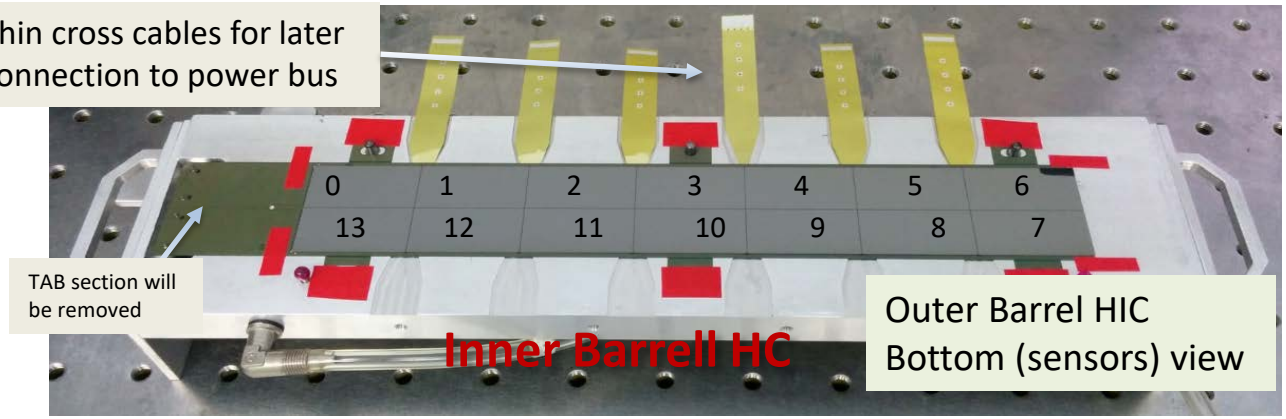


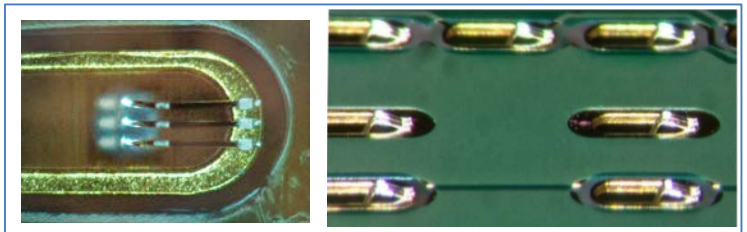
ITS-Upgrade hibrid integrated circuit

Outer Barrel HIC – threshold measurements



Thin cross cables for later connection to power bus

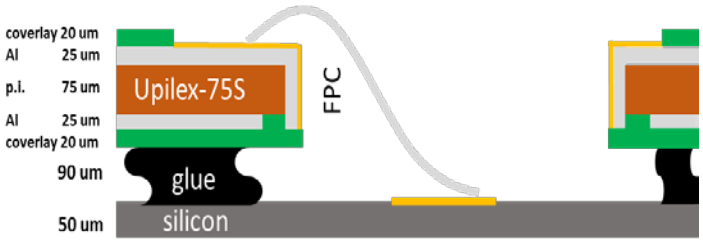




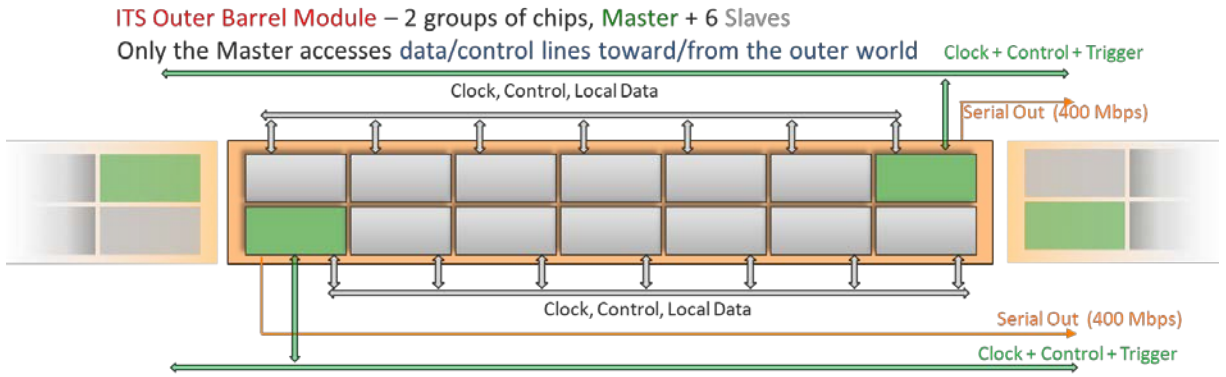
FPC to Chip interconnection

Low mass Hybrid Integrated Circuits (HIC)

- IB-HIC: 9 master chips (50 um);
- OB-HIC: 2x7 (1 master, 6 slaves) chips (100um)
- IB (OB): double sided Al(Cu)/polyamide Flexible Printed Circuits (FPC)
- Interconnection based on flip chip and wire bonding technology

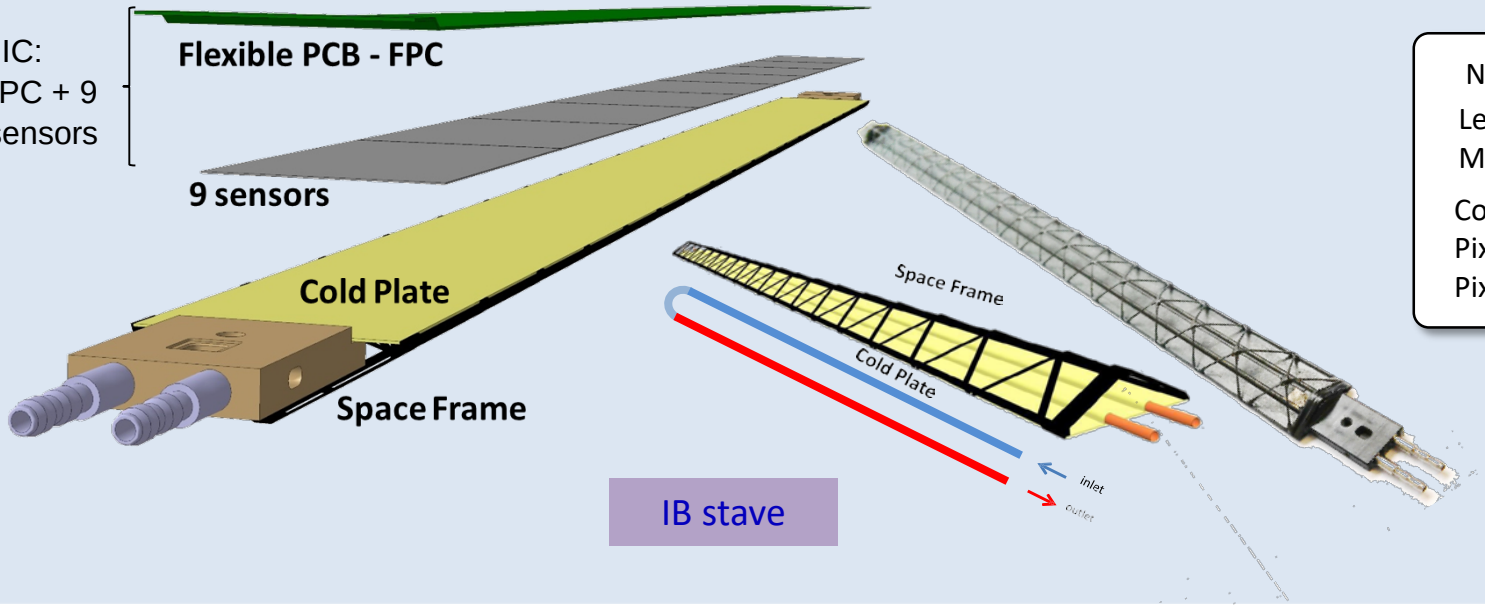


IB HIC cross section scheme



ITS-upgrade staves layout

HIC:
FPC + 9
sensors



IB stave

Nr. Staves: 12, 16, 20
Length in z (mm): **271.2 mm**
Material thickness:~0,3% X_0
Coolant Single-phase H_2O leak-less
Pixel operational temperature < 30°C
Pixel max temperature non-uniformity < 5°C

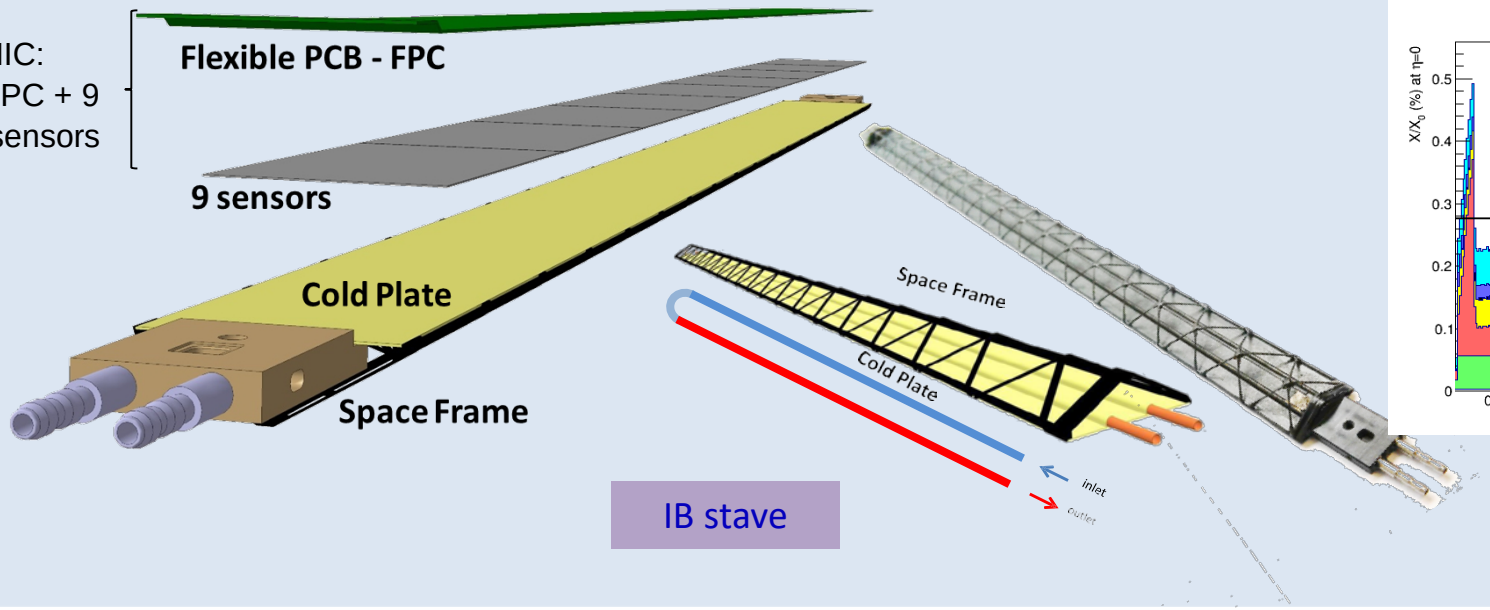
HIC:
FPC + 2x7
sensors

OB stave

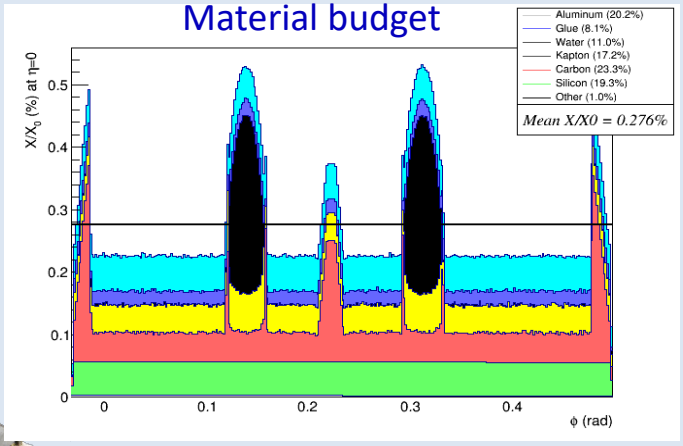
Nr. Staves: 24,30,42,48
Nr. Chips/ module:2x7
Length in z (mm): 844.2 (ML), **1477.5 mm** (OL)
Material thickness:~1% X0
Coolant Single-phase H_2O leak-less
Pixel operational temperature < 30°C
Pixel max temperature non-uniformity < 5°C

ITS-upgrade staves layout

HIC:
FPC + 9
sensors



IB stave



HIC:
FPC + 2x7
sensors

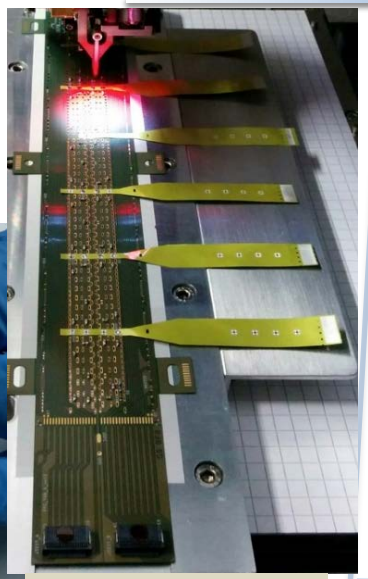
OB stave

Staves Material budget

IB: ~0.3% X_0 OB: ~1% X_0

- Ultra-light stiff space frame C structure
- Ultra-light C laminate Cold Plate (with integrated polyimide cooling ducts; single-phase H_2O coolant
- Low mass Hybrid Integrated Circuit

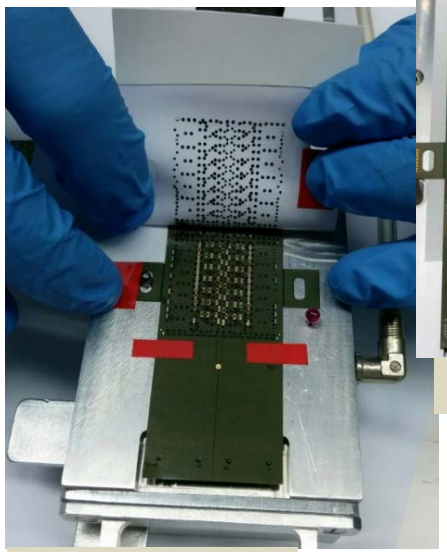
HIC, STAVE, MECHANICS, ASSEMBLY PRODUCTION



Chip interconnection

TAB removal

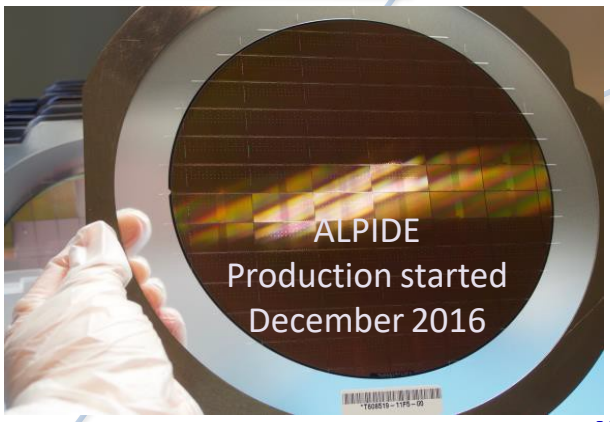
HIC Preparation for assembly

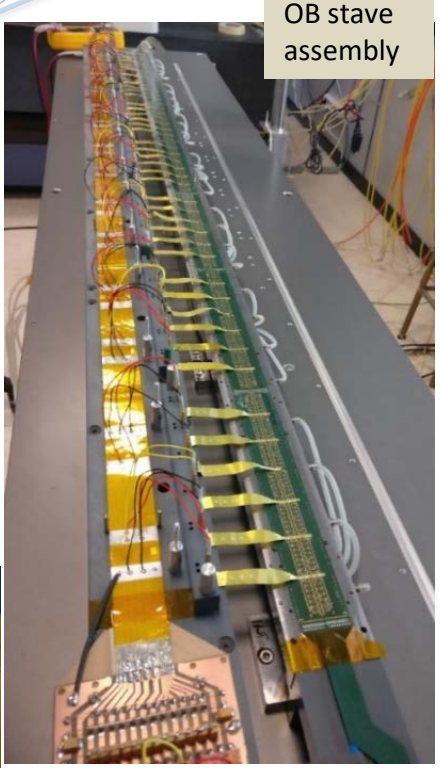


OB Glue spreading

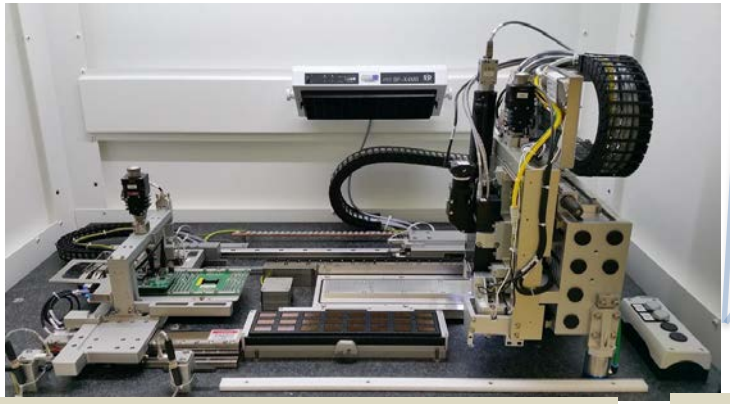
HIC assembly

Staves production: Cold plates and space frames



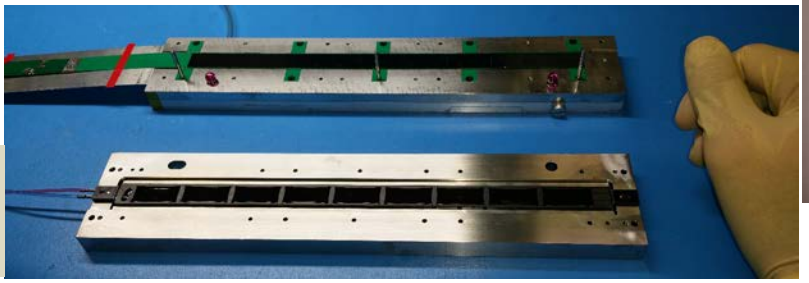


OB stave assembly



Automated module assembly machine

IB and OB staves assembly

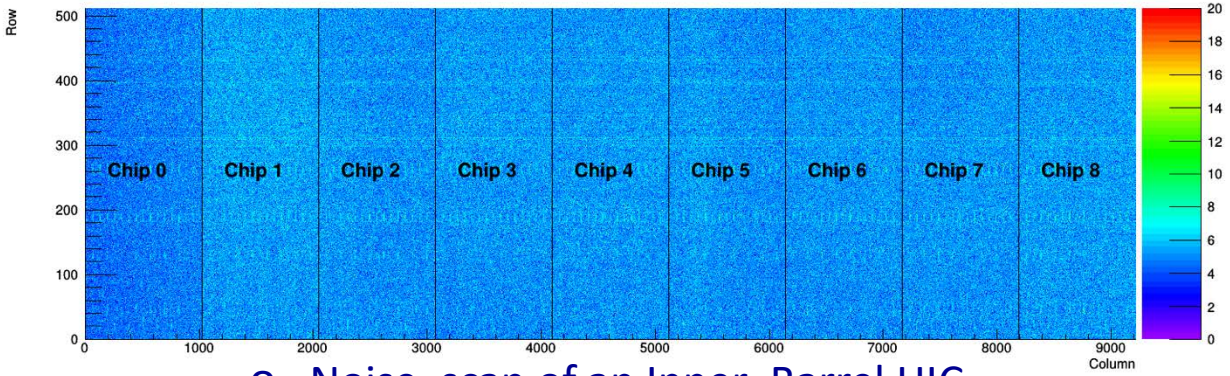


IB Space Frame + HIC gluing

HICS AND STAVES PROTOTYPES CHARACTERIZATION

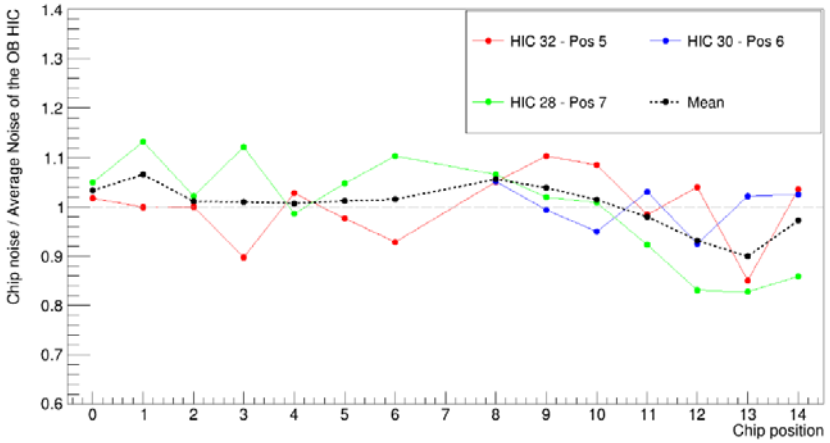
HICs and Staves prototypes

- HICs were characterized in different conditions, operation modes and readout rates
- No significant difference in performance found between standalone chip and chip mounted on HIC
- No significant difference in performance found between HICs and HICs mounted on staves.
- **All performances comparable to standalone ALPIDE chip**

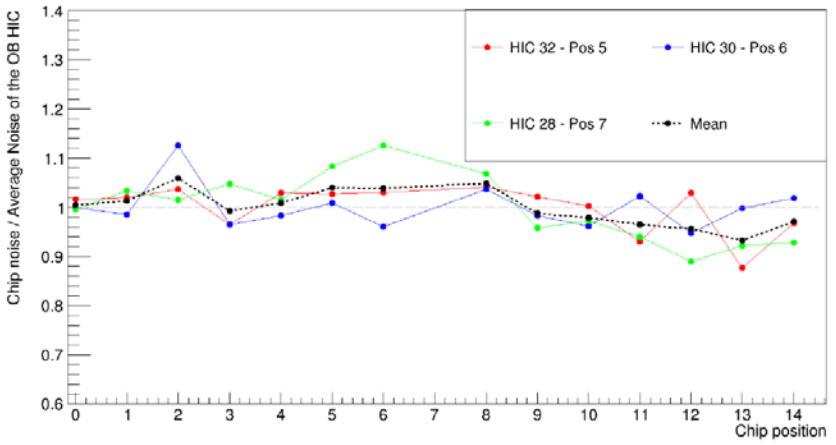


o Noise scan of an Inner Barrel HIC

Noise/Average noise-- after mounting



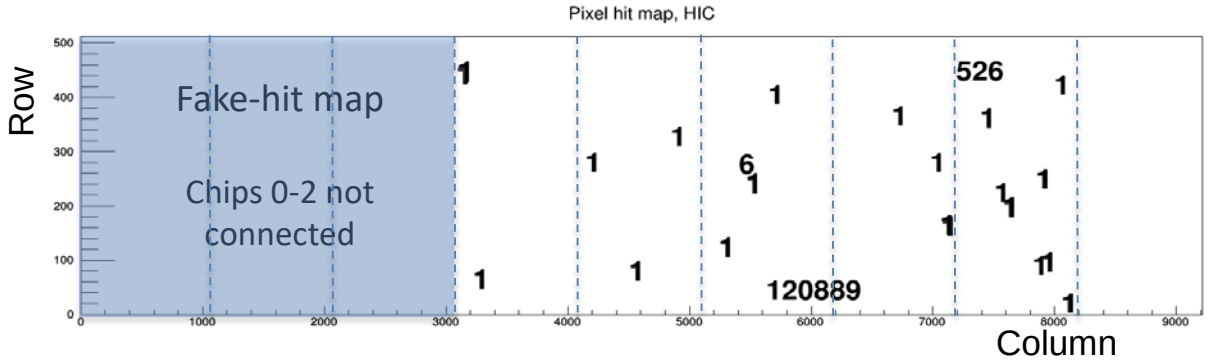
Noise/Average noise-- before mounting



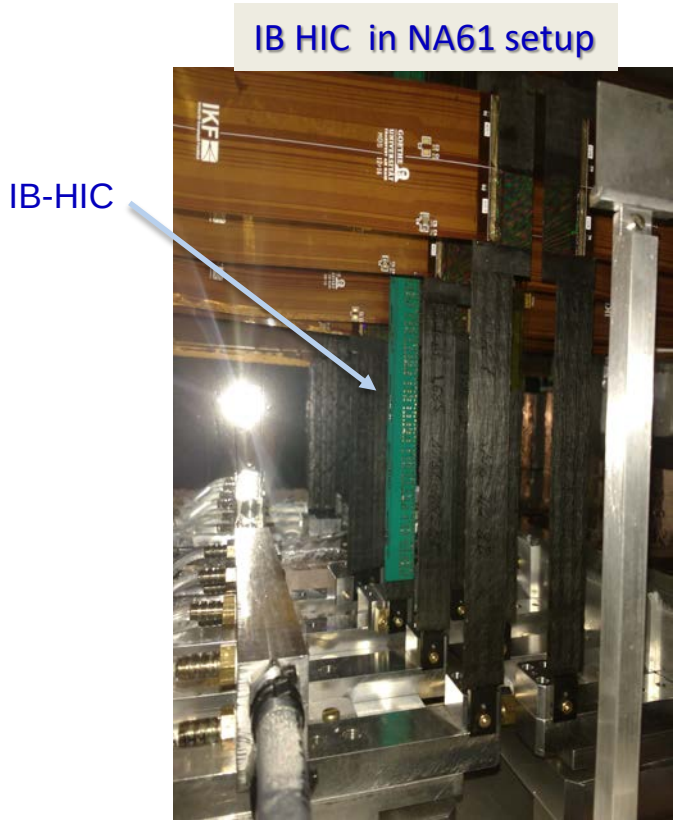
HICS AND STAVES PROTOTYPES CHARACTERIZATION

IB stave tested in Pb-Pb run in NA61/SHINE experiment

- Hit densities: up to 30 hits/cm^2 (realistic Pb-Pb ALICE running conditions)
- No cooling, no substrate reverse-bias used.
- **Fake hit rate < 10^{-10} hits/pixel/event (10 pixels masked)**
- **Detection efficiency: >99%**
- **Performance comparable to standalone ALPIDE chip**



IB HIC in NA61 setup



ITS-UPGRADE

Parameter	Inner Barrel	Outer Barrel	ALPIDE
Silicon thickness	50μm	100μm	OK
Spatial resolution	5μm	10μm	~ 5μm
Chip dimension	15mm x 30mm		OK
Power density	< 300mW/cm^2	< 100mW/cm^2	< 40mW/cm^2
Event-time resolution	< 30μs		~ 2μs
Detection efficiency	> 99%		OK
Fake-hit rate *	< 10^{-6}/event/pixel		< 10^{-10}/event/pixel
NIEL radiation tolerance **	1.7×10^{13} 1MeV n_{eq}/cm^2	10^{12} 1MeV n_{eq}/cm^2	OK
TID radiation tolerance **	2.7Mrad	100krad	tested at 500krad

* revised numbers w.r.t. TDR

** including a safety factor of 10, revised numbers w.r.t. TDR

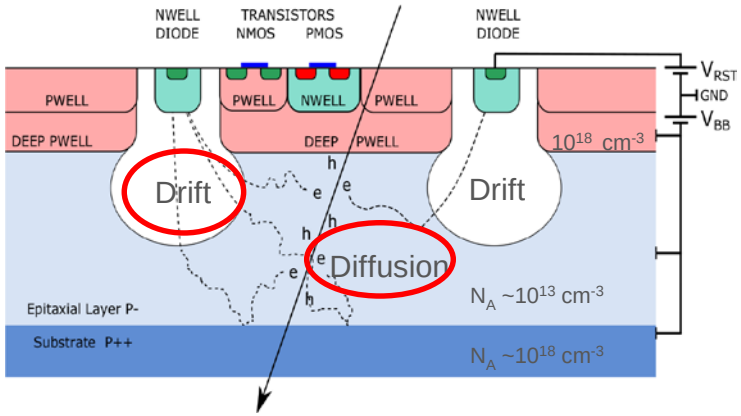
- The new tracker fulfills or even exceeds the requirements of the ALICE ITS upgrade
- ALPIDE represents a significant advancement for what concerns power density, fake-hit rate, readout speed, and radiation hardness
- Use of monolithic CMOS pixel sensors in more demanding environments requires greater radiation tolerance and better timing resolution

TOWARDS HIGHER PERFORMANCES

Diffusion in **undepleted** volume major **limitation** in high radiation environment

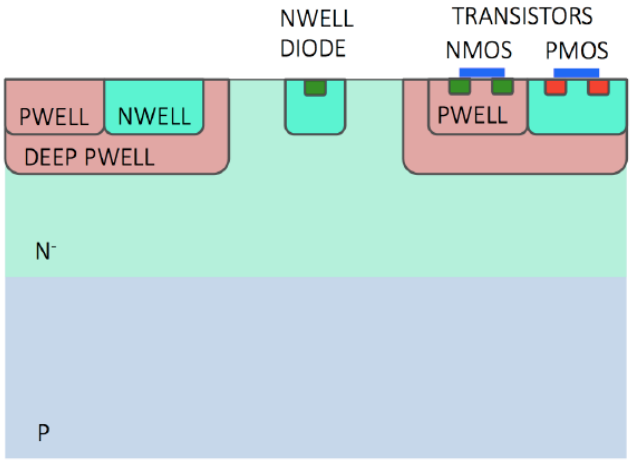
- Slow process
- Recombination, trapping

-> severe **charge loss** in strongly irradiated silicon



ALPIDE partial depletion extends the operability of MAPS

Extended depletion volume allows **faster** and more **efficient** charge collection by drift (less charge loss, more charge in seed pixel, better S/N).



Recent developments: TowerJazz modified Process

- Add **planar n-type layer** (planar p-n junction)
- Significantly improves depletion under p-well with deep junction

Investigator: dedicated test chip within ALPIDE R&D

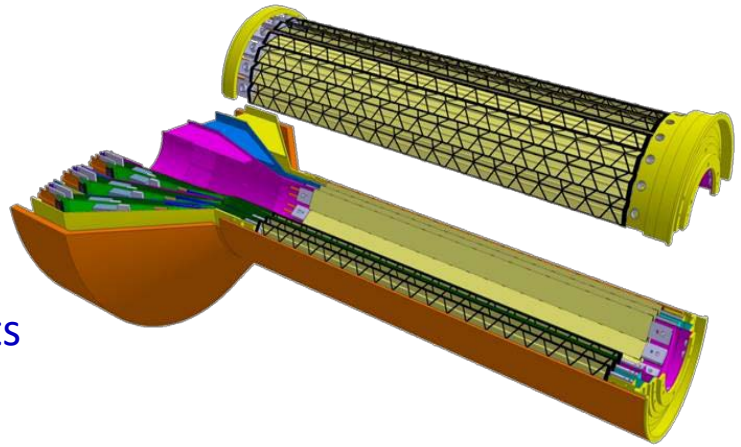
Investigator + modified process: tested within R&D of new radiation hard chips for ATLAS upgrade. Encouraging results up to 1x10^{15} 1MeV n_{eq}/cm^2 (NIEL) and 1Mrad (TID).

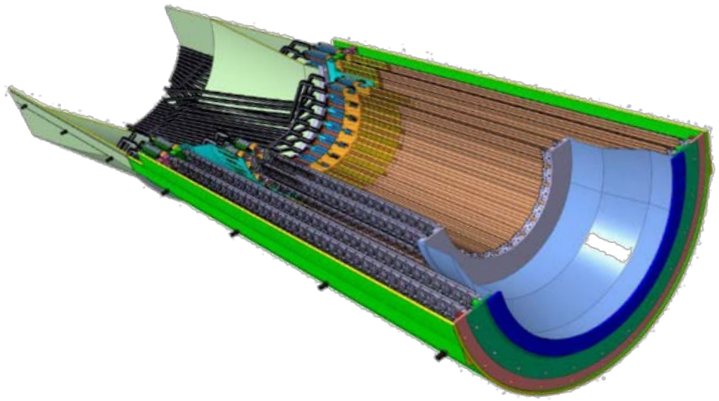
TJ MALTA and TJ MonoPix : new dedicated chips being submitted (ATLAS Upgrade)

Achieving these goals can be a major step towards radiation hard and fast CMOS sensors.

CONCLUSIONS - I

- The ALICE collaboration will perform a major detector upgrade during LS2 to improve readout and tracking capabilities for runs 3&4 at LHC.
- The ALICE Inner Tracking System Upgrade project has successfully completed the R&D phase. All requirements have been met or exceeded.
- The ITS Upgrade will be the largest existing pixel detector with an innovative monolithic pixel sensor with in pixel full CMOS circuitry.





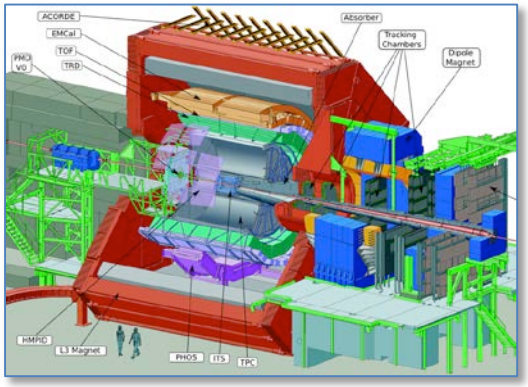
- Detector production started Dec 2016 with the ALPIDE chip start of production.
- All sites are entering the production phase, expected to finish by the end of 2018.

CONCLUSIONS - II

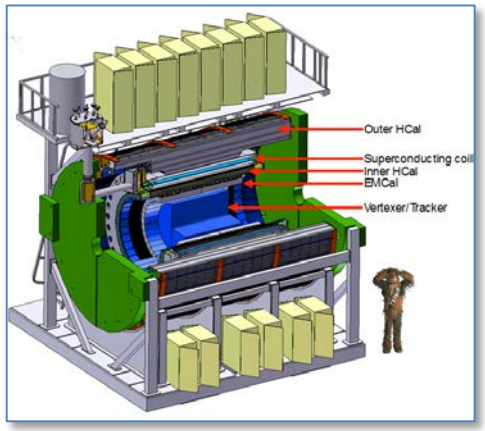
- Several experiments have decided to instrument their detectors with MAPS (ALICE, S-Phenix, CBM, MPD...).

- **ALPIDE**, developed for the new ALICE tracker, represents a **significant progress** regarding power density, fake-hit rate, radiation hardness, readout speed, in the field of Monolithic Active Pixel Sensors.

- ALPIDE development important step towards the use of monolithic CMOS pixel sensors in future experiments. More demanding environments require further developments .

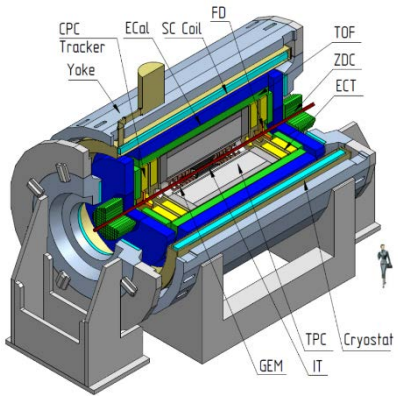


ALICE ITS Upgrade (and MFT)
10 m^2 – 12 G pixel

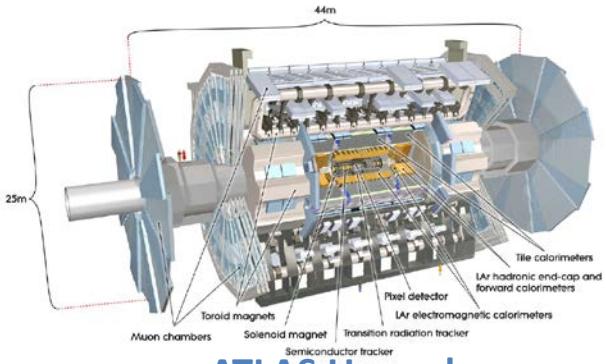


sPHENIX
0.2 m^2 – 251 M pixel

- Firsts tests with R&D chips and TJ modified process very promising.
- Strong R&D ongoing for development of chips for HL LHC (ATLAS ITK) and future experiments.



MPD @NICA



ATLAS Upgrade
High Luminosity LHC