AM08 & AM2020 requirements from ATLAS

Alberto Annovi

INFN Pisa

Work plan

- AM08 final prototype will all features
- AM2020 large area device
- AM08 Main goals
  - Have one “core” with known full custom with the main goal of using it for pattern matching to test the basic functionality on board
  - Test all the features that we want in AM2020
    - Use additional “cores” to make sure we can test all features even in case one features is not working

AM08 vs AM2020 goals

- We need to design AM08 keeping in mind AM2020 goals
- Let's avoid "this was decided for AM08 we have to change it for AM2020"
- In order not to forget AM2020… which is the ultimate goal… write specs for both!
  - **Keep AM2020 specs updated along the AM08 design**
  - Make sure for every AM08 choice we evaluate the impact on AM2020 in addition to AM08 impact

	AM08	AM2020
Parameter 1	value	value
Parameter 2	value	value

AM08/AM2020 requirements

- Large pattern density per chip: goal 512k patterns/chip
  - 8 bus, 16 bits input words, 18 bits memory (TBC)
- Input clock speed 250MHz – 500MHz
- Low power consumption
  - Need 0.4 fJ/comp/bit at 50% bit flip (more info later)
    - Some stress here … to be discussed
  - Per bit means per input bit (16 bits per word)
  - 0.5 fJ @ 100% usage 250 MHz 50% bit flip implies: 8W
    - (0.5E6*8*16*250E6)*0.5E-15
- Output bandwidth not defined yet
  - Less than 2 busses of 32 bits running at input clock speed
  - Shall we define this to be 250MHz in any case?

AM08/AM2020 requirements

- MLM submission: minimize submission cost
  - Keep under control NRE cost (# of layers, additional processes)
  - Will include 6 wafers from different corners
- Follow up with large production
- ATLAS possible production numbers
  - Regional tracking 6400 good AM2020 (|eta|<4)
  - Full scan tracking 12800 good AM2020 (|eta|<4)
  - Regional tracking 4000 good AM2020 (|eta|<2.5)
  - Full scan tracking 8000 good AM2020 (|eta|<2.5)
  - Changes to be expected

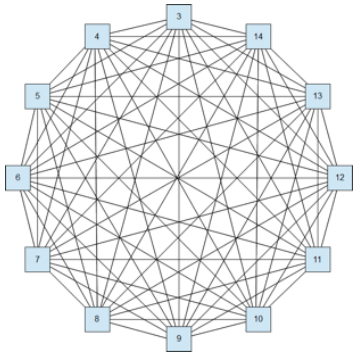
IO (worst case)

- Input 8 buses (0.2-0.4mW/pair)
  - Each at 16 bits * 500MHz = 8Gb/s
  - For each bus use four 2Gb/s pairs (eventually max FPGA speed)
  - Total of 32 pairs for ≈12.8mW
- Output 2 busses (8.5mW/pair)
  - Each at 32 bits * 500MHz = 16Gb/s
  - For each bus use eight 2Gb/s pairs (eventually max FPGA speed)
  - Total of 16 pairs for ≈136mW
- Controls
  - ~30 input signals?
  - ~10 output signals?
- Total <200mW power (assume <300mW with control signals)
  - The chip could be a 6-8W device
  - Power estimate for FPGA outputs 60 pairs @ 8.5mW = 500mW
  - What is the power for one FPGA input and output pair?

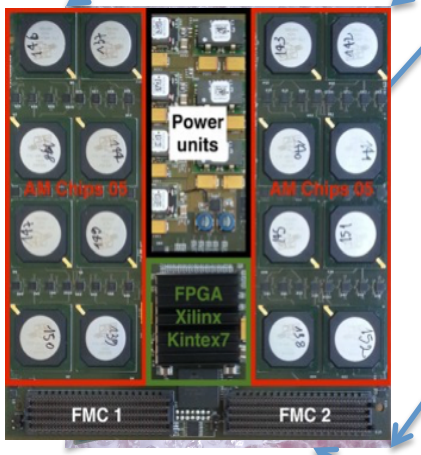
INFN proposal for a common & modular HW model

ATCA

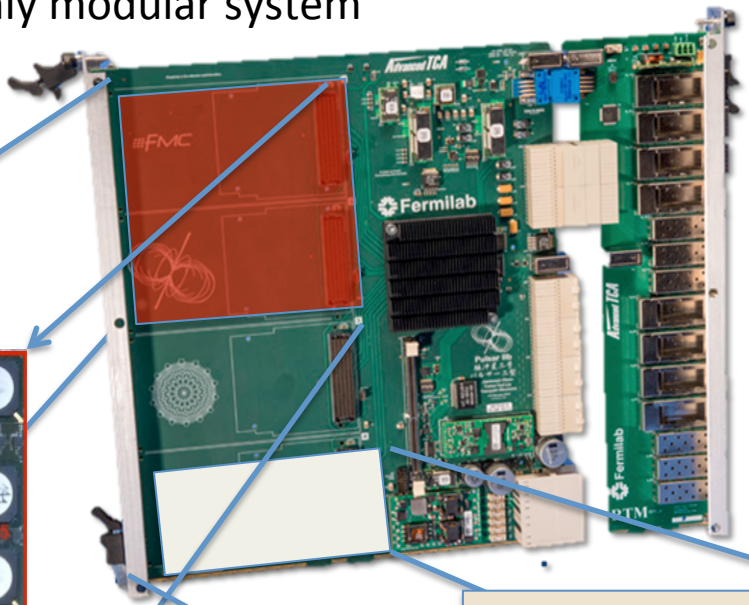
40Gb/s board-board
*2 (bidirectional)
*91 links
=O(7 Tb/s)



Highly modular system



FPGA
+AM

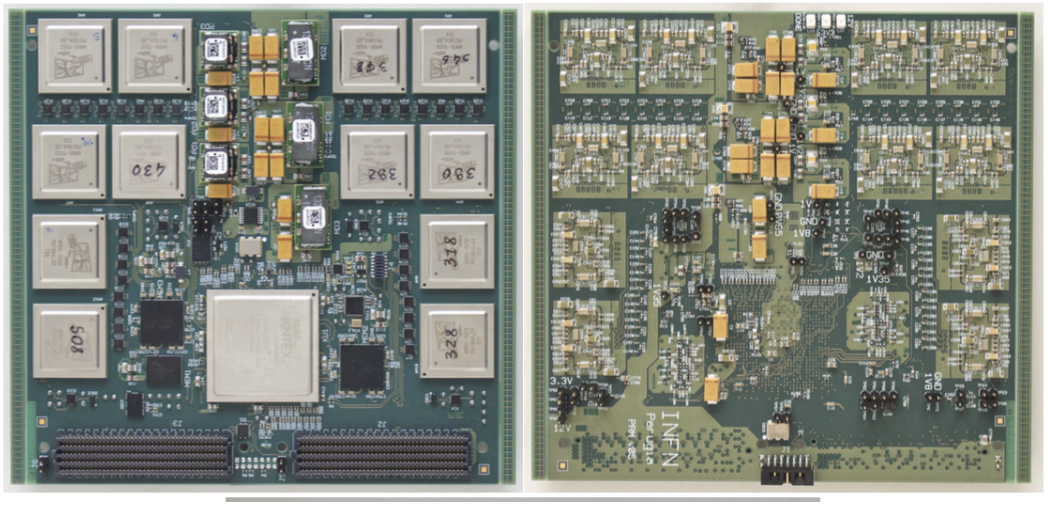


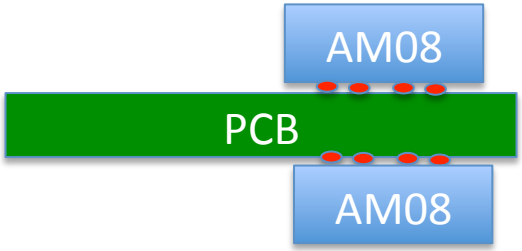
FPGA(s) + RAM(s)
second stage fit

future AM chip

x16

PRM06: Mezzanine with AM06

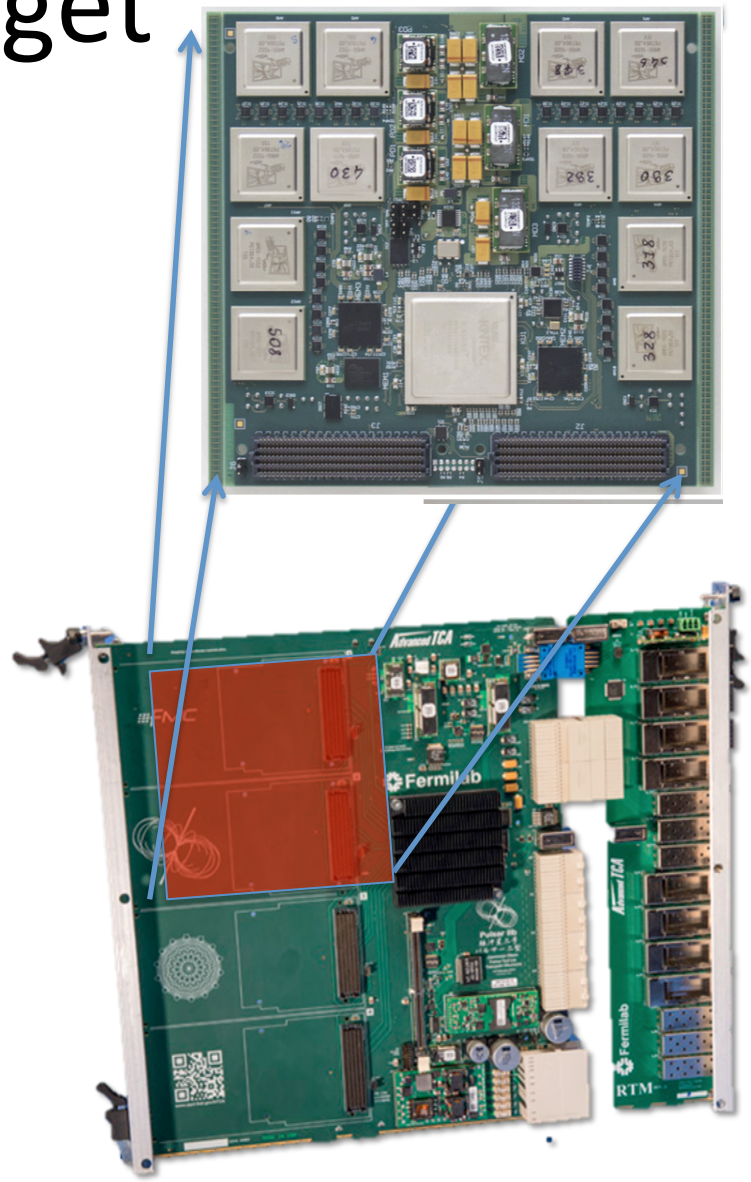




- Future PRM with AM08/AM2020 will be “similar”
- Embed caps in the package to allow AM chips on both sides.
  - Do you see issues with this?
  - Save area. Allow contingency in case pattern density below 512k/chip
  - Could simplify routing (if and only if) ball layout carefully designed?
    - Could we distribute a single LVDS signal to two chips?

Power budget

- 400W per ATCA slot
  - Allocate 100W to main card
- Allocate 150W per PRM
  - 50W to FPGA
  - 100W for 16 AM2020
    - 6W per chip (including IO and DC/DC converter efficiency)
- DC/DC efficiency to be accounted for all contributions
  - 48V input
  - 48V to 12V at ~92%
  - 12V to final at ~92%
  - Overall efficiency ~85%



AM2020 power budget

- 100W for 16 AM2020
  - 6W per chip (including IO and DC/DC converter efficiency)
  - 5W at 85% efficiency
  - 4.8W for processing, 0.3W for IO
  - At 250MHz 100% usage → 0.3 fJ/comp/bit
  - At 0.5fJ can do ~60% usage
  - Assume >=75% usage → need < 0.4 fJ/comp/bit
  - Specs at 0.4 fJ/comp/bit !!!

Let's avoid surprises later on

- We need to design AM08 keeping in mind AM2020 goals
- In order not to forget AM2020… which is the ultimate goal… write specs for both!

- Start allocating area, power, latency, other(?) budget for both AM08 and AM2020 !
  - The sooner we have a good estimate (specs) for each piece of AM08 (and AM2020) the better
  - We know the "future" from AM06 experience
    - no (or at least less) surprises for AM2020