AM chip requirements

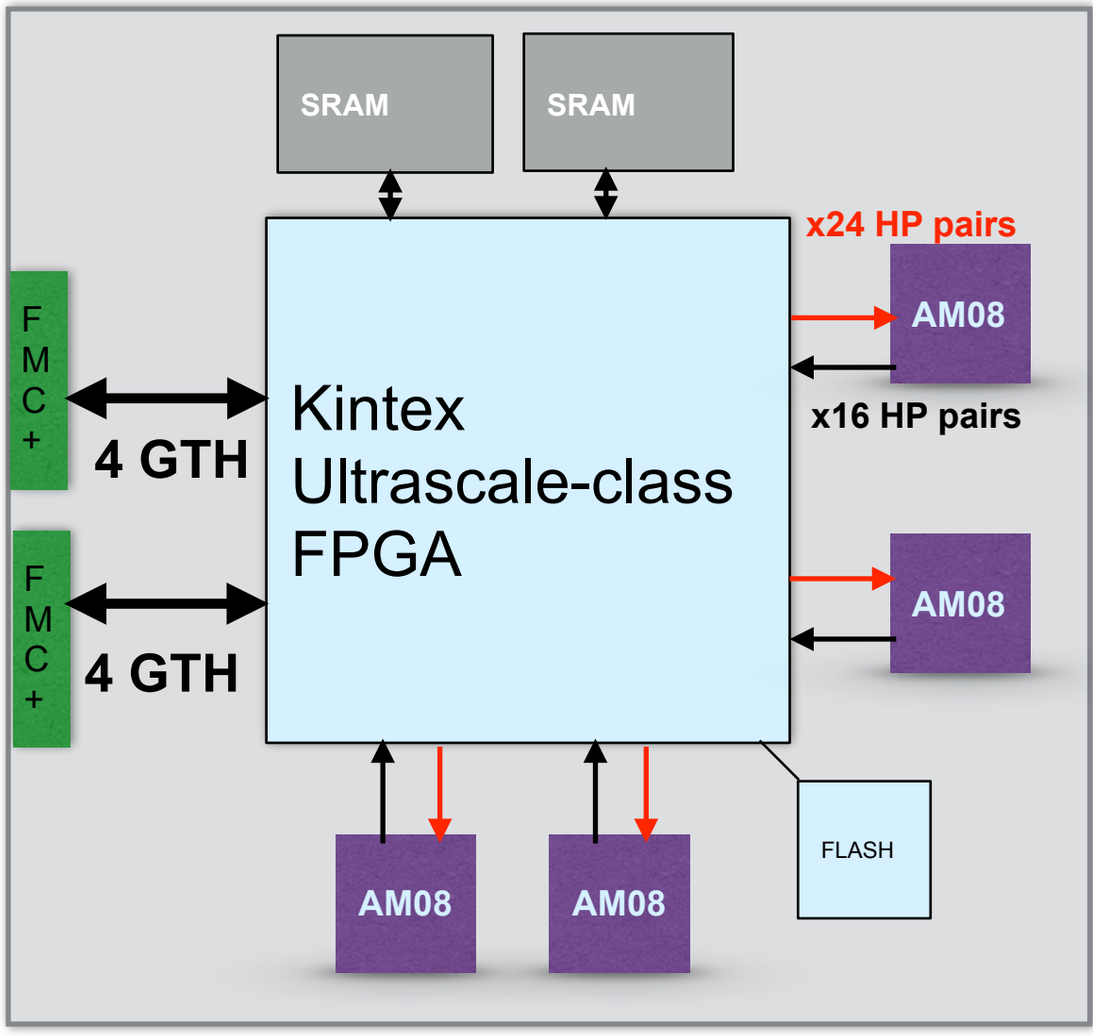
- From the system demonstration studies (T. Liu talk):
  - Maximum number of patterns/tower ~ 1.3 M patterns (hybrid 2 GeV)
    - Pattern density ~ 300k patterns/AM chip → 4 AM chips/PRM
  - A fast chip: AM clock ~250 MHz
  - Power limit to less than ~10 W/chip
  - Pipeline processing of the events:
    - Load events of "next event" N+1 while outputting matched roads of the "current event" N
  - Chips to be operated in a PRM and with 1:1 connection with the FPGA
    - Limits the number of I/O lines to and from the AM chip
- Thanks to the interplay between the AM and the FPGA the requirements are not that strict but leave some level of margins.

AM08 chip possible design

- AM08 chip
  - 28 nm technology TSMC - core frequency 250 MHz
  - Pattern density: 0.4-0.5 M Patterns/chip (3-4 times AM06) - but AM08 will be a test chip!
  - 8 input buses at 16 bits
    - each bus has 4 HP pairs running at 1.25 Gbps.
    - In CMS only 6 buses are used in the AM - 8 input buses is to remain compatible with ATLAS
  - 4 output buses@32 bits (of which 19 for patterns and 8 for bitmap)
    - each bus is has 4 HP I/O pairs running at 1.25 Gbps
  - Every chip will have 32 input HP pairs + 16 output HP pairs, with a total of 96 signal balls
    - For CMS only 24 input pairs are connected (6 layers only)
  - Power estimate (for full chip)
    - Energy per comparison/bit: extrapolate from KOXORAM ~0.2 fJ/comparison/bit to full chip 0.5 fJ/comparison/bit
    - For 500 k patterns/8 layers@250 MHz, 100% usage: 8 W

How could it fit into a PRM for CMS?

- A double FMC PRM08 mezzanine exercise
  - Double FMC(*) from Pulsar board
    - 2x4 GTH (up to 16 Gbps) - 8 layers
    - Possible to process 120+ Gbps (x10 TM)
  - 4 AM08 chips fed in parallel
    - 4x [24_{IN} (6 layers) + 16_{OUT}] HP pairs
    - up to 1.5-2 M patterns
      - could accommodate 2 GeV thresholds
  - Parallel I/O allows to reduce latency
  - 2 SRAM
  - Power from AM08 ~32 W
  - Power from FPGA+all the rest ~35 W
- Power per ATCA blade due to 2 PRM08 ~150 W



- We have studied a design compatible with 16 AM chips for ATLAS (see backup slides)

*NB: FMC connectors could be for example replaced by SAMTEC SEAM-XX

Plan-B

- **Change minimally AM06**
  - revise I/O registers and logic
    - replace SER-DES with LVDS
    - replace registers and Fisher tree in the output to accommodate shorter latency (ideally ~10 clock cycles)
    - increase clock frequency to ~200 MHz