Open issues on the logic and digital simulations

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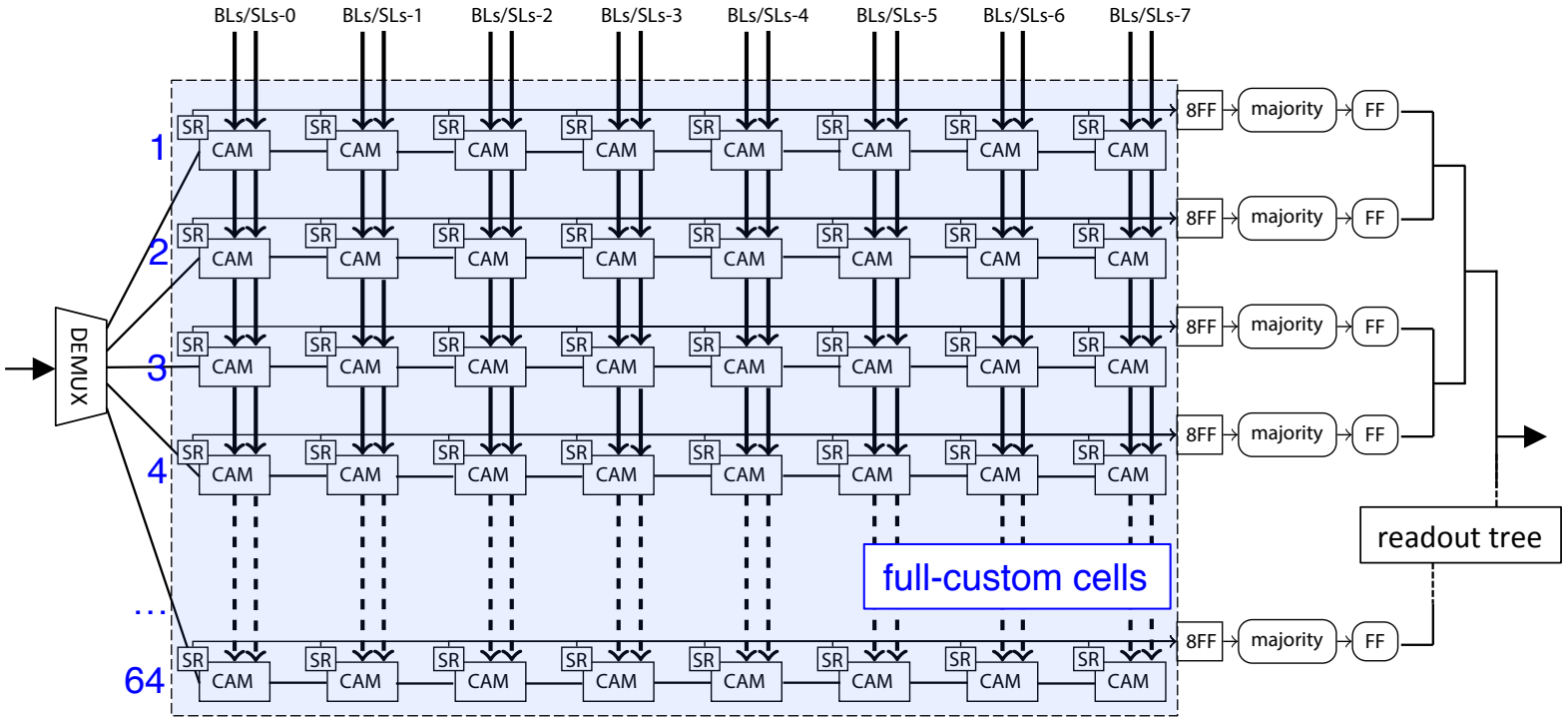
Basic structure: 64 CAM block

- The 64 CAM block consists of the following components:
  - Full-custom cells (DOXO/KOXORAM): **18** bit word × **8** layers × **64** blocks
  - Data buses with positive/negative bits:
    - Bit-lines (BLs) to write patterns in CAM segments
    - Search-lines (SLs) to distribute the detector hits to CAM segments
  - De-multiplexer to control write-lines (WLs)
  - Majority logic, FFs and readout tree



AM07 logic overview/open issues

- Based on the VHDL used in AM06, with some modifications:
  - LVDS I/O for bus0
  - DDR mode for bus1-7
  - Double edge clock strategy
  - Clock-less circuit (17^{th} bit plays the role of enable bit)
  - Share wires on top-level between the normal/BIST logics
- Missing components from AM06:
  - SER/DES related components
  - JTAG
- Open issues:
  - The combination of LVDS I/O and DDR mode is not tested
  - AM08 will go to higher clock (500 MHz). Some warnings seen in the AM07 validation could turn into errors?

AM07 logic validation result

MAXIMUM condition

	150 MHz	200 MHz	250 MHz	300 MHz	350 MHz	400 MHz
DOXORAM	OK	OK	ERROR	NA	NA	NA
KOXORAM	OK	OK	ERROR	NA	NA	NA

TYPICAL condition

	150 MHz	200 MHz	250 MHz	300 MHz	350 MHz	400 MHz
DOXORAM	OK	OK	OK	OK*	OK	ERROR
KOXORAM	OK	OK	OK	OK*	OK	ERROR

*: used negative edge

MINIMUM condition

	150 MHz	200 MHz	250 MHz	300 MHz	350 MHz	400 MHz
DOXORAM	OK	OK	OK	OK	OK	OK*
KOXORAM	OK	OK	OK	OK	OK	OK*

*: used negative edge

Some paths are very tight

- A FF in the DDR module
  - Actual setup time is only 41 ps whereas the threshold is set at 211 ps; the timing is already very tight

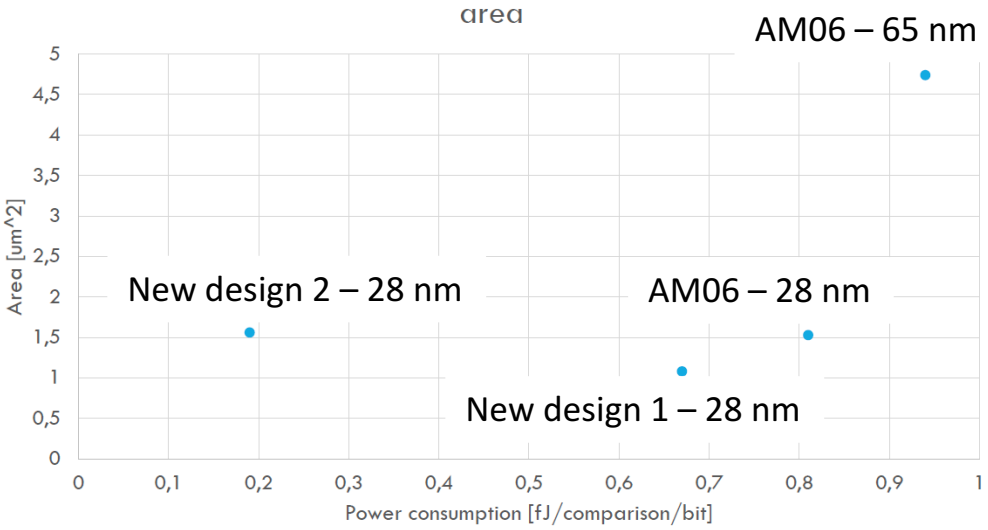
```
Warning!  Timing violation
          $setuphold<setup>( negedge CPN &&& nD_SI_SDFCHK:8113 PS, posedge SE:8072 PS,  0.211 : 211 PS,  -0.008 : -8 PS );
           File: /home/tsmc28/TSMCHOME/digital/Front_End/verilog/tcbn28hplbwp12t_120b/tcbn28hplbwp12t.v, line = 75575
          Scope: demo_top.dut.inst_en_ddrmode.\tmp_OutBusBLn_reg[5][1]
           Time: 8113 PS
```

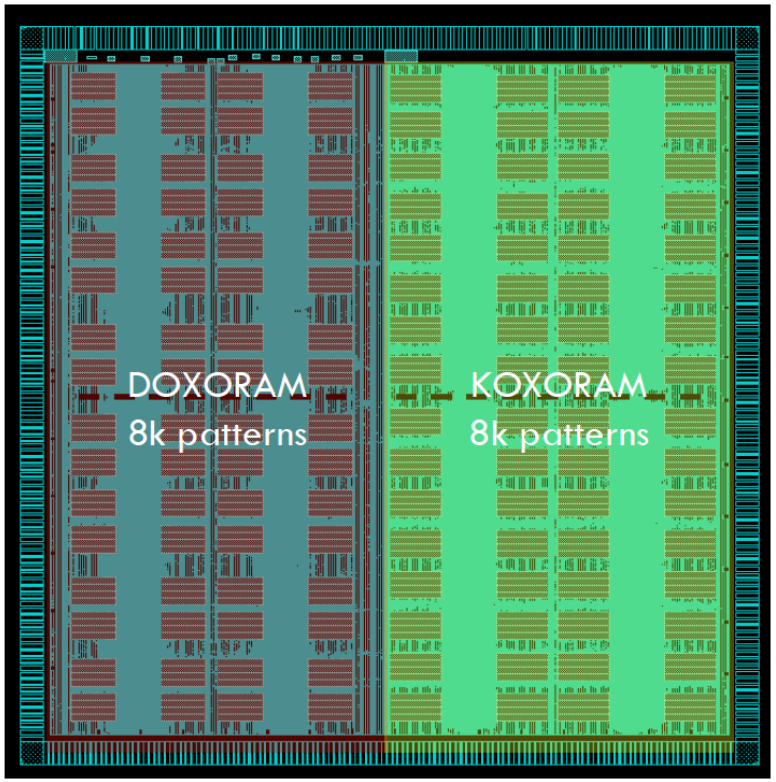
- Need better understanding of delay of each part
  - Full-custom front-end design could change the picture; not very efficient to start from understanding the timing of AM07
- Need consideration in structuring workflow so we can exploit the maximum number of iterations in optimising the timing
  - For example, statistic timing simulation should be done by the VHDL programmer?

The front-end logic size

- Area for front-end logic started limiting the total density
  - Convert a part of front-end logic into full-custom to fully exploit the gain in the full-custom part

full-custom cell performance





AMchip07 layout

Digital simulation outlook

- Basic plan is continue using the UVM
  - Revisit the structure of the current software
  - Feedback experience we will gain in the AM07 characterisation
  - Scriptise and streamline things as much as possible
  - Study and understand the coverage of the validation (eventually) for AM2020