All Digital PLL

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Outline

1. All digital PLL architecture
   - Existing architectures
   - Proposed architecture and preliminary simulation results
2. Improvements - discussion
   - Improvements
   - Discussion

All digital PLL architecture

Existing architectures

PLL	Phase detector or comparator	Loop filter	Voltage Controlled Oscillator
Analog or linear PLL	Analog	Analog	Analog
Digital PLL	Digital	Analog	Analog
All Digital PLL	Digital	Digital	Digital

Table: Type of PLLs

Digital circuits are more efficient, flexible, and less noisy comparing to analog circuit

All digital PLL architecture

Existing architectures

- Phase detector
  - XOR
  - JK flip flop
  - 2 $\times$ D flip flop
- Time to digital converter
  - K counter
  - UP-DOWN Counter
- DCO
  - Includes DAC + Varactors
  - Simple divider
  - Delay line inverters

K.Lata and M.Kumar, *ALL Digital Phase-Locked Loop (ADPLL): A Survey*, IJFCC, December 2013

All digital PLL architecture

Proposed architecture

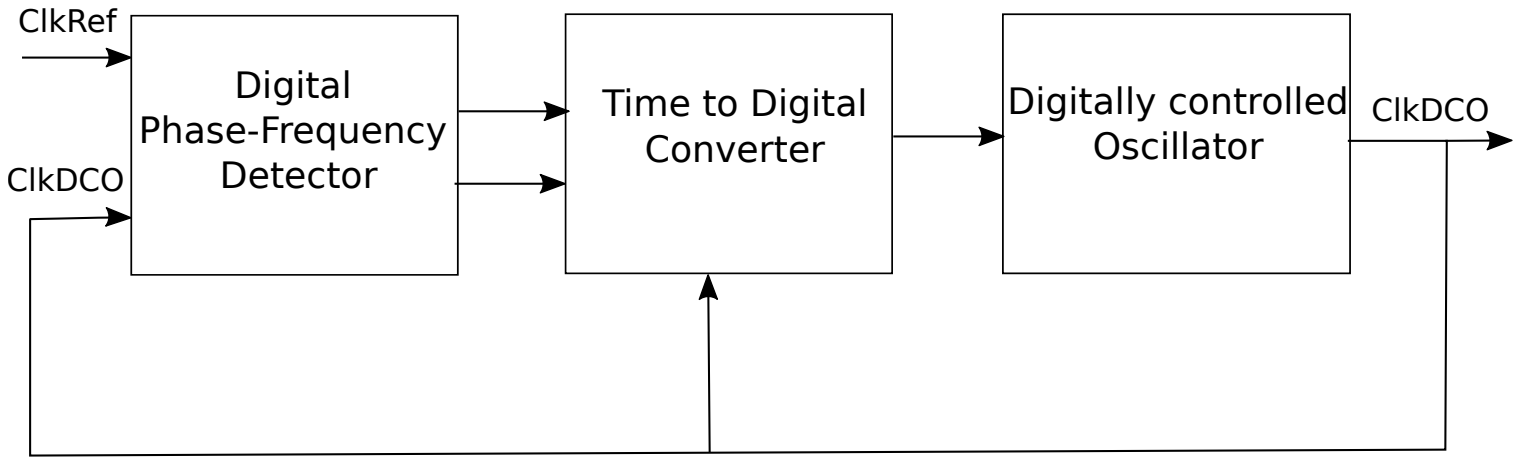

Figure: Proposed Architecture-ADPLL

Phase Frequency Detector

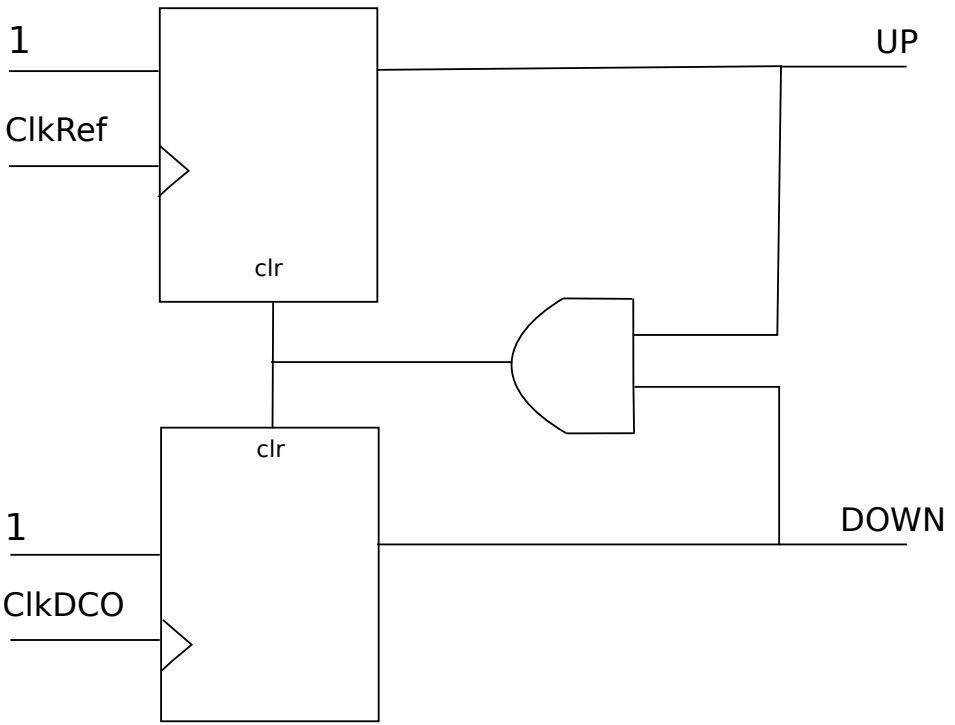

Figure: Phase Detector

Phase Frequency Detector

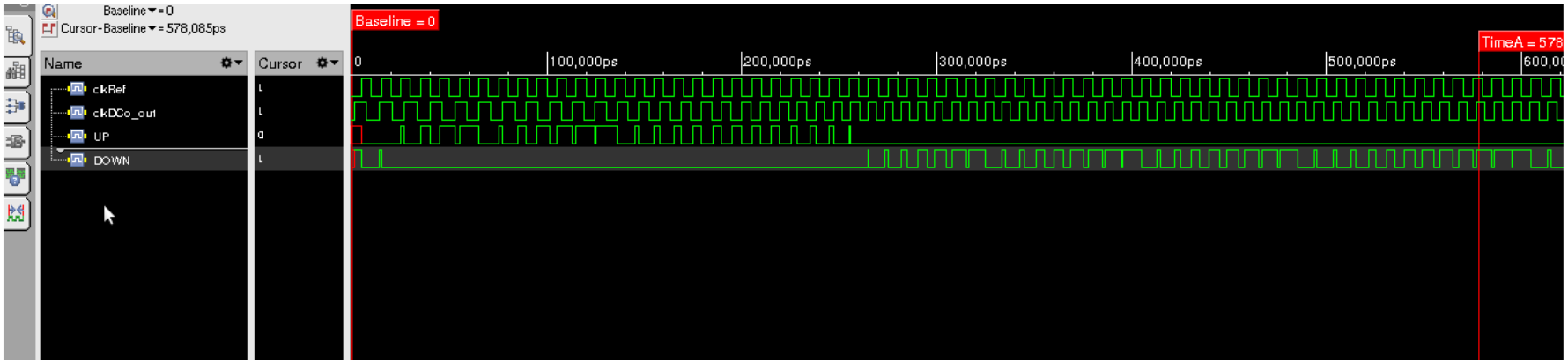

Figure: Phase Frequency Detector Simulation results

Time to Digital Converter

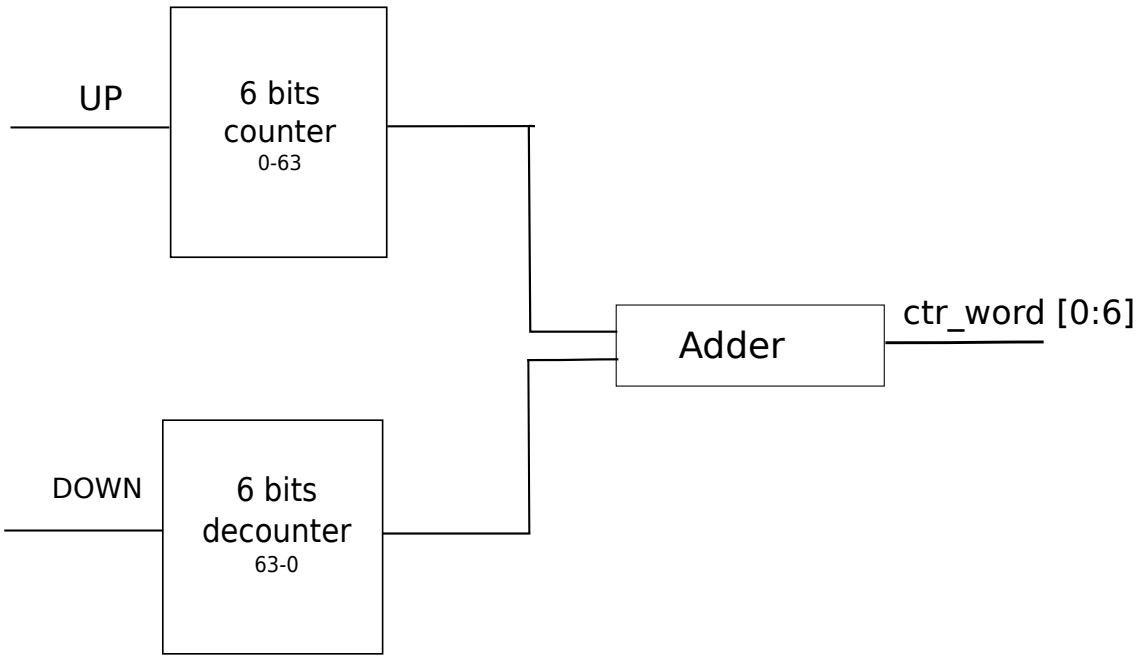

Figure: TDC architecture

All digital PLL architecture

Time to Digital Converter

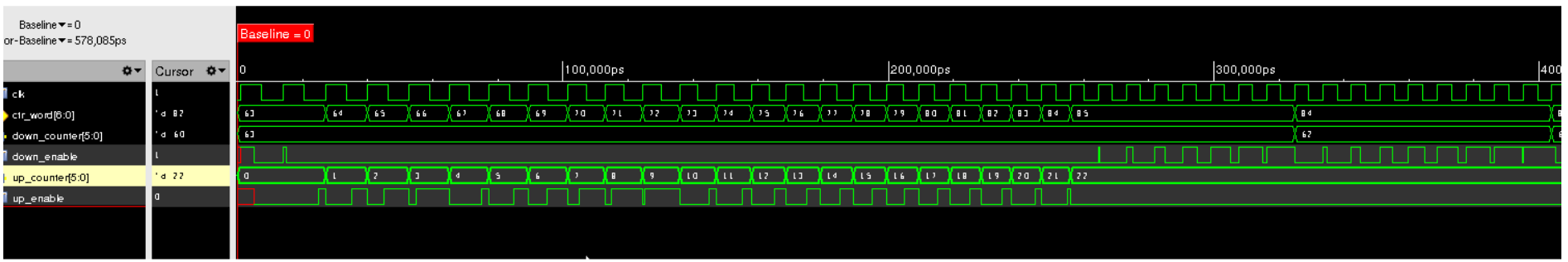

Figure: TDC simulation results

All digital PLL architecture

Digitally Controlled Oscillator - Dummy model

$DCOhalfperiod = invdelay * (128 - ctrword)$

Frequency range = [39Mhz-2,5GHz] for $invdelay = 0.1ns$

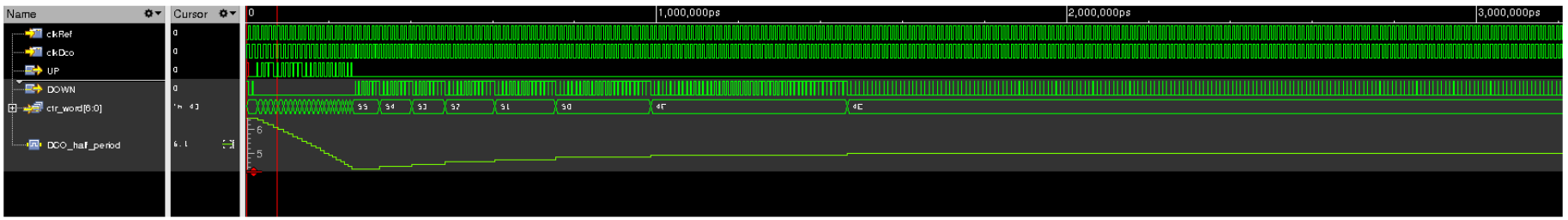

Figure: DCO Simulation Results

All digital PLL architecture

Preliminary simulation results

Example: for $f_{ref} = 100MHz$:

f_{DCO}=f_{ref} after $Locktime = 1,5ms$ with $\Delta T_{max} = 0,1ns$

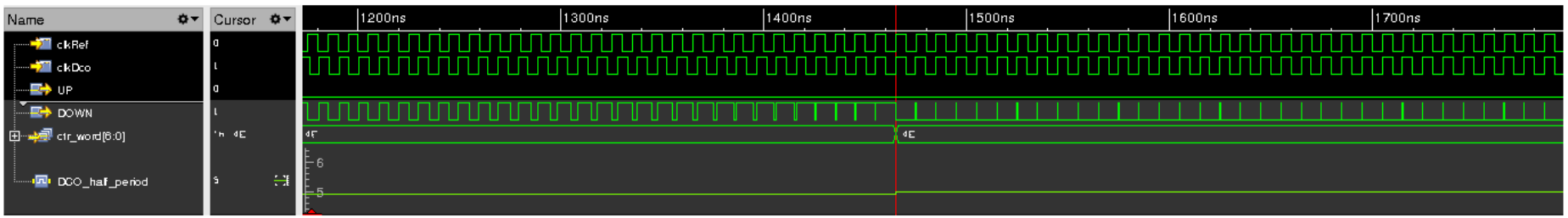

Figure: ADPLL Simulation results

ADPLL, frequency divider and Shift register

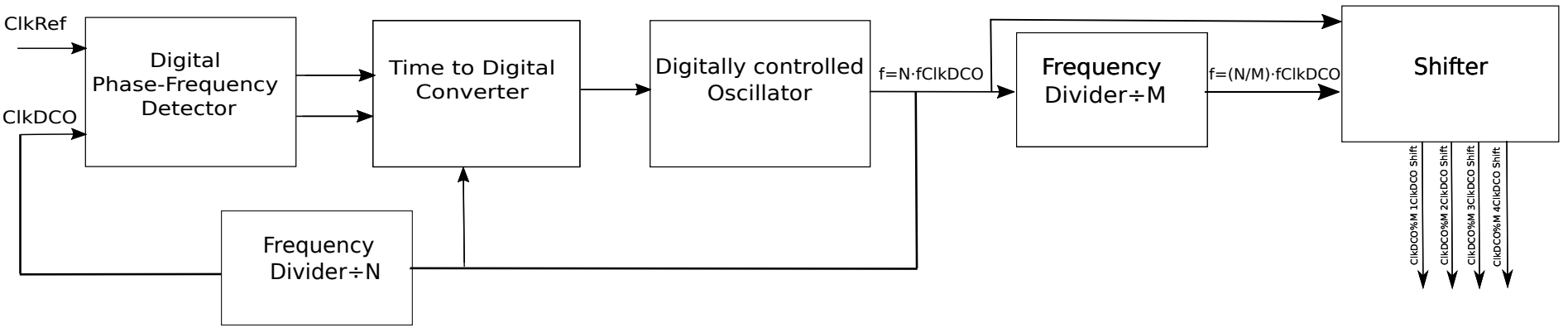

Figure: Different Clk generation - different delays

This could be a solution for a better power distribution

Improvements - Discussion

- Improvements
  - Add Filter
  - Analyse
    - Jitter
    - Lock time
    - Stability
    - Noise
- Discussion
  - Exact value and number of output frequencies?
  - DCO with Milano

Thank you for your attention