Highlights on Module Assembly and Testing

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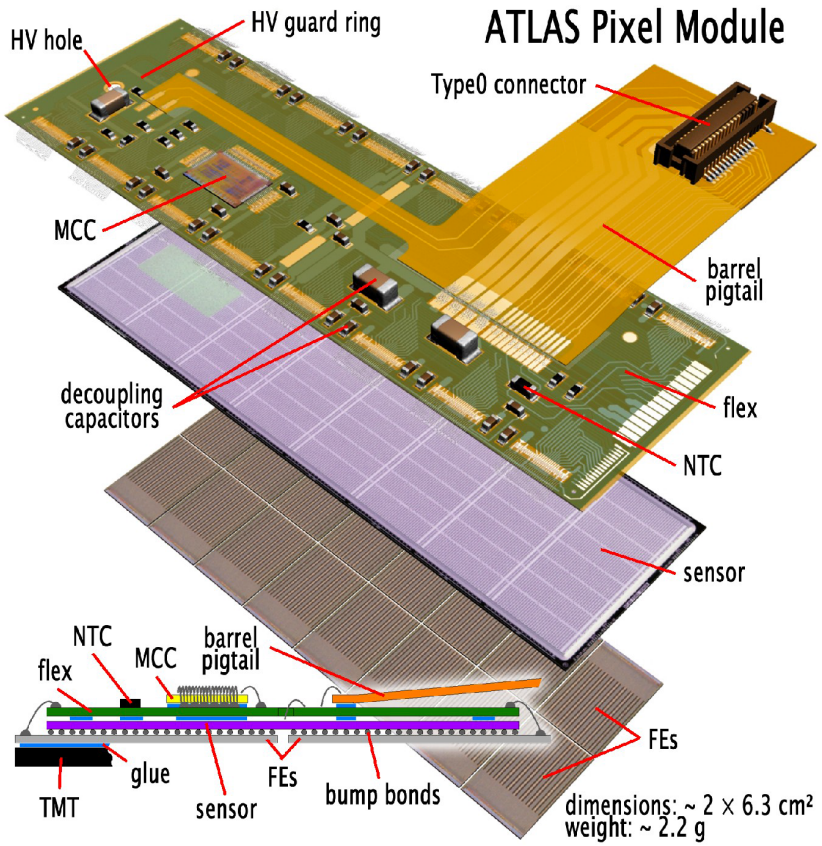
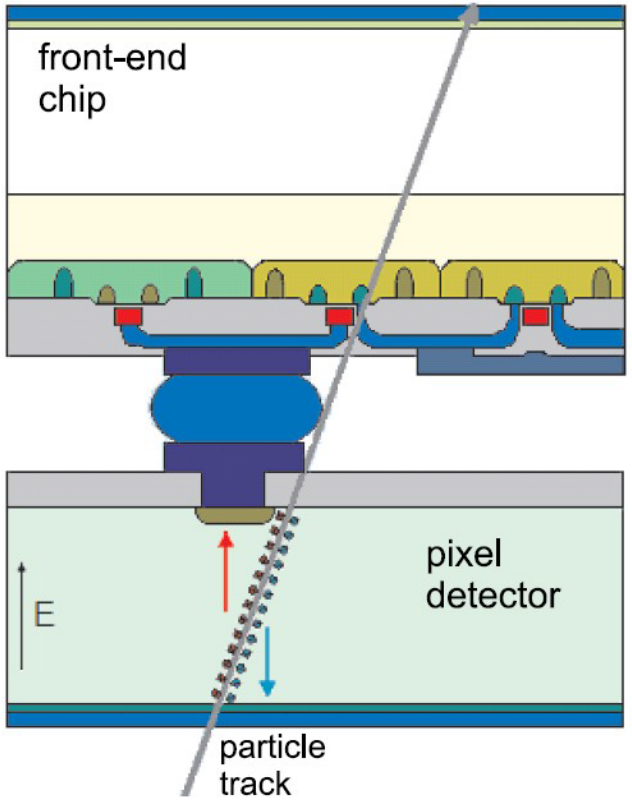
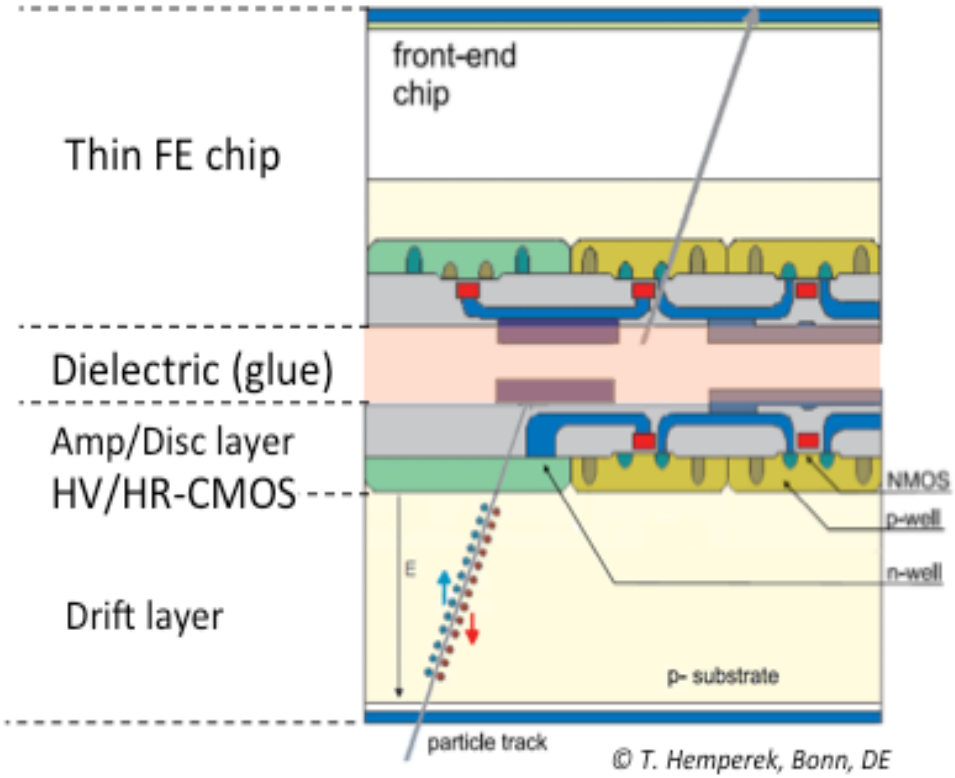
Itk Italia - 08-09 Feb 2017 - Genova

The Hybrid Module Concept





Bump-bonding



Glue-bonding

Assembly chain in a nutshell

Bare module assembly

Bump-Deposition (not for CMOS case) and thinning

Dicing

bonding between sensor and FE(s)

Laser release of glass substrate (Depending on used BB technique)

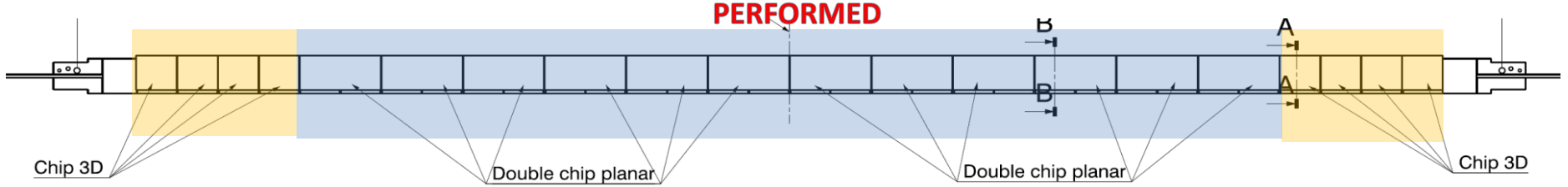
Module assembly and QA

Module dressing

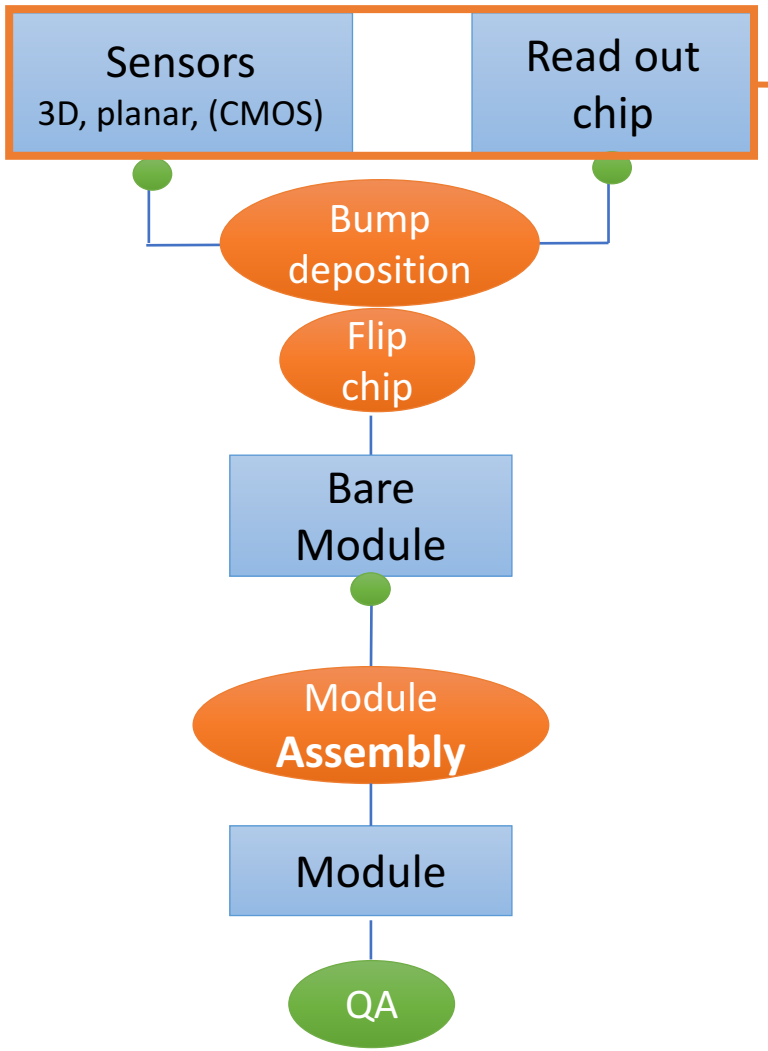
Wire bonding

Electrical QA, Termal Cycling and functionality test with ^{241}Am

In the IBL case, the qualified modules were shipped to the assembly site where the final stave assembly was performed

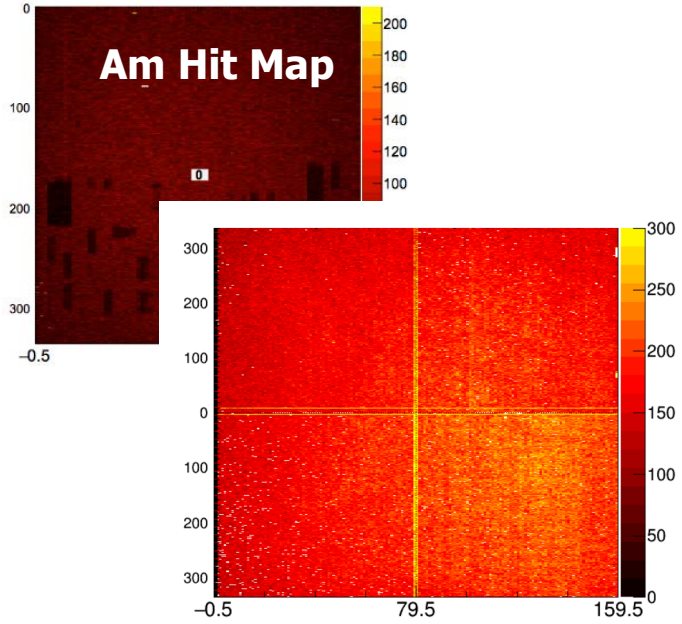


Sensors and FE electronics



Sensors

- 3Ds and Planars -> innermost layers
  - Planars for disks
- CMOS and/or Planars -> for other layers



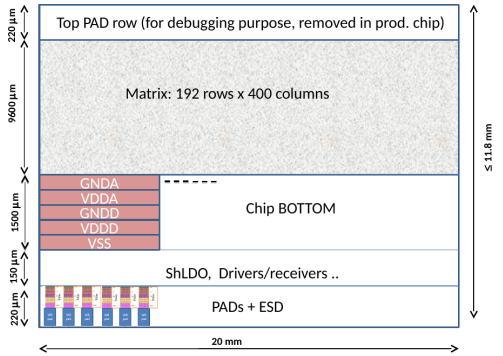
Readout chip

Two small 64x64 pixel matrix prototypes already finalized

- FE65-P2 (Received on Dec 2015)
- CHIPIX65 (Submitted July 2016)

Full scale demostrator

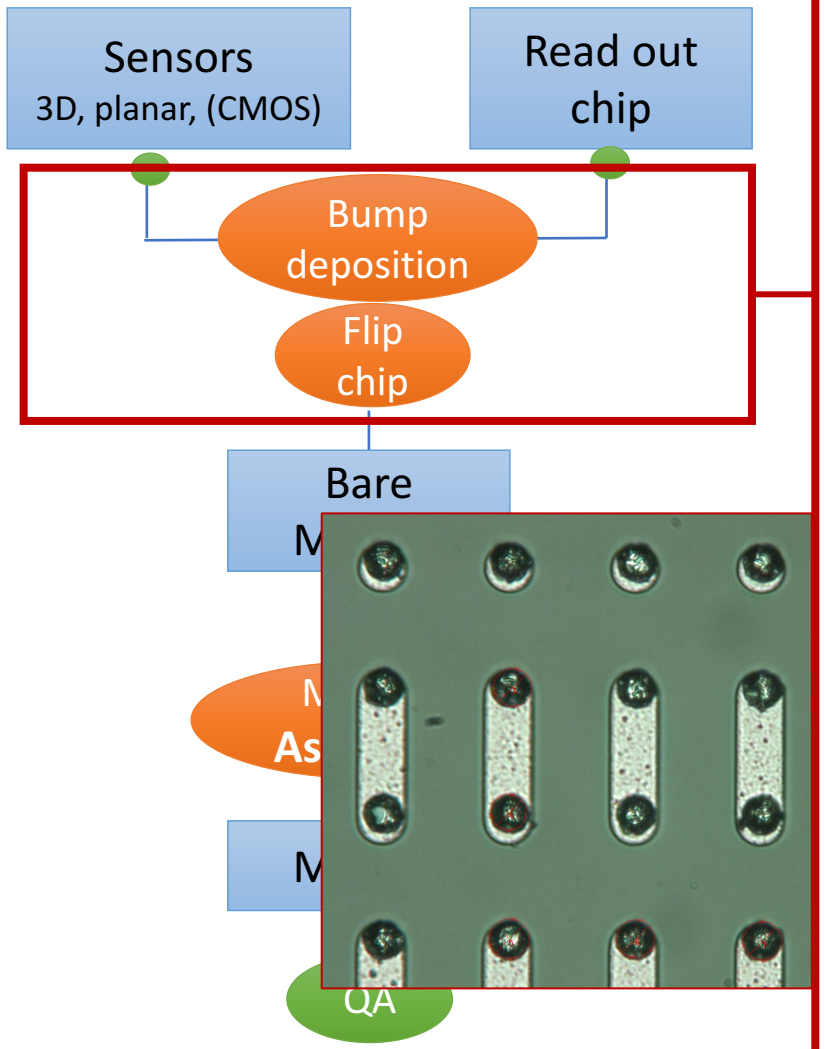
↳ **RD53A:** 20x11.8 mm^2 chip (400x192 pixels), 50x50 µm^2 pixel size (July 2017)



The demonstrator is not intented to be a the final production chip, but it will enable the prototyping of bump bonding assemblies with realistic sensors in new technology -> performance measuraments.

Specifications : http://cds.cern.ch/record/2113263

Hybridization Challenges



The new 65 nm front-end chip, being developed by RD53 Collaboration, will be compatible with **50 × 50 µm² or 25 × 100 µm² pixel size sensors.**

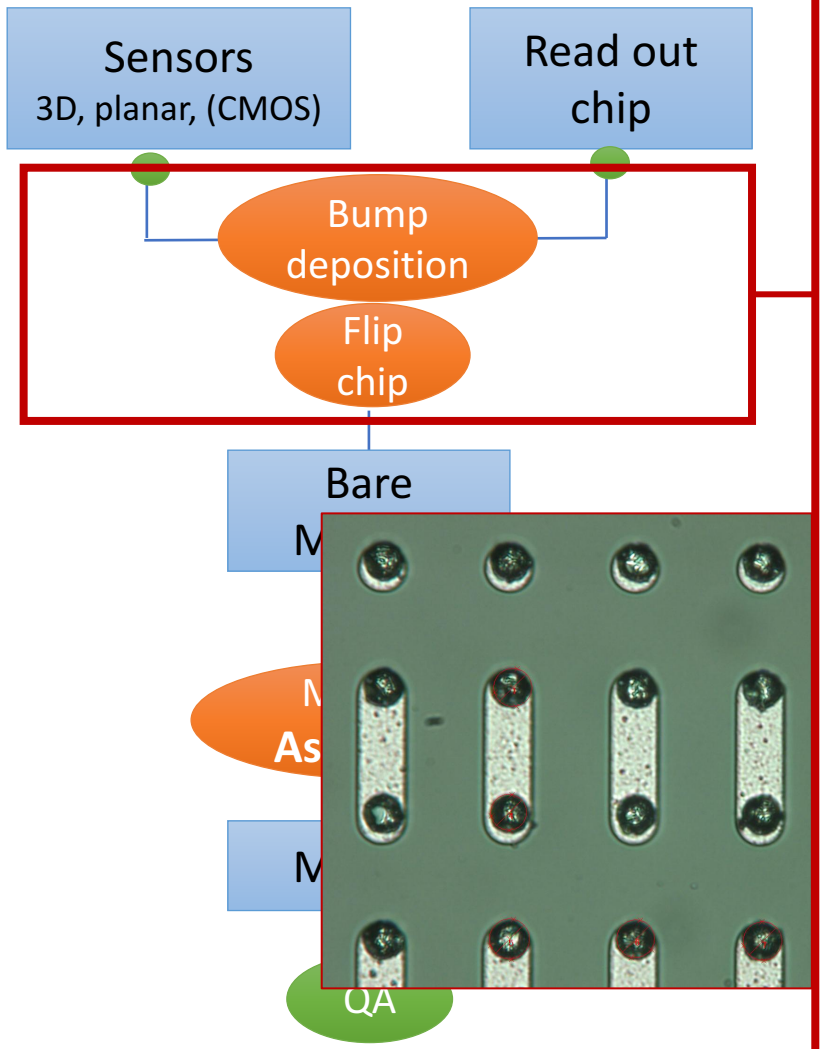
↳ The smaller pixel sizes imply up to 5x the bump density used in the current ATLAS Insertable B-Layer modules and consequently an order of **120 k pixels per FE-I4 size chip (2x2 cm²)**.

↳ Improving or developing hybridizations forms:
- High-Density Bump Bonding
- Capacitive couplings

Bump-Bonding at high density ($4 \cdot 10^4$ bumps/cm²) is a real productive effort:

- Optimize the process on dummies, studying bump height, size and the process parameters as pressure and temperature.
  - Visual, mechanical and electrical test of the parts and assemblies.
- Bump deposition on 12-inch electronics and 8-inch sensors wafers (was 8” and 6”)
  - Optimize the process on dummy supports
  - Wafers and deposition masks procured: test uniformity of bumps deposition.

Hybridization Challenges



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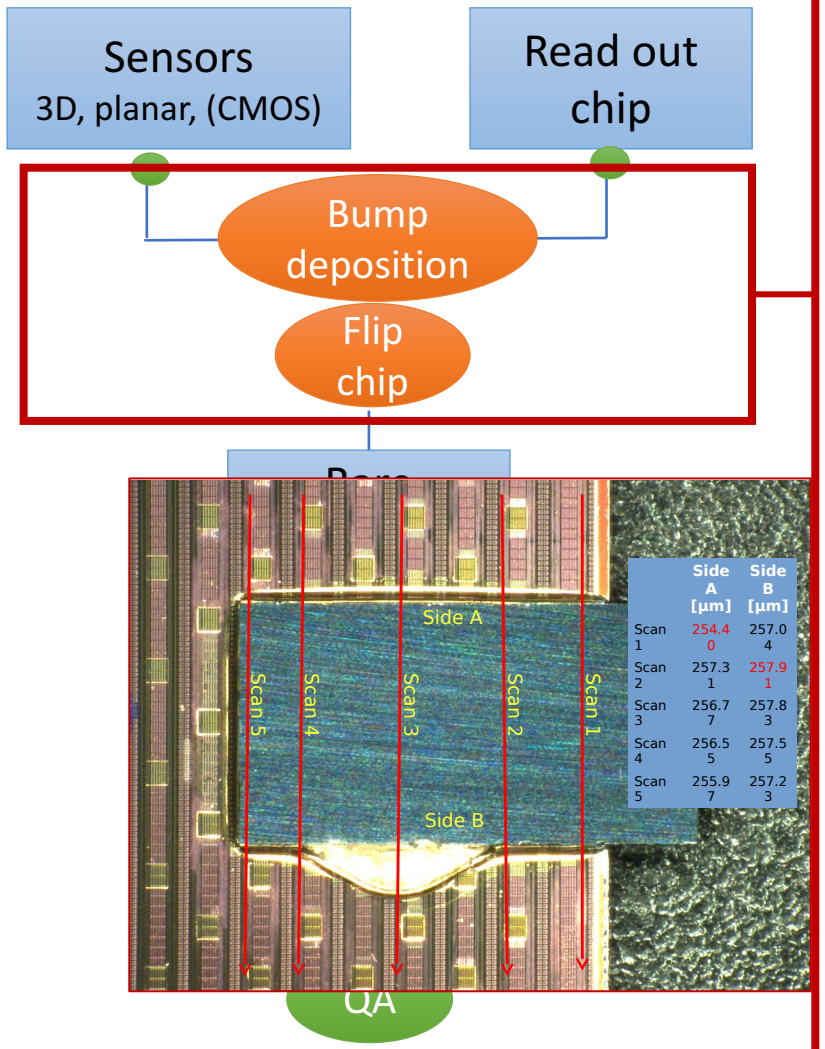
Bump-Bonding at high density ($4 \cdot 10^4$ bumps/cm²) is a real productive effort:

- Handling of thin electronics (100 µm has been achieved for few FEI4 test modules).
  - Indium bumps have an easier process that does not need temporary support wafer → competitive for innermost layers

We are working with Leonardo for the R&D phase and to qualify it as vendor.

Hybridization Challenges



	Side A [µm]	Side B [µm]
Scan 1	254.40	257.04
Scan 2	257.31	257.91
Scan 3	256.77	257.83
Scan 4	256.55	257.55
Scan 5	255.97	257.23

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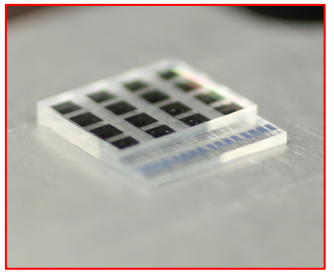
↳ Improving or developing hybridizations forms:

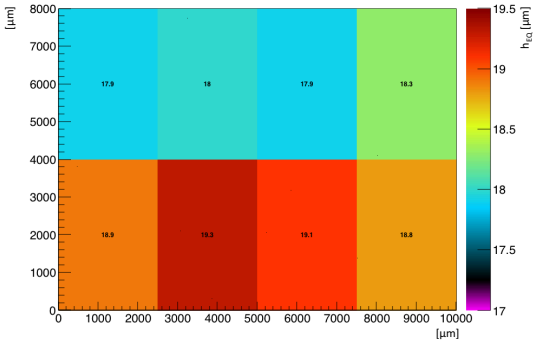
- High-Density Bump Bonding
- Capacitive couplings

Capacitive couplings could be a real good option to reduce cost and simplify the hybridization process

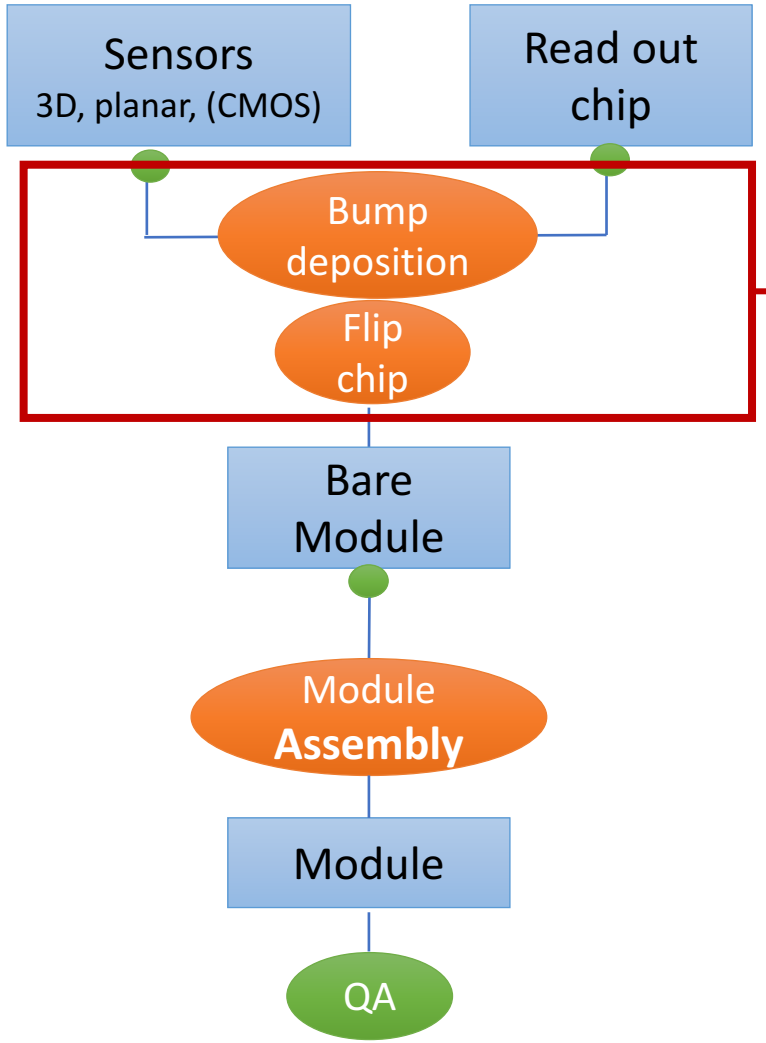
At the moment R&D is ongoing with the following requirements:

- Uniformity and repeatability of the process
- Evaluation of radiation tolerance of the coupling medium (typically glues)
- Evaluation of cost effectiveness
- Control of thickness the coupling medium and making of the spacers between the sensor and the FE

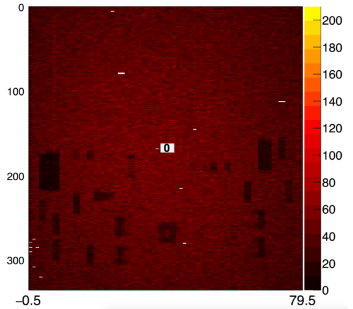




Bump-Bonding @ Leonardo



Bump bonded FBK 3D and planar sensors: <0.02% of unconnected bumps

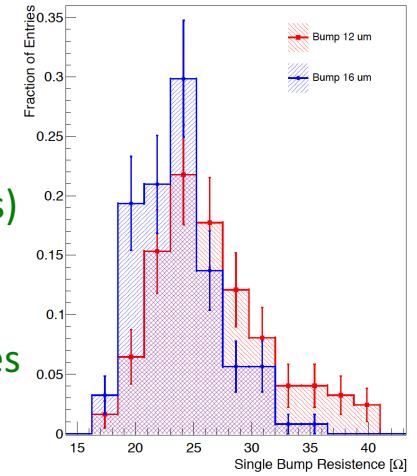


Source scan of a 3D sensor bump bonded to a +FEI4 by Leonardo

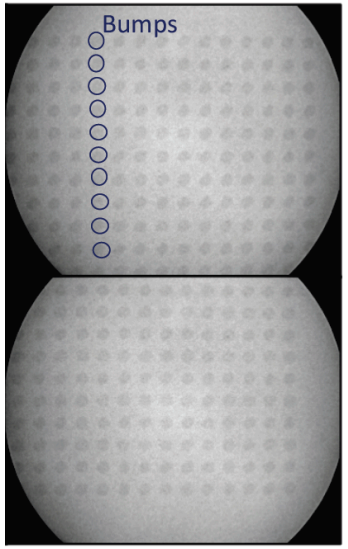
High bump density deposition (50x50 µm² over 2x2 cm²) validated with electrical and visual QA on 6" wafers with dummy chains.

Very promising results from first resistive chain tests on 6":

- Bumps resistivity as expected
- No open among 64k bumps (3 chips)
- No indication of shorts (either by X-rays or R measurement)
- Mechanical tests with thermal cycles on module-like structure are fine

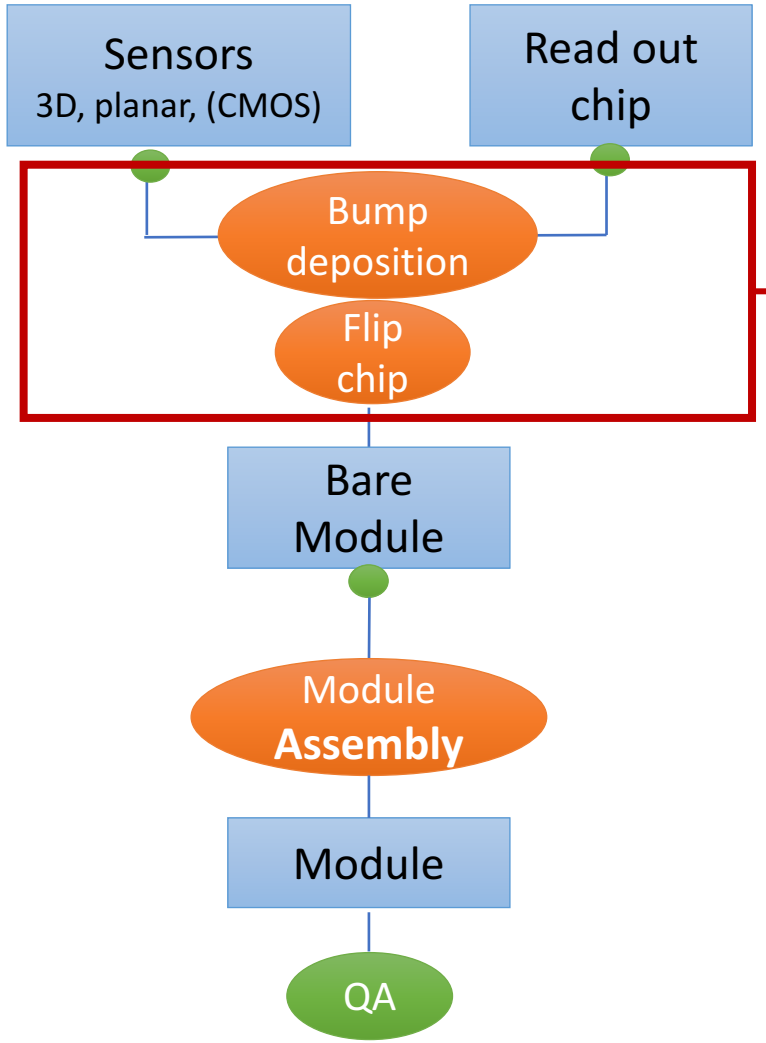


Bump R of dummy chains



High density Bumps X-ray

Bump-Bonding @ Leonardo



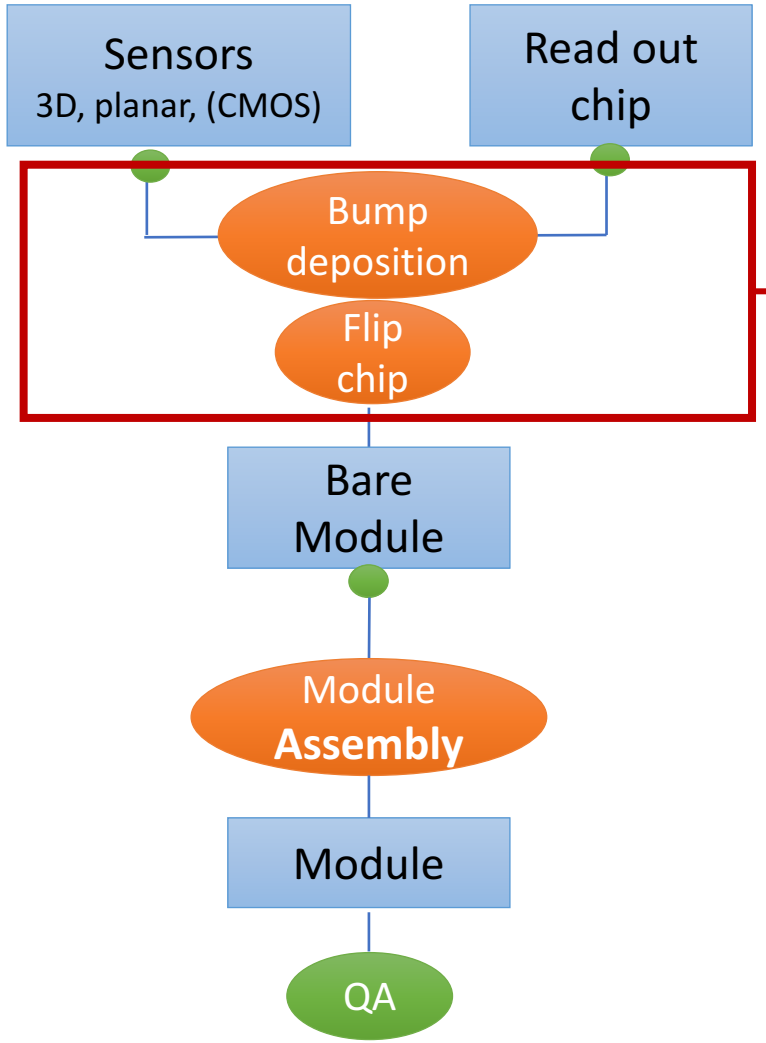
Bump deposition on 12” bare wafer (just Si, no pattern) with several bumps openings under test

- Wafer has been visually analyzed and bumps height measured with a profilometer
  - preliminary results on bump height (~10 μm) uniformity good (~1 μm) if opening is larger than 16 μm.
  - Some problems at the photoresist lift-off due to low number of bumps (bump density is nominal but only in spots uniformly distributed over the wafer surface).

Towards the TDR→ Qualify Leonardo as a BB vendor

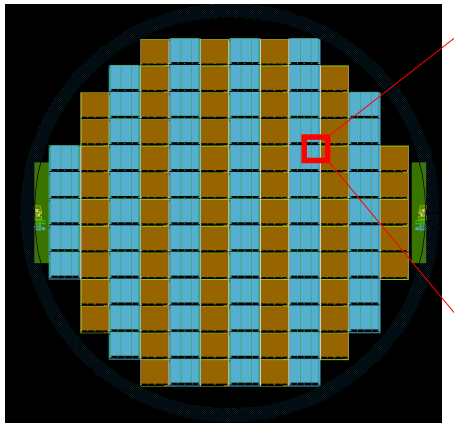
- **Next step is to deposit bumps on 12”** wafer with resistive chains. If successful to be used for RD53A wafer in Fall 2017
- For the TDR and beyond: Qualify Leonardo to do high density In bump deposition on 12” wafers and maybe part of the flip-chip.
  - Deposited wafers may be flip-chipped by users in the collaboration (BCN, Moscow, Glasgow, Geneva, etc...).

Bump-Bonding @ Leonardo

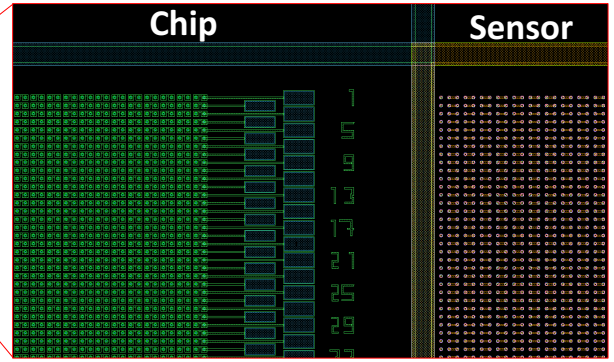


12” daisy chains:

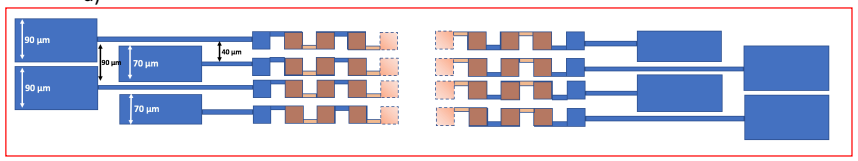
- More tests needed with high bumps density all over the wafer and daisy chains to measure bump resistivity.
- Resistive chains layout on 12” is a common layout for all the groups.
- In fabrication now→ BB in March



a)



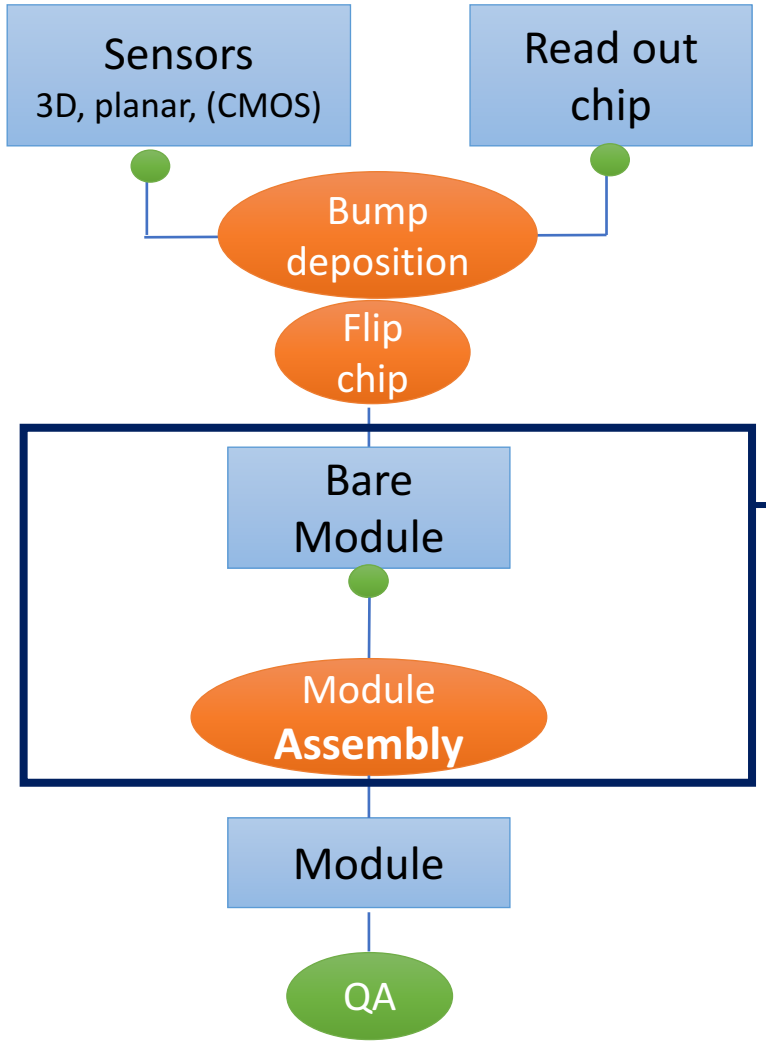
b)



c)

On the wafer are present 62 dummy chip and sensor tiles with a dimension of ~1.92 × 2.08 cm2 respectively. On each tile is present a pixel matrix of 400 × 336, close to the final RD53 FE pixel density

Assembly



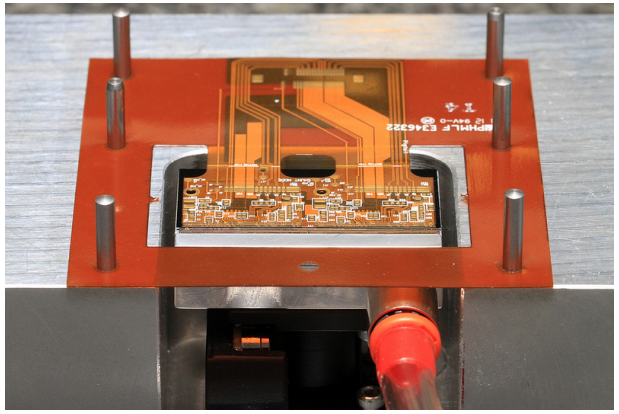
- Flex hybrid
  - Test w/ and w/o components
  - Cleaning
- Bare module
  - Sensor: IV Test
  - Readout: probe test @ bare (if needed)

It will difficult to have one unique assembly procedure, glues, etc… in the collaboration (differences also in with two assembly sites)

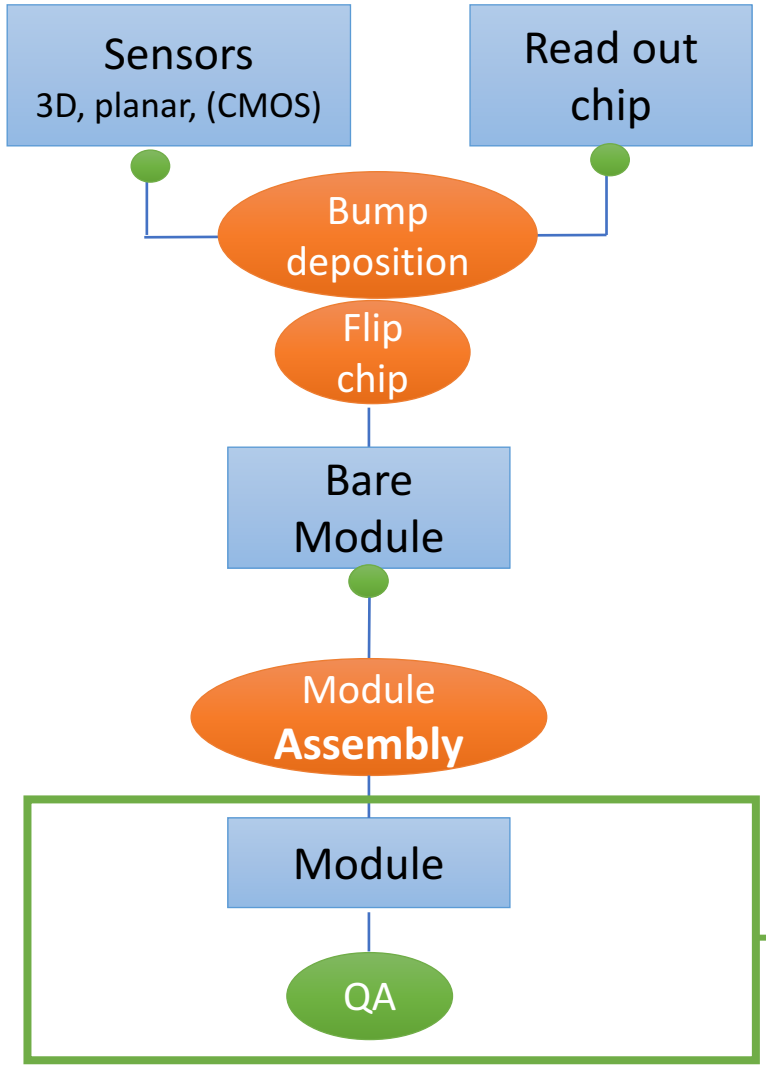
- However the procedure should be qualified
- Need to start now in the module group to give our contribution

Module Assembly:

1. Gluing flex to the bare module
   - Precise handling tools
2. Wirebonding
   - Wire bonder
3. Pull test
   - Pull tester
4. Quick QA test
   - Test setup
5. Potting



Quality Assurance



BARE

- **Preliminary electrical test after assembly - check if wire-bonds properly done.**

ASSY

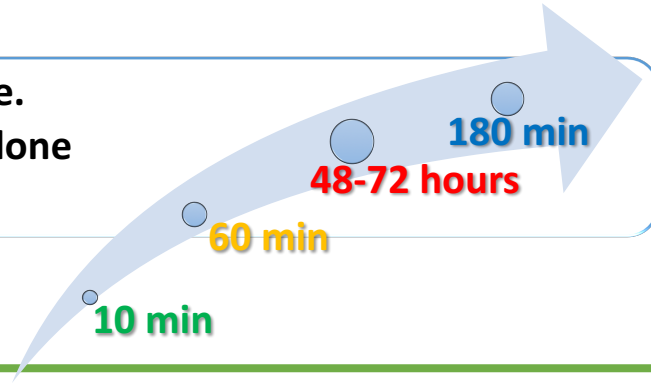
- **Electrical test at ambient temperature, in which is checked the proper basic functioning of the module (e.g. IV Curve, bumps connectivity with delta noise). Also done the Tuning at working point of 3ke$^-$ Threshold and 9BC @ 20ke$^-$**

BURN

- **Module is thermal cycling (-40, +40 °C for 2-3 days) and retested at ambient temperature.**

FLEX

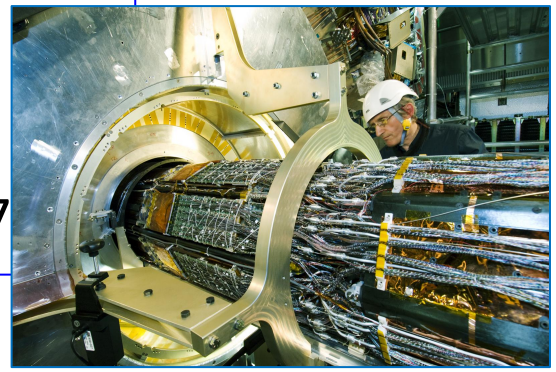
- **Complete calibration of the module.**
- **A functionality test with ^{241}Am is done**
- **All tests are executed at -10 °C.**

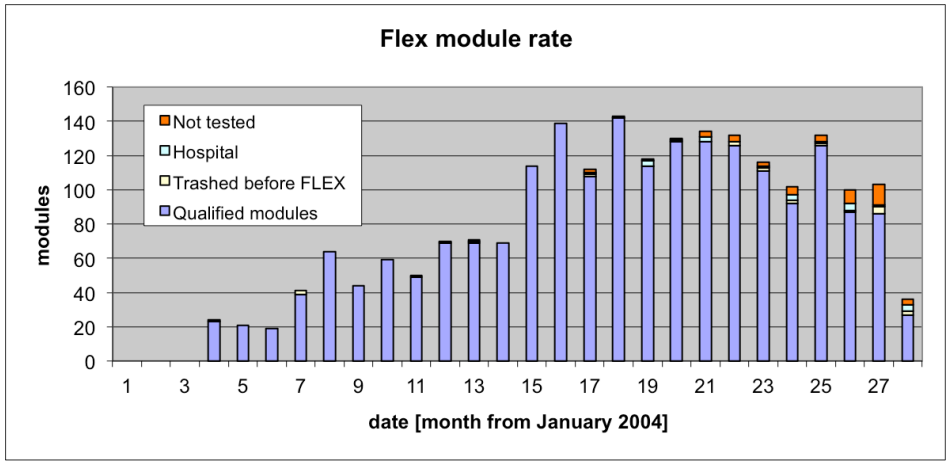


ATLAS Pixel Production Timescales

Pixel Detector

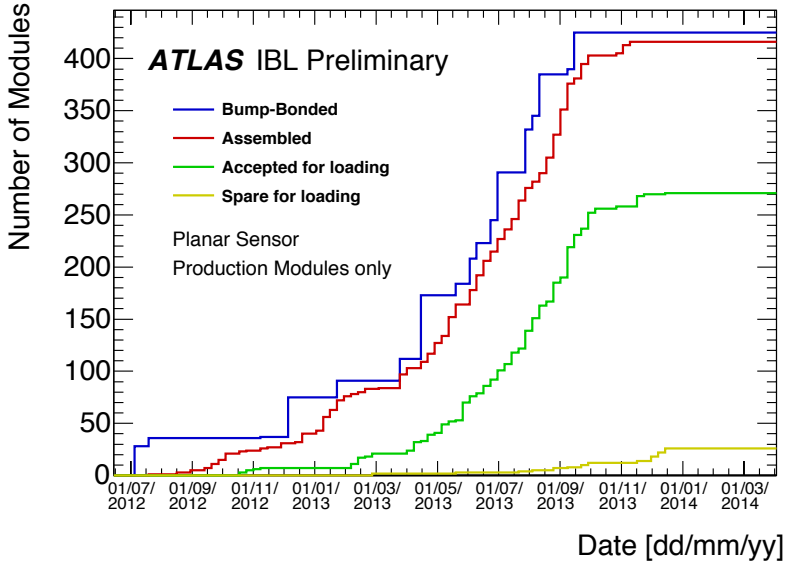
- Sites:
  - **3** Bare module QA sites
  - **5** Module Assembly sites
  - **5+1** Module QA sites
- Production peak:
  - 140 modules/month
- Paper: 2008 JINST 3 P07007





IBL Detector

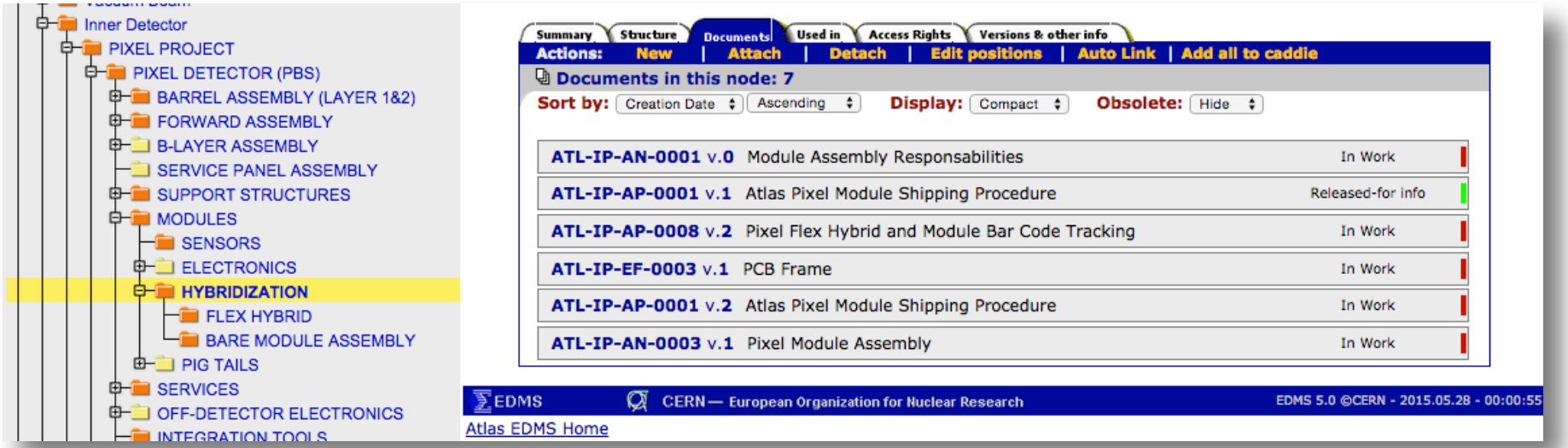
- ✓ Sites:
  - ***No Bare*** module QA
  - **2** Module Assembly sites
  - **2** Module QA sites
- ✓ Production peak:
  - 50 DC + 25 SC modules/month
- ✓ Jinst Paper in preparation.



Pixel Case: Lessons Learned-1

It profited by a large effort in organization:

- *Production database*: ready on day-1 and optimized during production according to user requests
- *Automatic QA* analysis and *storage of results* on database and web sites
- *Documentation* on EDMS for all procedures, items, etc…
- *Inter-calibration* of sites
- Large sharing and *optimization of resources* in order to keep the production rate always as high as possible.



Pixel Case: Lessons Learned-2

- Assuming a ‘standard’ QA
  - Preliminary tests at room temperature to validate the assembly
  - Thermal cycles without power
    - Long burn-in for few modules in devoted sites
  - Long and full qualification at operational temperature → Focus on tests that may detect subtle misbehaving.

- A priority is to have a lab test setup that allows parallel testing! This has been in the past experiences the main bottleneck in the QA.
  - In the Pixel production we started with the TPCC-TPLL for one module operation.
  - The hardware and the software grown around it with SURFs card to be able to power and clock modules simultaneously and to test them sequentially up to 16 modules.
  - Not really ideal: Data test was possible only sequentially and connection was a bit tricky and not very reliable, mainly during integration in SR1.
  - In IBL production we started with the USBPix, born for one FE operation.
  - As for Pixel, hardware and software grown to test up to 4 DC modules sequentially.
  - Setup not ideal, mainly for DC some reliability problems.
  - A much more optimized system was the RCE, able to test 16 FEs in parallel, used for test during stave QA and integration.

Conclusions

- Planning for a setup well in advance properly defining the list of requirements.
  - Foresee compliance, it will be useful!
- Plan for documentation.
- Plan for all the software tools that make the QA as automatic as possible.
- Qualify more labs to contribute, and explore industrial assembly and QA.