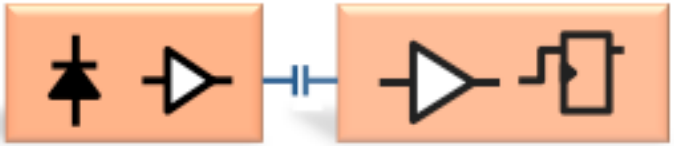


HVR - CCPD

# Stato e prospettive HVCMOS

**ATLAS ITk Italia, 08/02/2017**

**Attilio Andreazza**, M. Citterio, V. Liberali, F. Ragusa
INFN Milano

G. Darbo, G. Gariano, A. Gaudiello, C. Gemme, L. Rossi, E. Ruscino - INFN Genova

C. Sbarra, A. Sidoti – INFN Bologna

G. Chiodini – INFN Lecce.

# ITk CMOS Pixel Effort

- Collaborative effort of ~25 ATLAS ITK institutes
- Capable of attracting also non-ATLAS institutes and resources

# ITk CMOS Pixel Effort

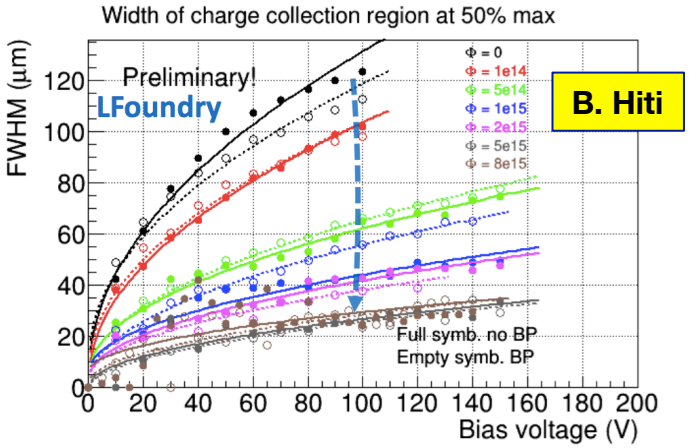
- CMOS detectors may provide:
  - **better granularity**: pixel decoding or small pitch monolithic
  - **reduction in material**: especially for monolithic solutions
  - **fast production turnaround**: commercial process
  - **simplification of the assembly and QA process**: viable solutions that do not require bump-bonding
- R&D effort till now covered a wide range of options:
  - many foundries and high-voltage or high-resistivity processes have been investigated
  - hybrid solutions using both bump-bonding and capacitive coupling (CCPD):
    - passive sensors
    - pixel encoding
    - both digital and analog signals
  - full monolithic approach

- **HV-CMOS**
  - **AMS 350 nm**
  - **AMS 180 nm**
  - STM 180 nm
- **HR-CMOS**
  - **LFoundry 150 nm**
  - Global Foundry 130 nm
  - ESPROS 150 nm
  - Toshiba 130 nm
  - **TowerJazz 180 nm**
  - IBM T3 130 nm
  - ON Semiconductor 180 nm
- **SOI – CMOS Pixel**
  - XFAB 180 nm

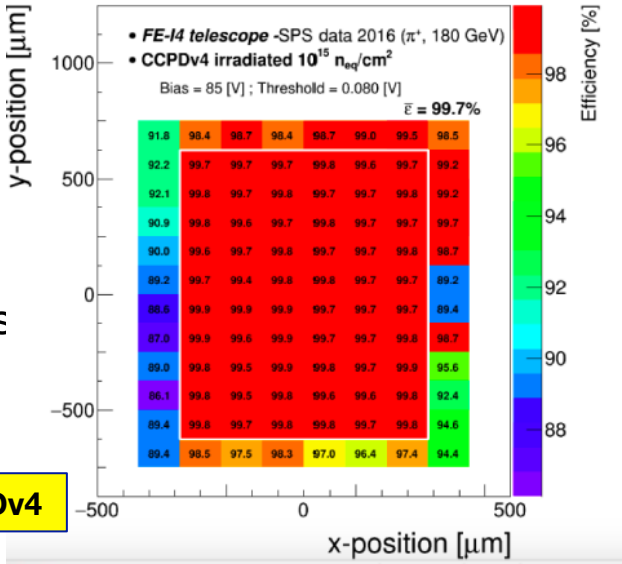
# ITk CMOS Pixel Effort

## R&D effort covering a wide range of options.

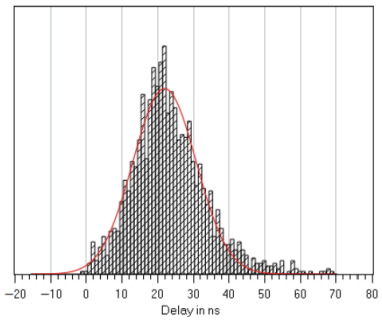
Sensor radiation hardness above $10^{15}$ $n_{eq}/cm^2$



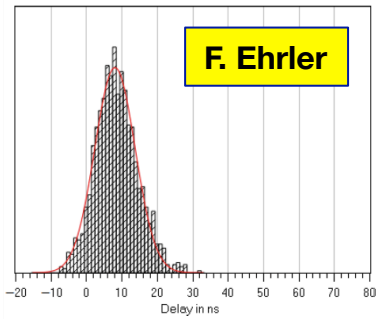

Assembled CCPD devices with high efficiency



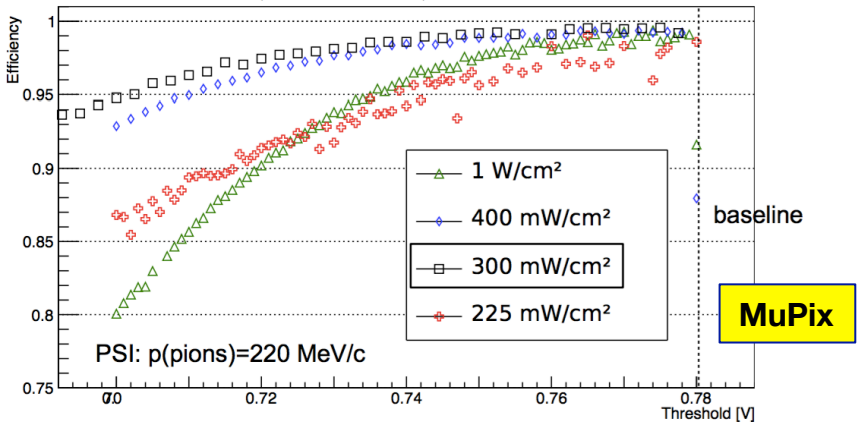

Handles to improve timing performance




Threshold = 50 mV
Ø Delay = 22 ns
σ Delay = 8.8 ns




Th 1 = 20 mV
Th 2 = 50 mV
Ø Delay = 8.2 ns
σ Delay = 5.8 ns



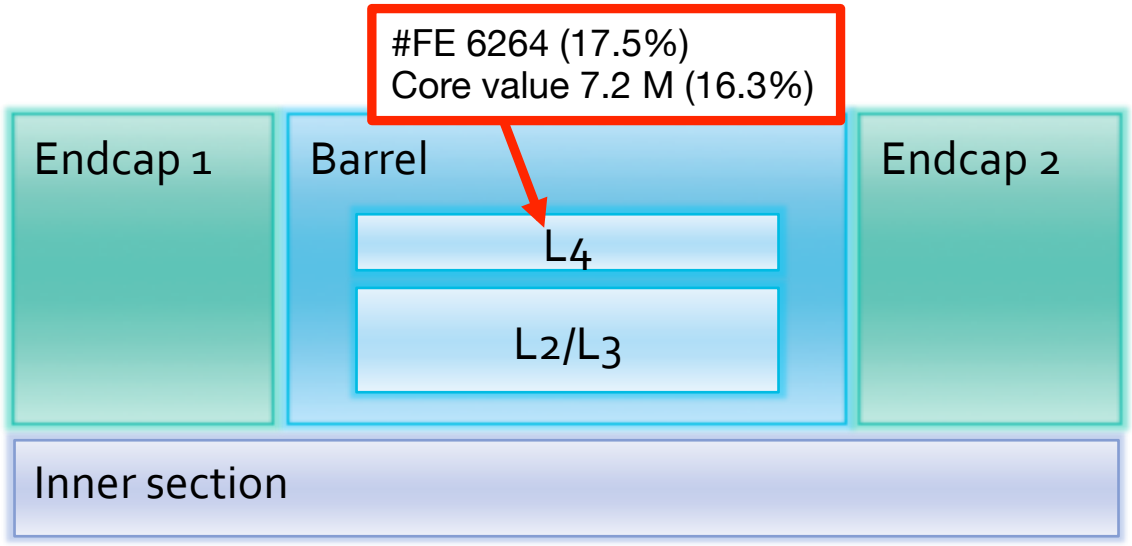

Monolithic architectures have been realized

# CMOS Project

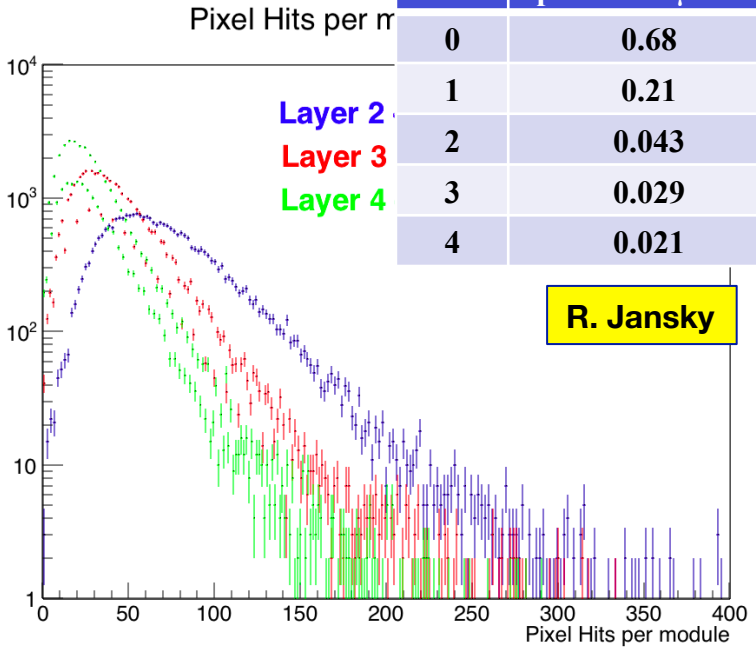
- ITK Performance with (Pixel) CMOS sensors
  - Study CMOS sensors in ITK layout for potential in performance gain
  - Establish requirements for sensors & electronics
  - Study “practical” benefits (low power, no bump-bondig, gain in production contingency and savings in personpower)
- Develop CMOS sensors adequate for ATLAS operation
  - **Completing the development phase** (until mid 2017):
    - evaluation of sensors already prepared during 2016/early 2017
    - optimization of specific designs on front-end and digital architecture
    - test results at the chip and module level as input to the ITK Pixel TDR
  - **Engineering phase** (mid 2017—2018):
    - focus on optimal choice of designs
    - engineering towards system-ready implementation
    - sharing the design load (“designer taskforce”)
    - testing of chips and modules (“test and qualification working group”)
- System Integration of CMOS sensors modules in the ITK baseline system
  - Demonstrate assembly and QA of “drop-in” modules compatible with mechanical, thermal and electrical ITK Pixel system design

# Design goal

- **Monolithic CMOS detector will be the most profitable option for ATLAS**
  - clear reduction of material, simplification of assembly, potential reduction of power consumption
- Candidate application is for the **outermost pixel layer**
  - largest area layer, where practical benefits are outstanding
  - reducing pressure on bump bonding and simplifying the assembly, it provides contingency to the whole pixel project
  - radiation level and data rates comparable with current IBL/L0: compatible with integration level provided by HR/HV technologies, in the 130-180 nm range.




| Layer | Hit rate /mm² per BC at μ=200 |
|---|---|
| 0 | 0.68 |
| 1 | 0.21 |
| 2 | 0.043 |
| 3 | 0.029 |
| 4 | 0.021 |



# Lankford review recommendations

- Assess quantitatively the impact on ATLAS of the potential advantages of the CMOS option in the context of the baseline pixel project schedule and cost estimate. Complete this assessment no later than end of May 2017.
- Define intermediate milestones in the development of a CMOS pixel module. Use these milestones as breakpoints in the consideration of a CMOS option. Redirect effort from CMOS to the baseline pixel development if a CMOS breakpoint-milestone is not met.
- Develop a detailed schedule for the CMOS option no later than the next ATLAS Upgrade Week in March 2017.
- Include in the TDR the approach to an eventual procurement of a CMOS design in production quantities

# Milestones

- **TDR 2017**
  - choice of analog cell design and readout architecture
- **End of 2017**
  - submission of full-scale common design
    - enough features to assess detector performance on a device with size compatible with RD53 chip
    - qualification of module concept
- **Mid 2018**
  - demonstration of module design
    - quad size, “drop-in” compatibility requirement
- **End of 2018**
  - system-ready chip submission
    - full feature chip, suitable for preproduction

**Q1 2017 - Spec Review**
preliminary specification document available and attached to the agenda

**Q4 2017 – PDR**

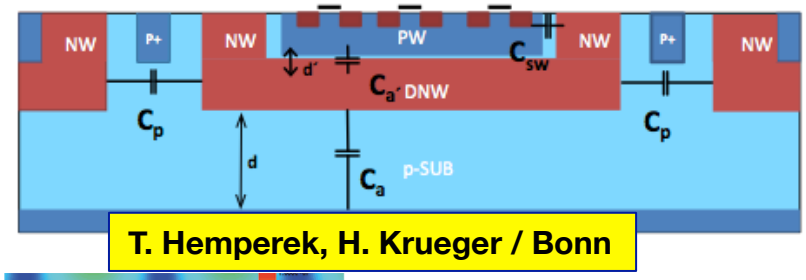
**Q3 2018 – FDR**

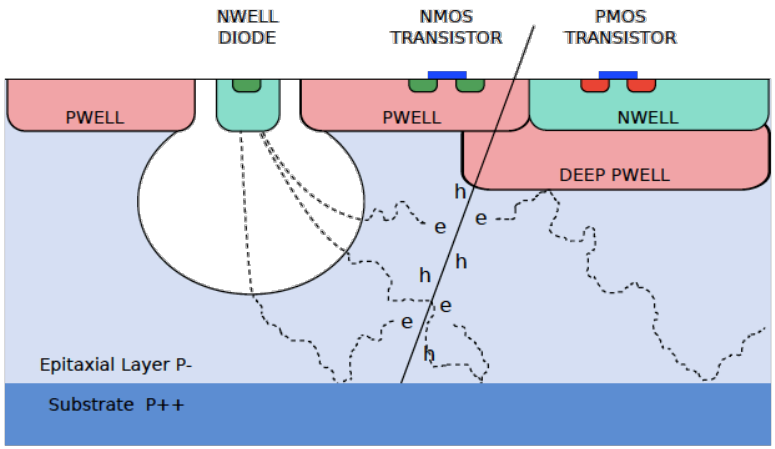
**Q2 2020 – PRR**

# Technology options: 1) analog cell

- Large fill factor
  - Uniform charge collection
  - Large capacitance (~50 fF) on charge sensitive amplifier
  - More power necessary to achieve fast signals with reasonable amplitude

- Small fill factor
  - Higher gain and faster response due to smaller capacitance (2-5 fF) and higher *Q*/*C*
  - Potentially lower power consumption
  - Signal collection under deep p-well after irradiation more difficult on edges



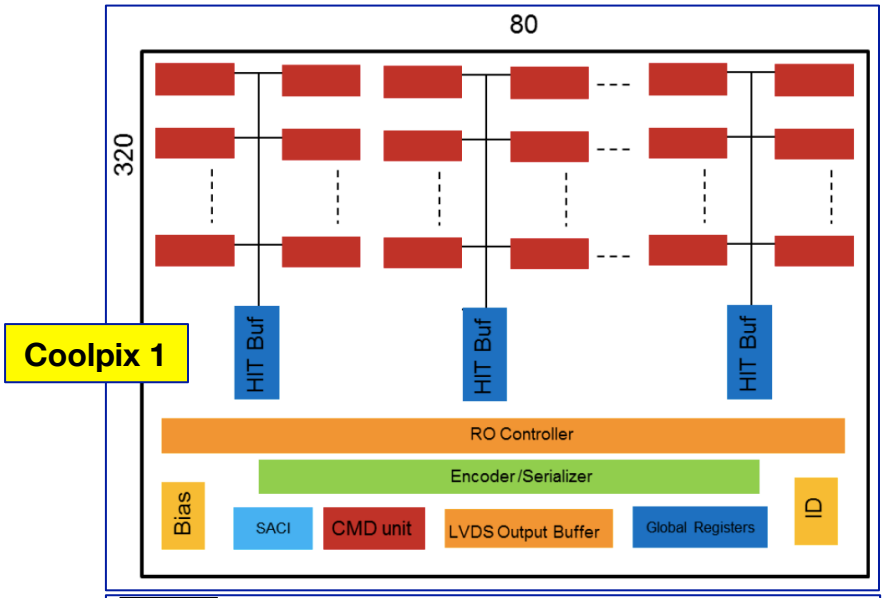



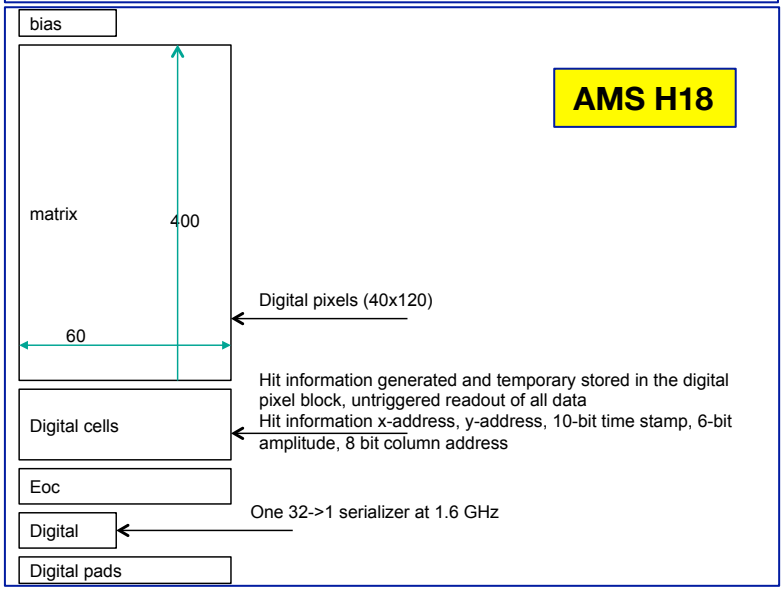

Schematic cross-section of CMOS pixel sensor (*ALICE ITS Upgrade TDR*)

# Technology options: 2) readout architecture

Two main concepts for pixel matrix readout with ATLAS ITK specs for outer layers:

1. Column drain architecture
   - Token distribution through column, synchronous readout of pixel buffers
   - Include hit buffering (leading edge, trailing edge) in pixel
   - Two main submissions prepared: L-Foundry MonoPix1 and Coolpix1, AMS H18
2. Asynchronous hit direct to periphery
   - Comparator output directly to periphery
   - Buffering and time-stamp at periphery
   - Two submissions in preparation: AMS H18 and TowerJazz 180



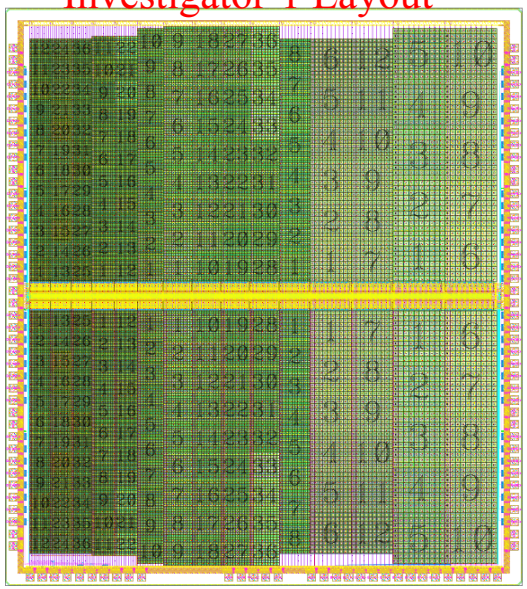



# Technological choices: process

## TowerJazz

- Subm. in **??? 2017**
- Two large scale demon-strators based on ALPIDE like front-end:
  - Asynchronous matrix readout (no clock distribution over the matrix)
  - Column Drain Read-Out (based on Monopix)

Investigator-1 Layout

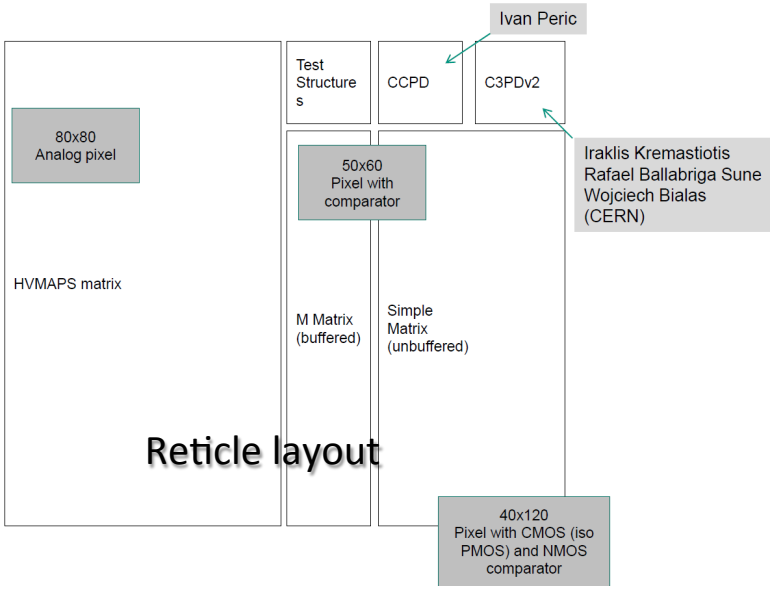


5.0 mm x 5.7 mm

## AMS H180

Mu3E + ATLAS (monolithic)

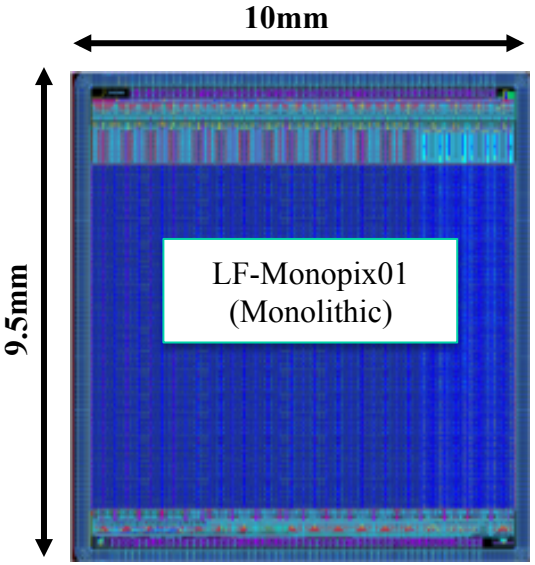
- Subm. in **Nov. 2016**
- Additional production step – isolated PMOS
- 80 and 200 Ohm.cm wafers
- Reticle Size about 21mm x 23mm

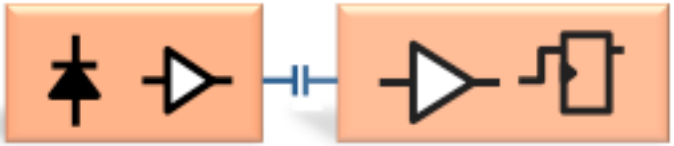



## LFoundry

Monopix01 and Coolpix1

- Subm. in **Aug. 2016**
- "Demonstrator size"
- 50 x 250 μm² pixels
- Fast standalone R/O





HVR - CCPD

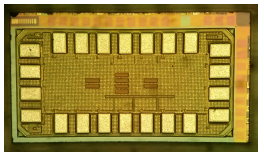
# ATTIVITÀ ITALIANE

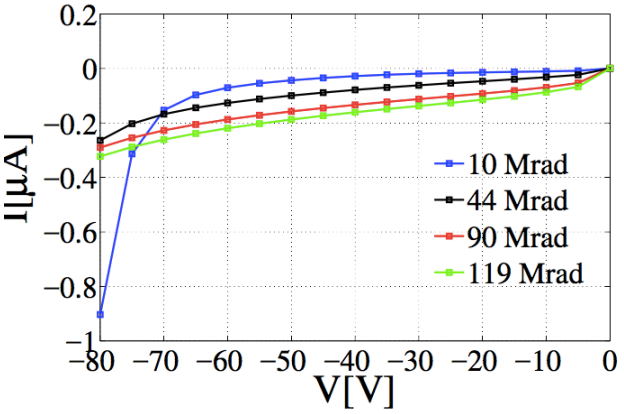
# Introduzione

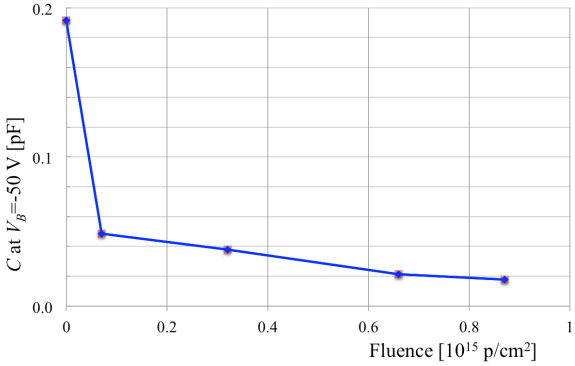
- HVR_CCPD è iniziato con due obiettivi:
  - sviluppare sensori con STMicroelectronics
    - Processo BCD8 con caratteristiche specifiche rispetto agli altri competitori
  - controllo del processo di ibridizzazione
    - spaziatori per controllare lo spessore della colla

- Gli sviluppi in ATLAS stanno volgendo verso un altro aspetto, molto più stimolante:
  - Portare a conclusione le attività in atto
  - Entrare nella caratterizzazione dei dispositivi monolitici
  - Integrarsi nell'R&D di ATLAS

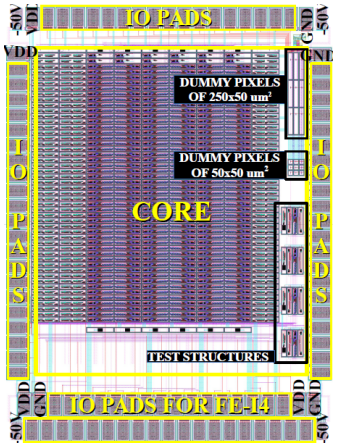
- KC53A
  - utilizzato per la caratterizzazione della parte di sensore
  - irraggiamento con protoni: aumento della zona di svuotamento con l'irraggiamento
  - Rivelatori irraggiati con n da $2\times10^{14}$ a $5\times10^{15}$ n/cm$^2$
  - **Organizzare e-TCT e testbeam**

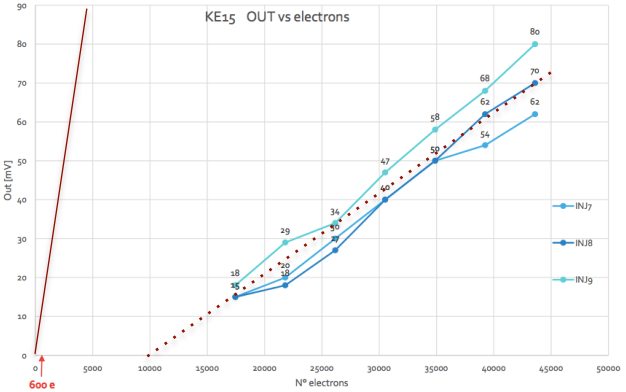





- KE15A
  - matrice ibridizzabile a FE-I4
  - design aveva passato tutti i test di simulazione
  - prime misura mostrano un comportamento insoddisfacente dell'amplificatore
  - **Simulazione con parassiti**
  - **Setup di test standalone**

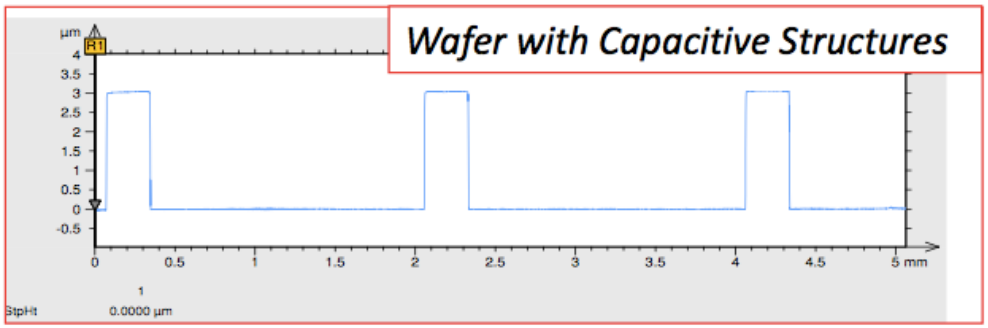


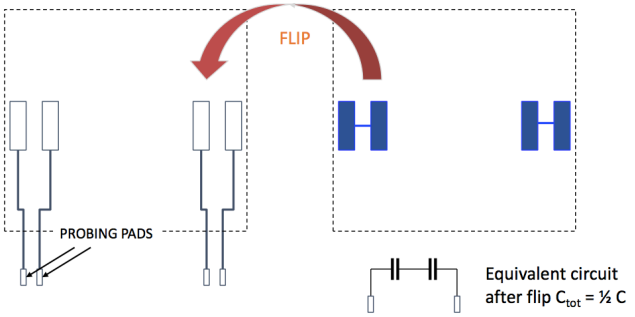

- Se capiti i difetti, un ultimo run:
  - **Solo pixel di test, versione full CMOS e e con amplificatore bipolare** misura unica

# Ibridizzazione

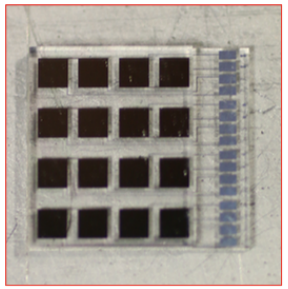
- Caratterizzazione del processo di ibridiz-zazione con spaziatura controllata.
- Dummy per misura della capacità:
  - primo lotto su wafer a bassa resistività: uniformità dell'altezza dei pilastri <0.1 µm
  - nuovo lotto su substrato di quarzo: 1 wafer già consegnato (senza spacer), altri due wafer ordinati con pillar di 3 µm e 6 µm
  - Primi test con colle:
    - Arclad 5913 – tape, 25 µm thick – uniformità <1 µm
    - Araldite 2011, 2020 and Masterbond – uniformità ~5 µm
      - Masterbond is a dual cure epoxy based system which offers a primary cure utilizing UV light (365 nm) along with a secondary a secondary heat curing mechanism (80 C)
- Processo di qualifica:
  - misure di resistenza meccanica e capacità
  - cicli termici
  - irraggiamento
  - deposizione su wafer FE-I4
  - ibridizzazione di dimostratori LFoundry e AMS

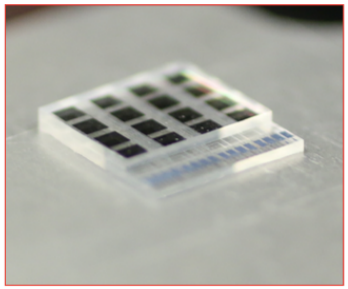



**Mean from Profilometer 3.05 +/- 0.06 µm**




$$h_{eq} = d = \varepsilon_0 \varepsilon_r \frac{S}{2C_{meas}}$$



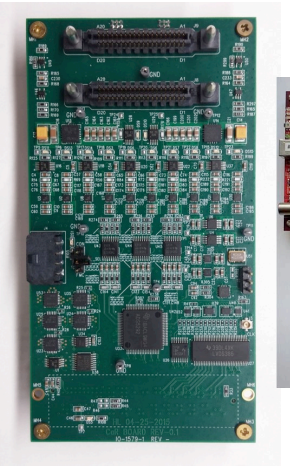


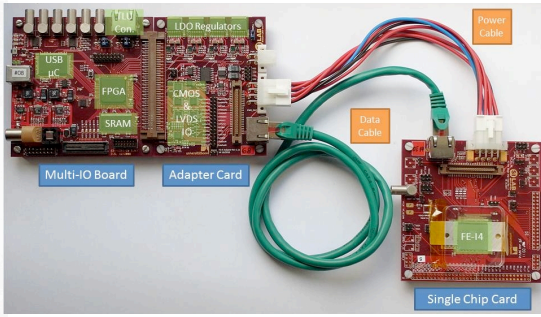
# Developments in ATLAS: Design

- Difficult to contribute to design effort:
  - many technologies still on the market and decisions will not be taken soon
  - cannot spread manpower on different development kits
  - no strong intellectual properties that can be contributed
    - SEU resistant memory cell and combinational logic (developed within RD53)
    - Pending validation on TSMC

- Some competence have been developed and should not be lost:
  - it may work if we manage to build up a team joining one of the major developer (LFoundry, AMS, or TowerJazz)
  - Focusing on some service blocsk or rad-hard cells
  - Valentino/Hitesh leading Luca, Ettore + Mandi students
  - **Useful if agree on a project with other ATLAS groups in a two months time scale**

# Developments in ATLAS: Testing+Module






- Characterization of new monolithic devices
  - Test systems:
    - Caribou for AMS
    - USBPix 3 for LF, TowerJazz... and also for RD53
  - The developers will be much faster in performing the early measurements: try to define some specific topics:
    - SEU cross section seems uncovered till now
    - need to develop setup and irradiation location
    - Match expertise in Milano (Mauro, Valentino...)
- Take part in module design:
  - more likely 4 adjacent chips to build a drop-in module “quad-module”
  - topics to address: **flex layout**, data aggregator, power distribution
- A possibility would be to volunteer for taking part in test beams
  - hot season in summer, with all devices to evaluate

# Developments in ATLAS: Simulation

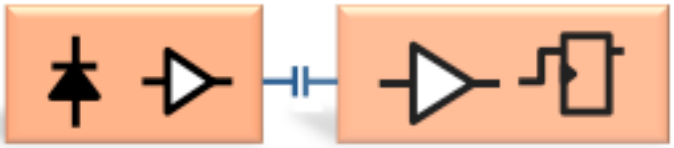
- Top priority
  - three pixel sizes in Layer 4, to compare with default 50×50×150
    - 36×36×25 (small fill factor)
    - 50×250×100 (large fill factor, fully depleted)
    - 50×250×50 (large fill factor, partly depleted)
  - **Possibly with reduced material**
    - **no FE chip (monolithic solution)**
  - Digitization:
    - threshold 1/5 of a MIP
    - noise 1/10 of threshold
    - 4 bit ToT for large fill factor solutions

**Requires new geometry**

**Full simulation: CPPM**

- Second Priority
  - A parameter scan (*z*-pitch, depletion, threshold and noise) for the monolithic solution would be preferred:
    - fast digitization?
    - how easy is two compare two digitization settings?
  - **CCPD solution for layer 0**:
    - 25×25×50 assuming pixel encoding (no ToT information)
  - **Redundancy:**
    - extension of CMOS to Layer 3

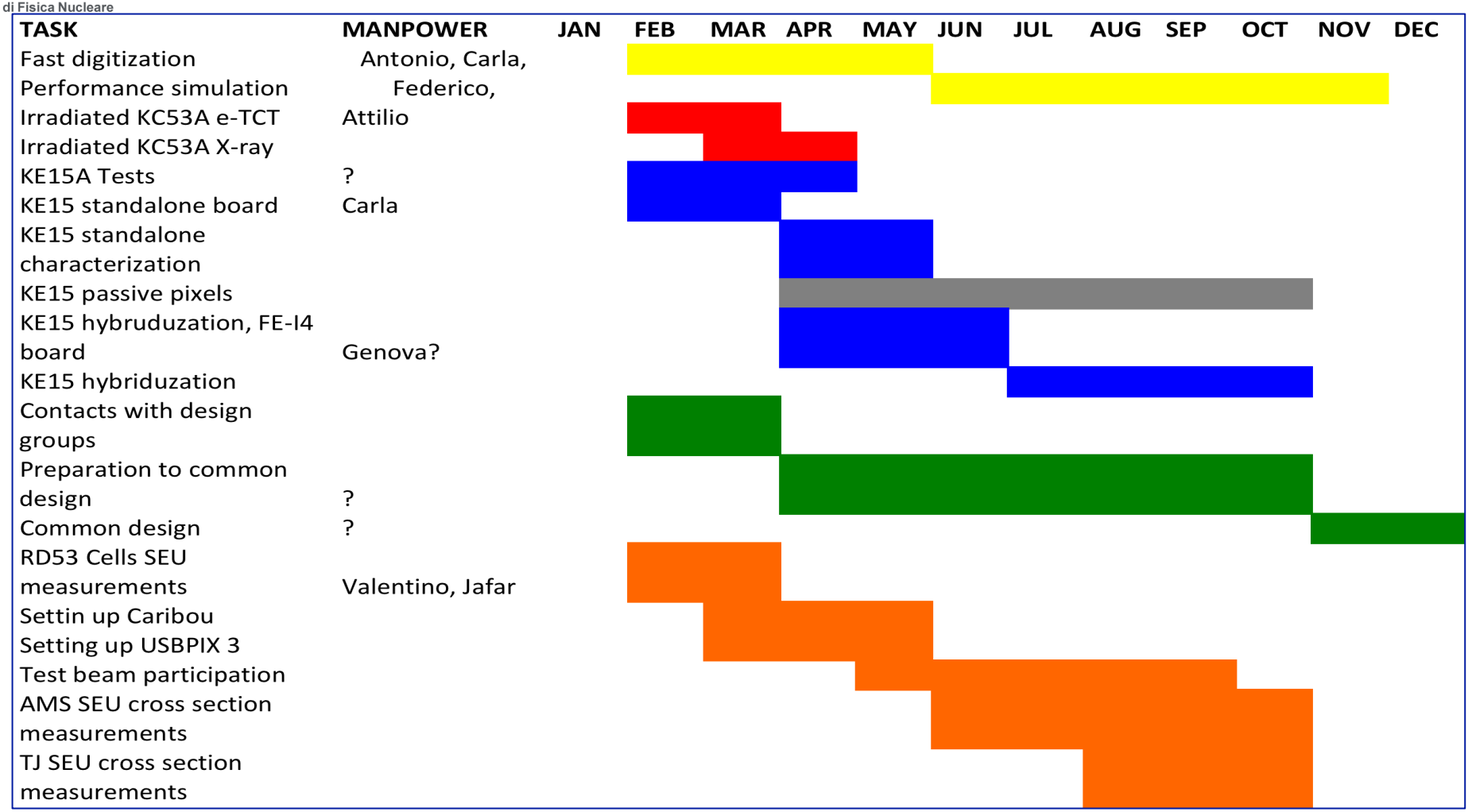
**Fast digitization: Bologna**



# HVR - CCPD

## BACKUP

# Workplan



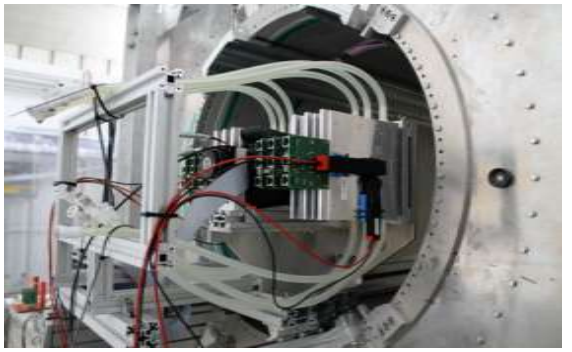

- Just a draft, summarizing previous consideration:
  - to modulate according to manpower, adjust timeline, boxes to be filled

# status and plans

## Plans for 2017

- requested 3x3 weeks @ CERN: H6A/B and H8B together with Mathieu
  (beam available early May to mid October)
- 1x3 weeks, 1x2 weeks, plus two weeks CMOS? @ DESY
  (beam available mid- to late February to mid December)

- re-try data taking in B-field (DESY, 1T dipole)
- 'combined' testbeam with ITk strips



| | Week | | TB21 | | TB22 | | TB24/1 | | TB24 |
|---|---|---|---|---|---|---|---|---|---|
| | | | DATURA | none | DURANTA | none | Telescope in PCMAG | PCMAG | none |
| 2-Jan-17 | 1 | | Shutdown | | | | | | |
| 9-Jan-17 | 2 | | | | | | | | |
| 16-Jan-17 | 3 | | | | | | | | |
| 23-Jan-17 | 4 | | | | | | | | |
| 30-Jan-17 | 5 | | | | | | | | |
| 6-Feb-17 | 6 | | Startup | | Startup | | Startup | | Startup |
| 13-Feb-17 | 7 | | Goe-ATLAS-3D-Dia | | | LHCb-SCiFi | BELLE-II | | |
| 20-Feb-17 | 8 | | CMS-Tracker-PSP | | | LHCb-SCiFi | | | |
| 27-Feb-17 | 9 | | CMS-Tracker-PSP | | | ALICE-ITS | ATLAS ITk Pixel | | |
| 6-Mar-17 | 10 | | | | | ALICE-ITS | ATLAS ITk Pixel | | |
| 13-Mar-17 | 11 | | | | | CALICE-AHCAL | ATLAS ITk Pixel | | |
| 20-Mar-17 | 12 | | Mu3e | | ATLAS HV-CMOS-Pix | | | | |
| 27-Mar-17 | 13 | | CMS-Tracker-PSP | | ATLAS HV-CMOS-Pix | | | | |
| 3-Apr-17 | 14 | | CMS-Tracker-PSP | | | | | | |
| 10-Apr-17 | 15 | | | | | | | | |
| 17-Apr-17 | 16 | | | | | | | | |
| 24-Apr-17 | 17 | | ATLAS-Strip-Pitch | | ATLAS-Strip-Glue | | | | |
| 1-May-17 | 18 | | | | | | | | |
| 8-May-17 | 19 | | | | | | | | |
| 15-May-17 | 20 | | | | Setup | | | | |
| 22-May-17 | 21 | | | | ATLAS-ITk-Strips | | | | |
| 29-May-17 | 22 | | | | ATLAS-ITk-Strips | | | | |
| 5-Jun-17 | 23 | | | | | | | | |
| | | | ... | | | | | | |
| 13-Nov-17 | 46 | | | | | | | | |
| 20-Nov-17 | 47 | | | | | | | | |
| 27-Nov-17 | 48 | | | | | | | | |
| 4-Dec-17 | 49 | | CMS-Pixel-Phase-2 | | ATLAS-ITk-Pixel | | | | |
| 11-Dec-17 | 50 | | CMS-Pixel-Phase-2 | | ATLAS-ITk-Pixel | | | | |
| 18-Dec-17 | 51 | Beam till 22/12 0800 | | | | | | | |
| 25-Dec-17 | 52 | | Shutdown | | | | | | |