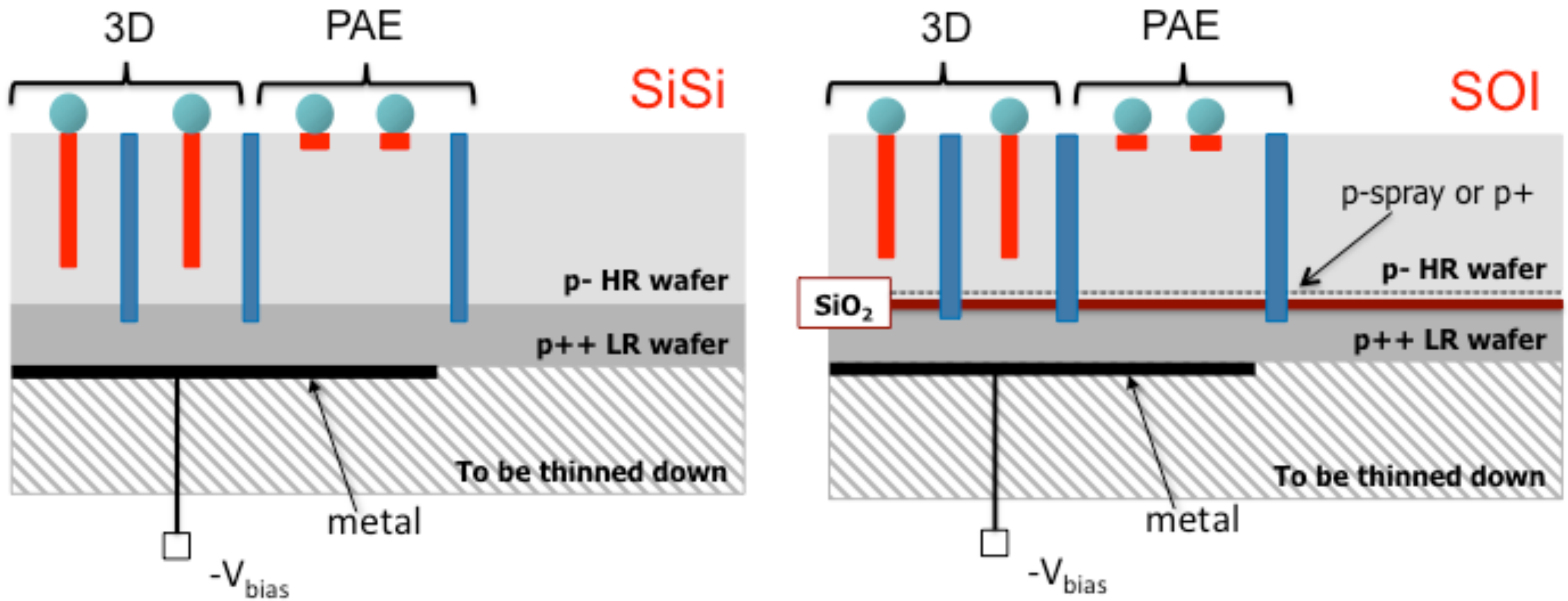
3D Sensors

Gian-Franco Dalla Betta
University of Trento and TIFPA INFN, Trento, Italy
gianfranco.dallabetta@unitn.it
on behalf of Trento and Udine groups

Work carried out within INFN RD_FASE2 and AIDA2020 projects:
Development of new thin 3D and Planar Active Edge (PAE) pixel sensors on 6” p-type wafers at FBK:

- Technology and design to be optimized and qualified for extreme radiation hardness (2x10^{16} n_{eq} cm^{-2})
- Pixel layouts compatible with present (for testing) and future (RD53 65nm) FE chips of ATLAS and CMS

New single-side approach to 3D/PAE

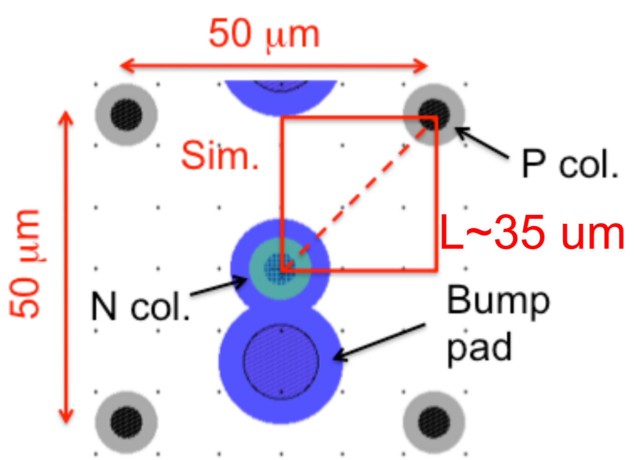


- Thin sensors on support wafer: SiSi or SOI → Substrate qualification
- Ohmic columns/trenches depth > active layer depth (for bias)
- Junction columns depth < active layer depth (for high V_{bd})
- Reduction of hole diameters to ~5 um
- Holes (at least partially) filled with poly-Si

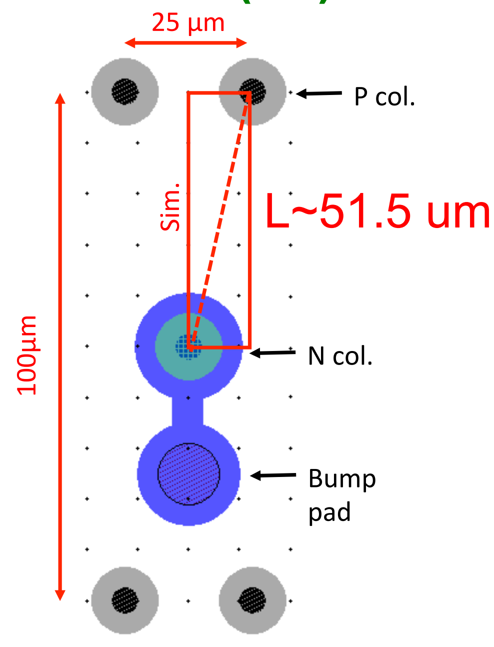
Process Tests

Small-pitch 3D pixel layouts: geometrical constraints

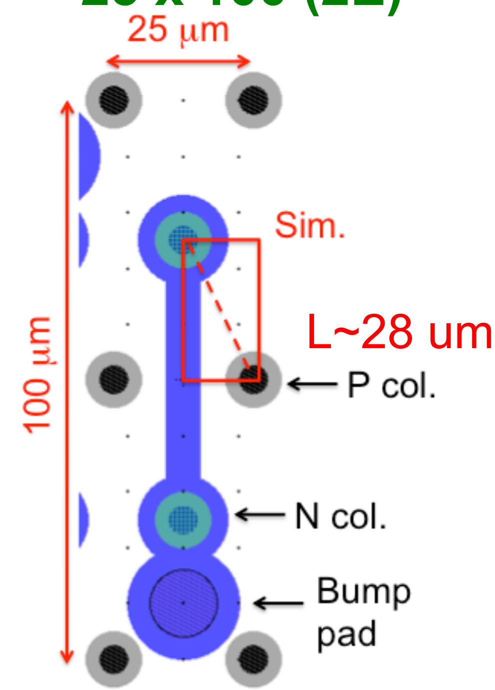
50 x 50 (1E)



25 x 100 (1E)

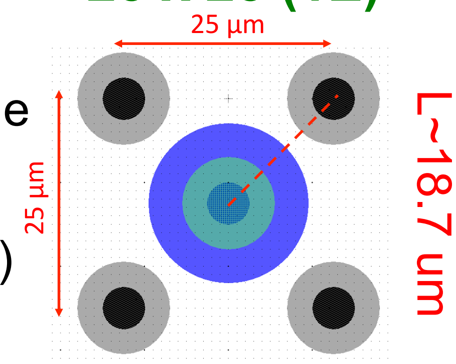


25 x 100 (2E)



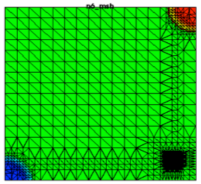
All designs refer to FBK SS-3D process, assuming d=5 μm

25 x 25 (1E)

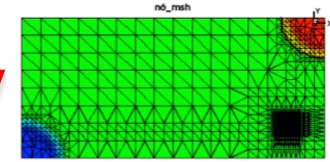


- No problems with 50x50 -1E (and 25x100 -1E) designs
- 25x100 -2E is difficult, because the bump pad size does not scale
  - new ideas to be tested in SS-3D (e.g., bumps on columns)
  - this would allow for even smaller sizes (with higher dead volume)

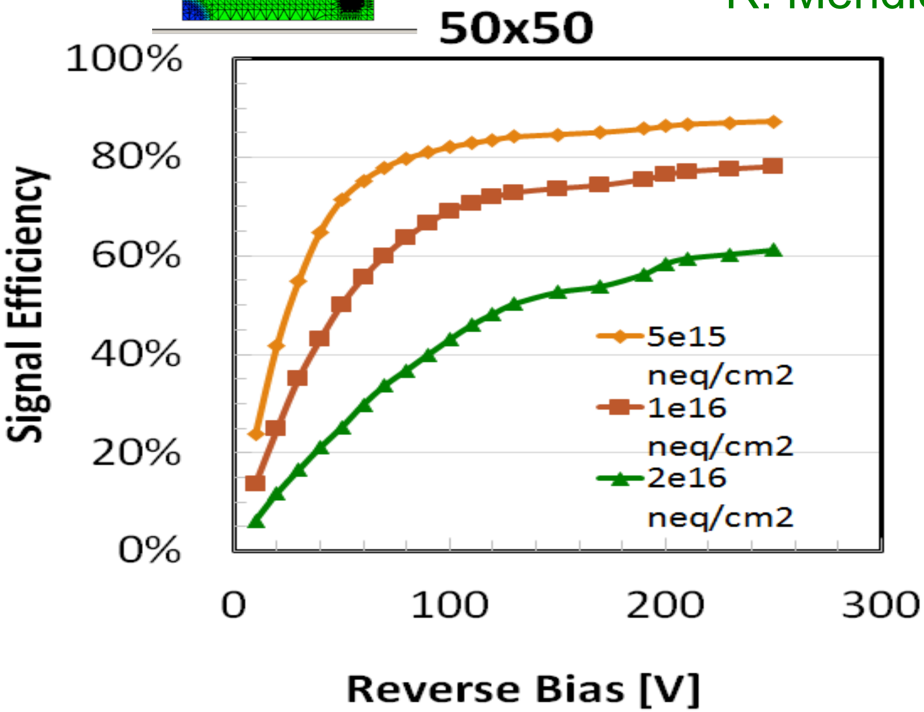
G.-F. Dalla Betta et al., IEEE NSS 2015, N3C3-5

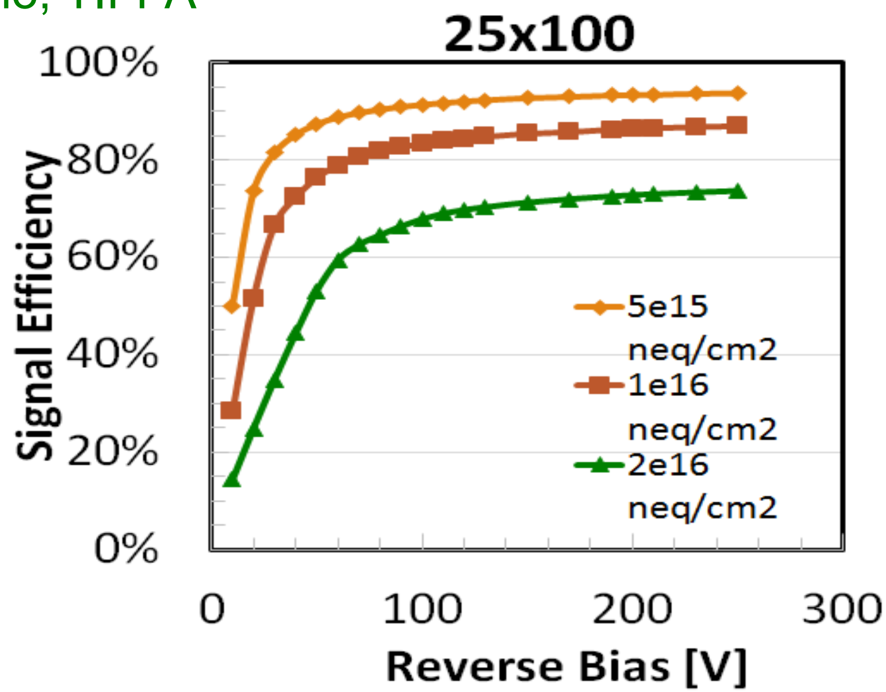


Simulated Signal Efficiency



R. Mendicino, TIFPA

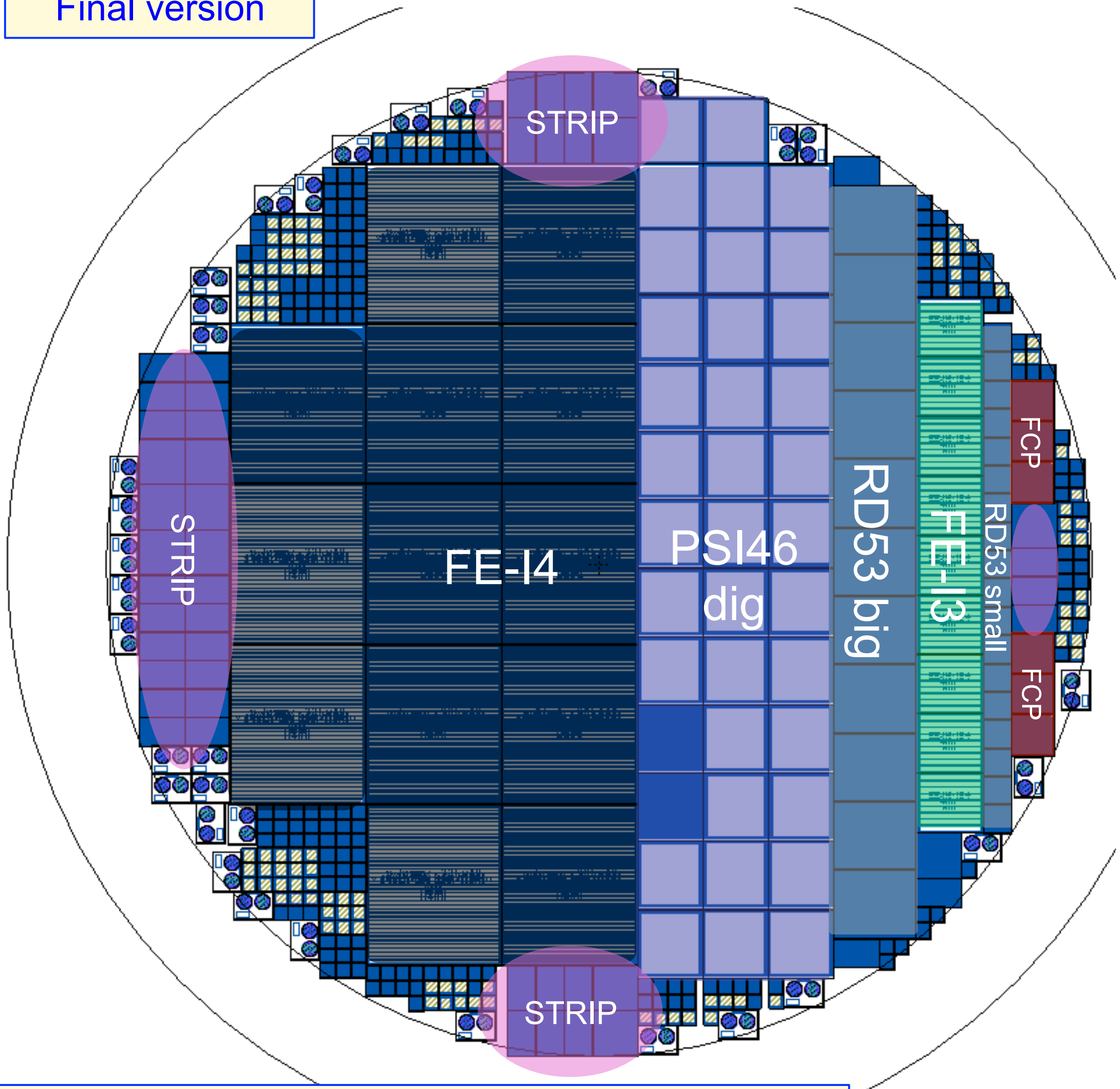




- Simplified simulation domain (2d slice), no pixel edge effects
- Bulk damage: new Perugia radiation damage model
- Very high average signal efficiency
- Significant variations of signal efficiency with hit position
- Possible impact ionization effects at high field

3D Pixel Wafer Layout

Final version



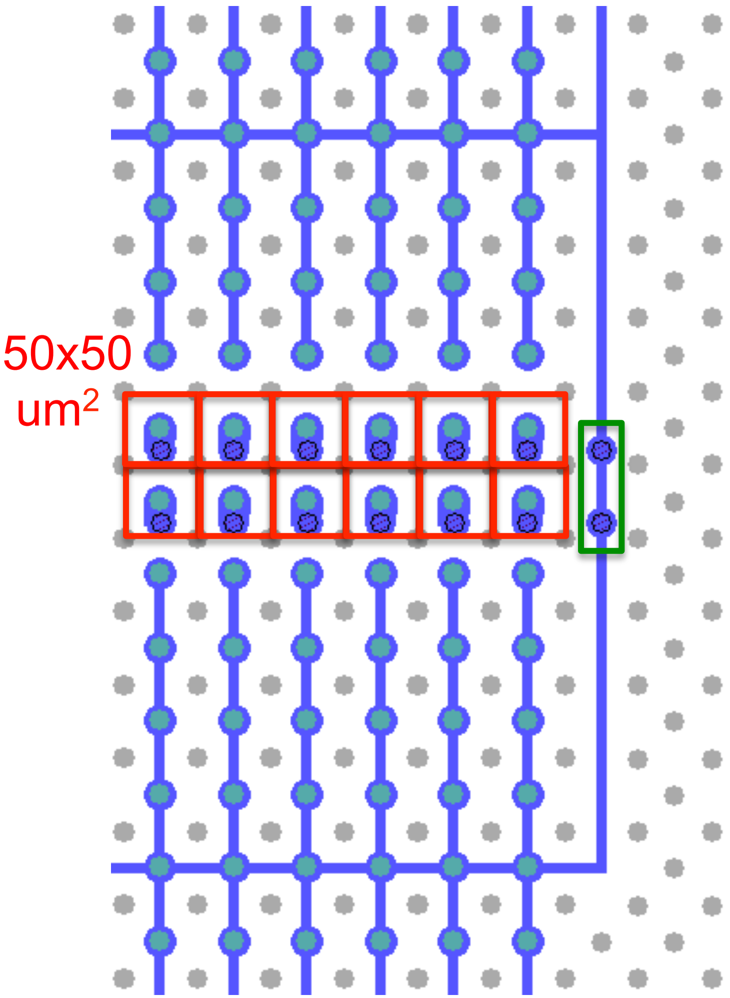
+ Test structures (strip, diodes, etc)

Many different pixel geometries and pitch variations:

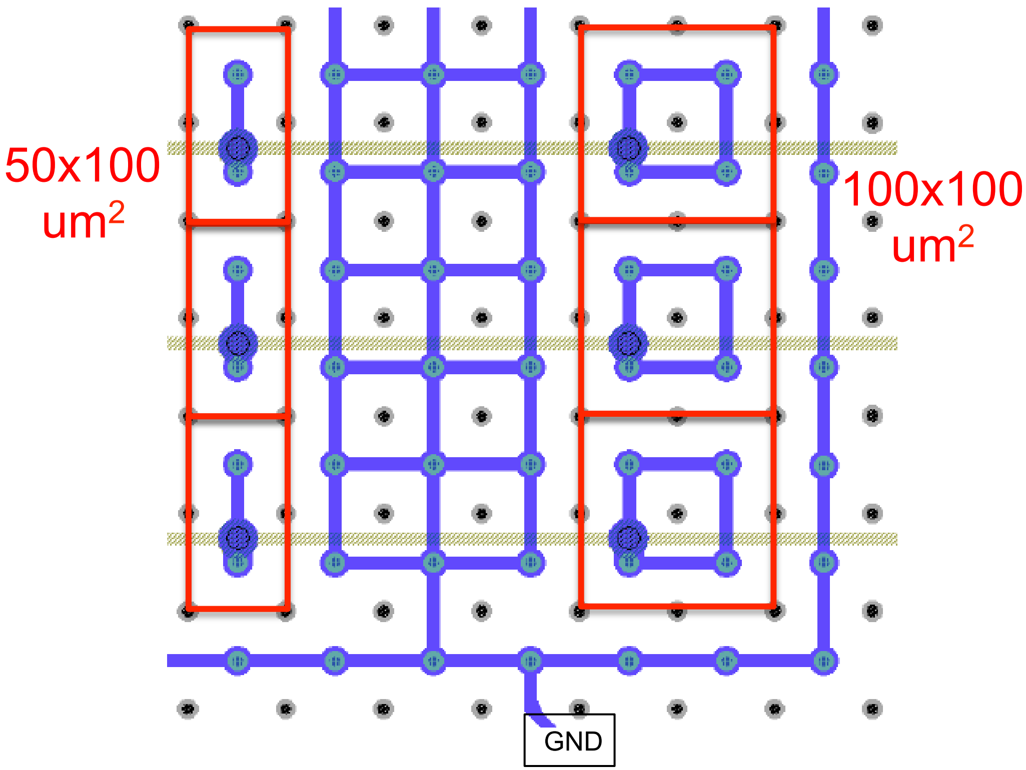
- FE-I4
  - 50 x 250 (2E) std
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
  - 25 x 500 (1E)
- FE-I3
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
- PSI46dig
  - 100 x 150 (2E and 3E) std
  - 50 x 50 (1E and 2E)
  - 50 x 100, 100 x 100 (2E + 4E)
  - 50 x 100, 100 X 150 (2E + 6E)
  - 25 x 100 (1E and 2E)
- FCP
  - 30 x 100 (1E)
- RD53
  - 50 x 50 (1E)
  - 25 x 100 (1E)
  - 25 x 100 (2E)

New pixels with existing ROCs ?

ATLAS FE-I4 50x50 (1E) + grid



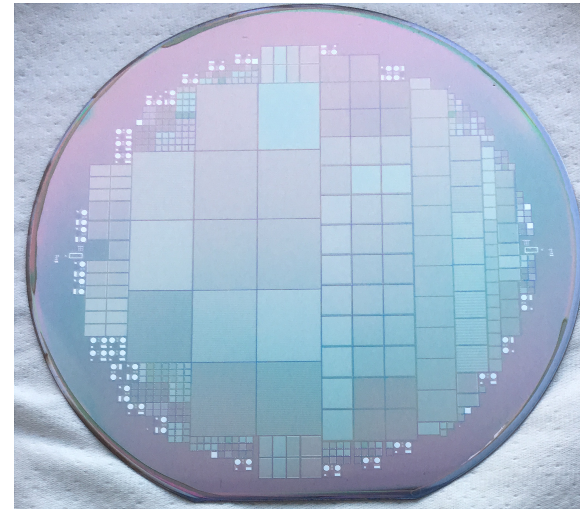
CMS PSI46: 50x50 (2E+4E) + grid

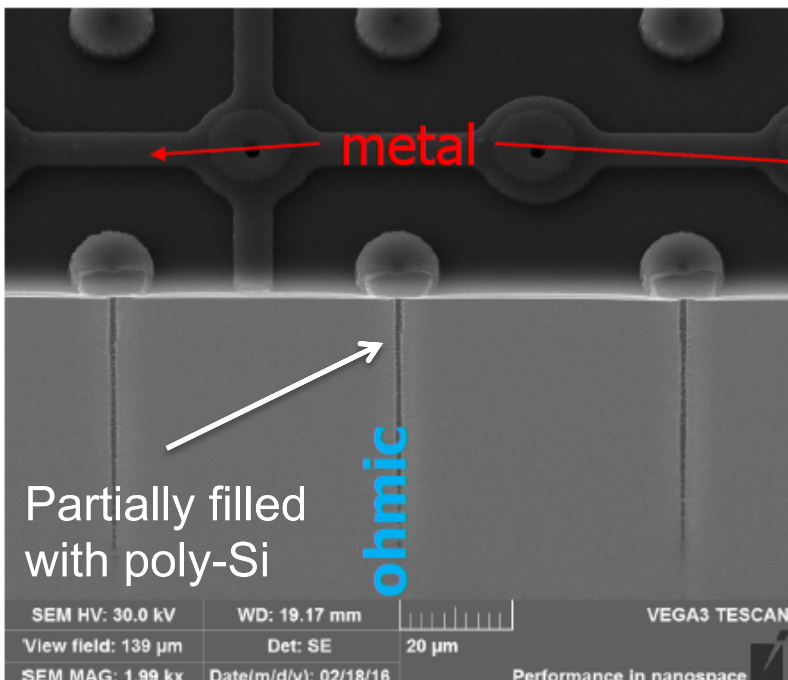


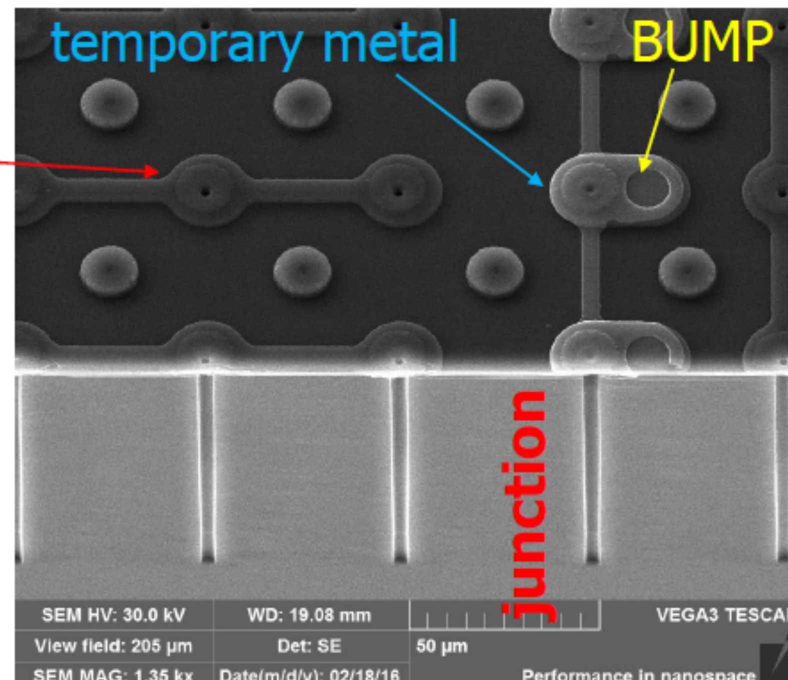
Small pixels take all bonding pads + rest of pixels at GND using a metal grid and extra-pads at the periphery

Sensor fabrication

- Ten wafers processed
- Two different active thicknesses: 100 vs 130 μm
- Two process splits:
  - sintering temperature (350 vs 420 °C)
  - p-Poly-Si etching (with and w/o mask)



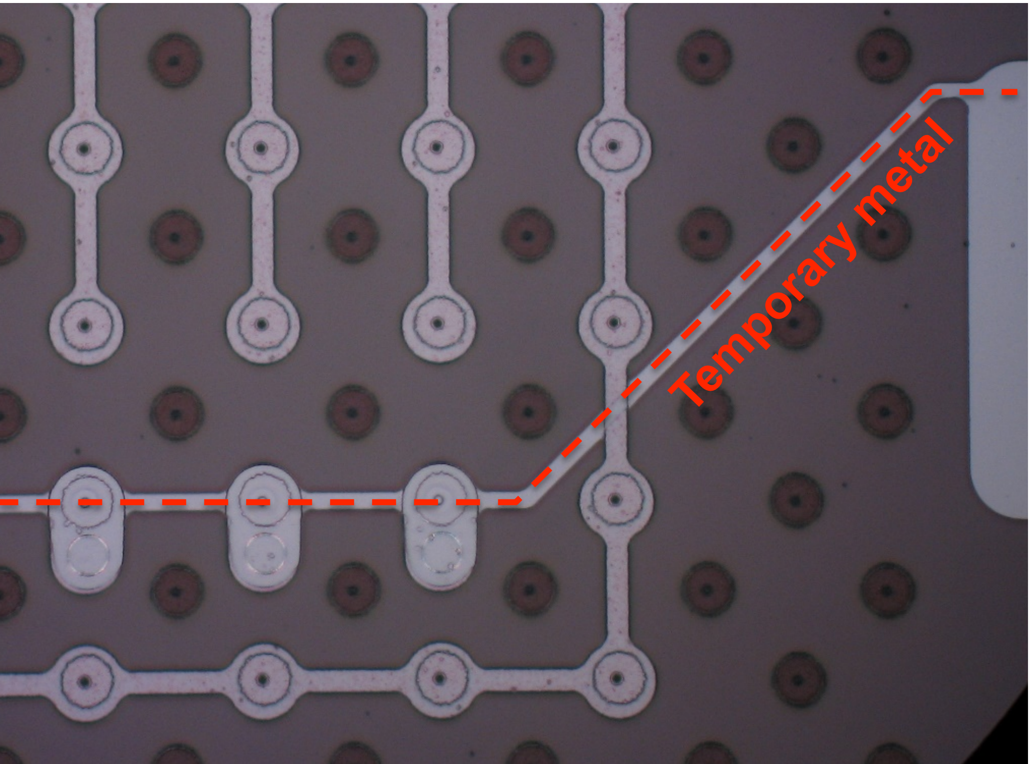




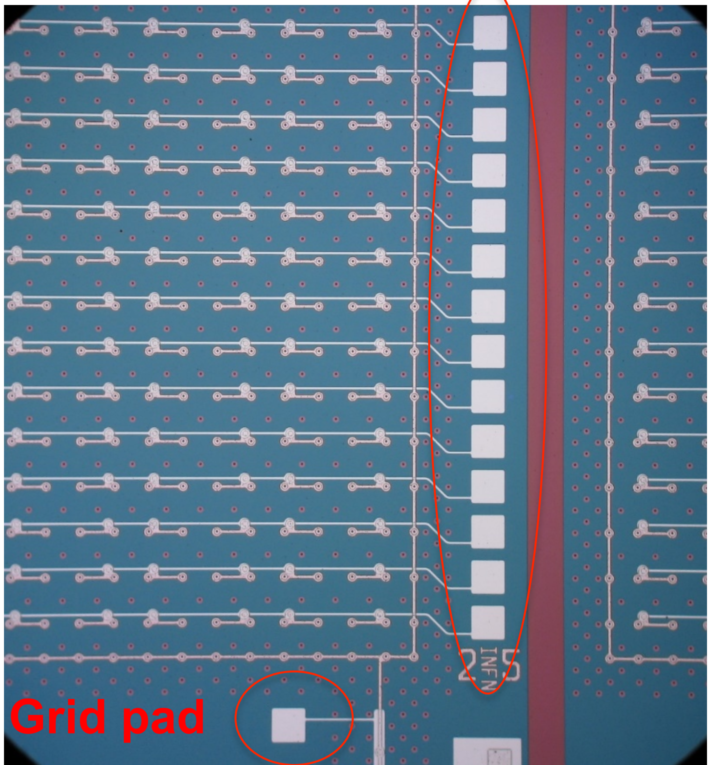
Temporary metal tests on pixels

- Rows of pixels are shorted by temporary metal for electrical tests on wafer (more effective monitoring of process defects)
- Total currents are obtained by the sum of all single-row and grid currents

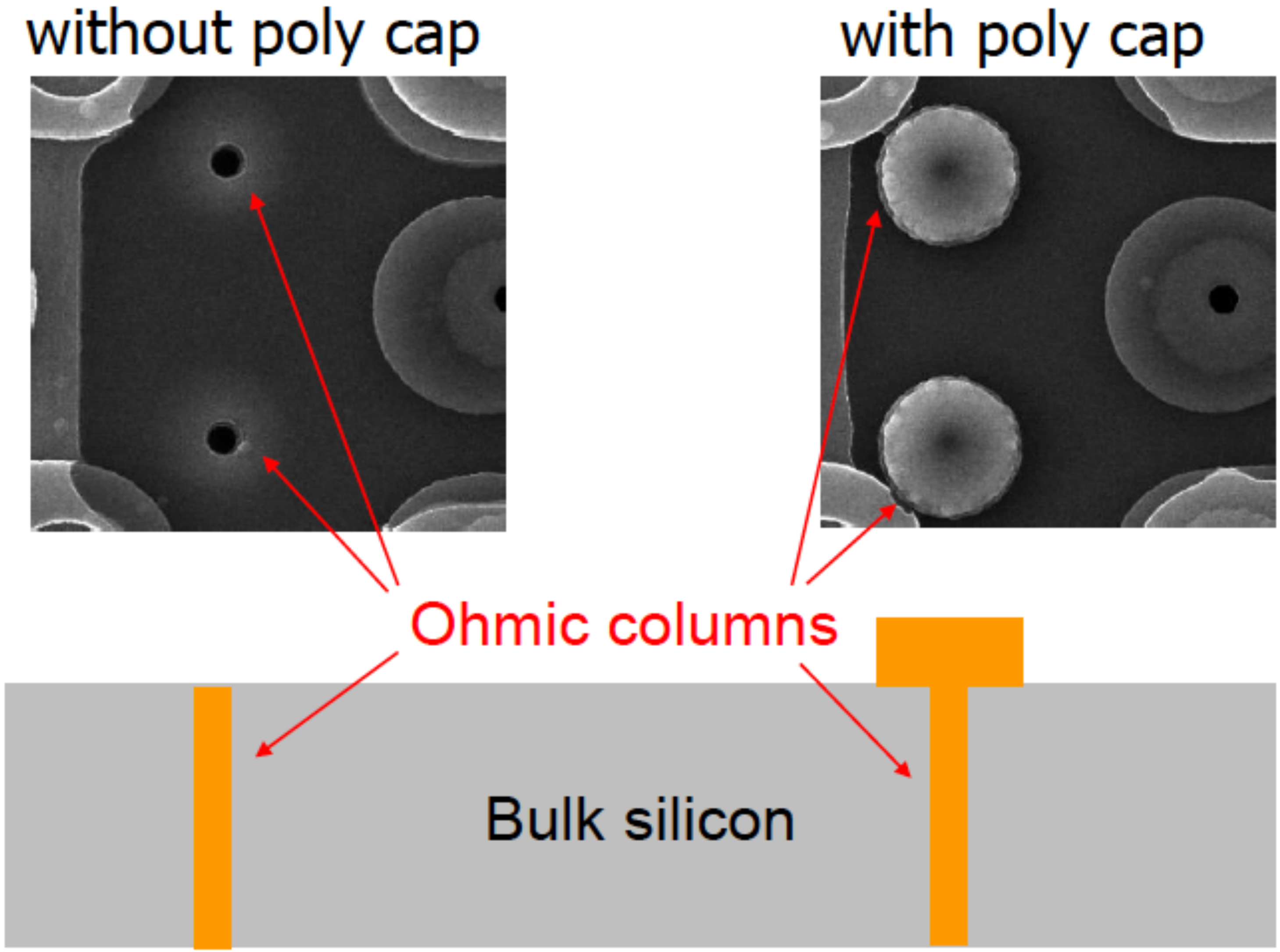
Permanent metal



Temporary metal pads

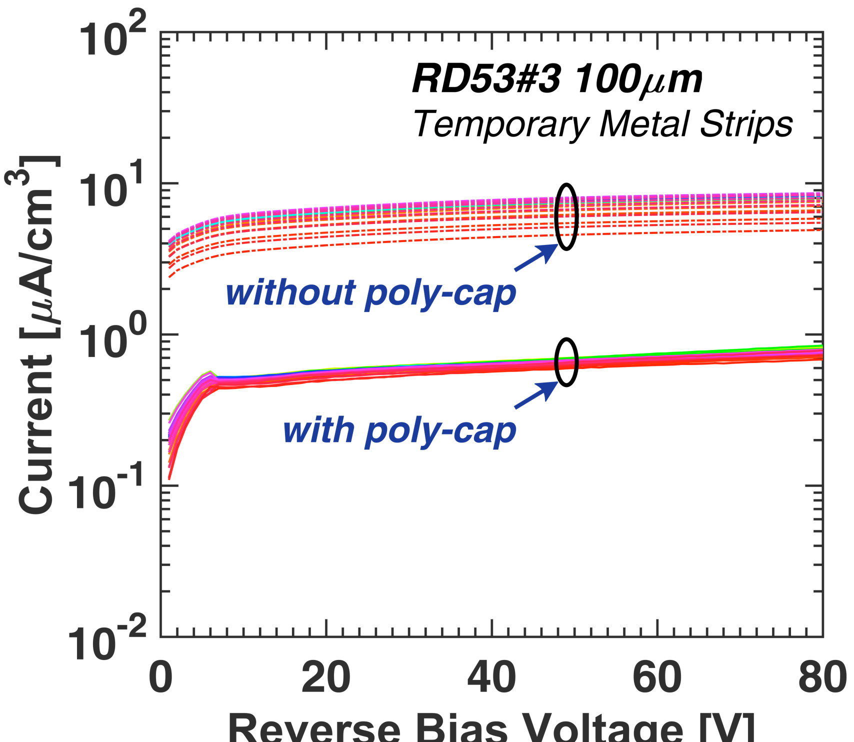


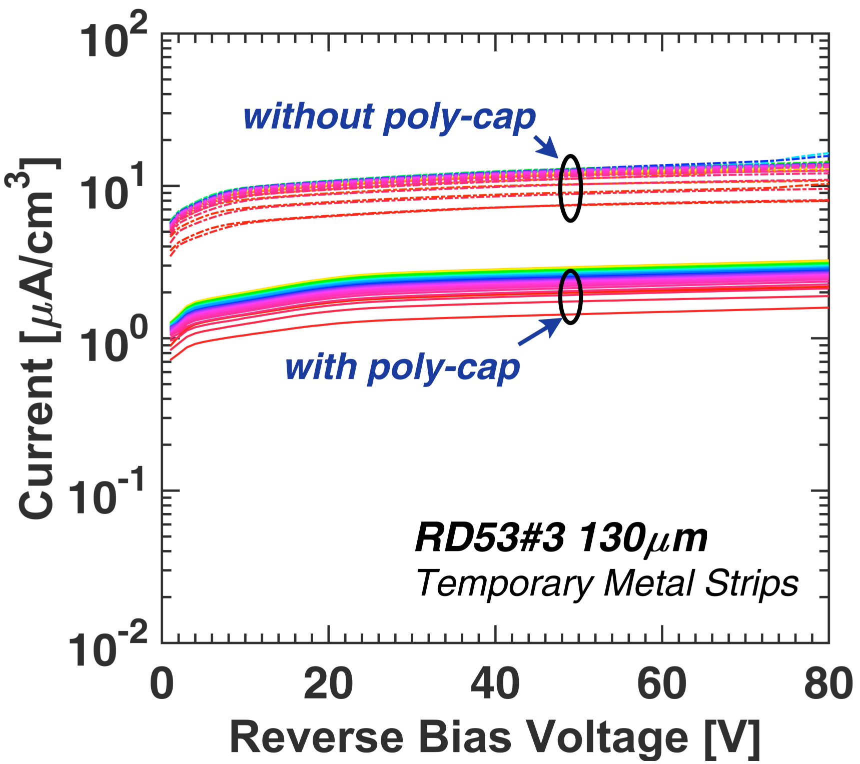
p-Poly-cap split



Impact of poly-cap on leakage current

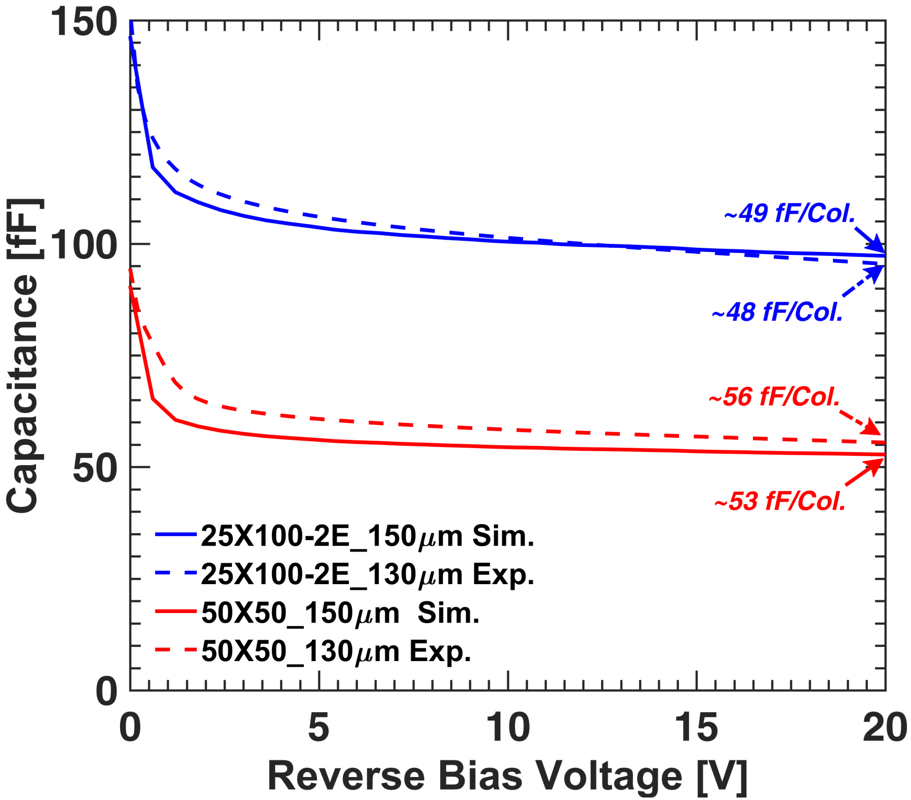
- From temporary metal “RD53” measurements (raws of pixels)
- Leakage currents are all low (~1 pA per column),
- But a significant difference can be observed w and w/o poly-cap

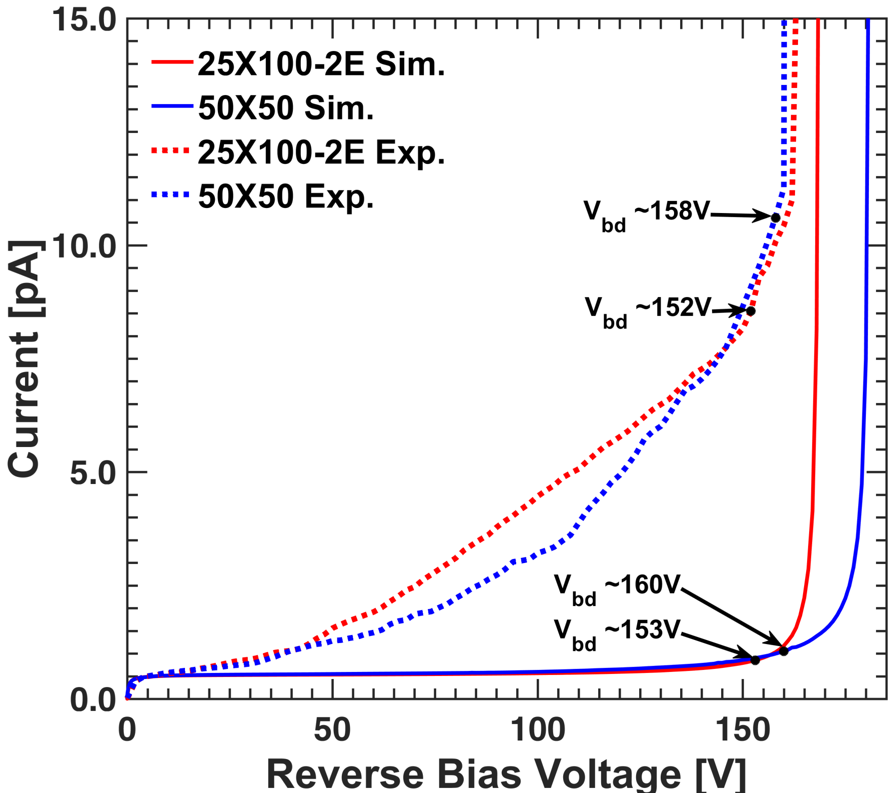




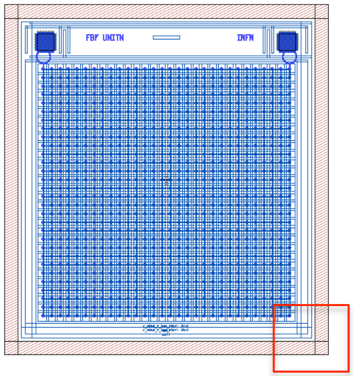
Measurements vs TCAD simulations

- From 3D diode measurements
- Very good agreement in C-V curves
- Good agreement in I-V curves but for the slope (that depends on interface states, so far not included in the model)

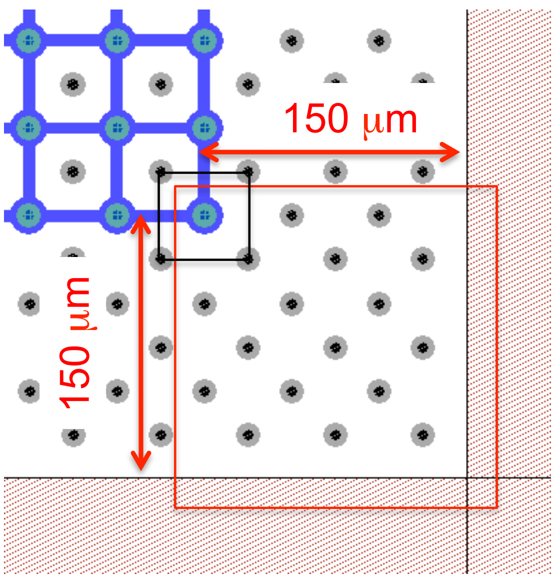


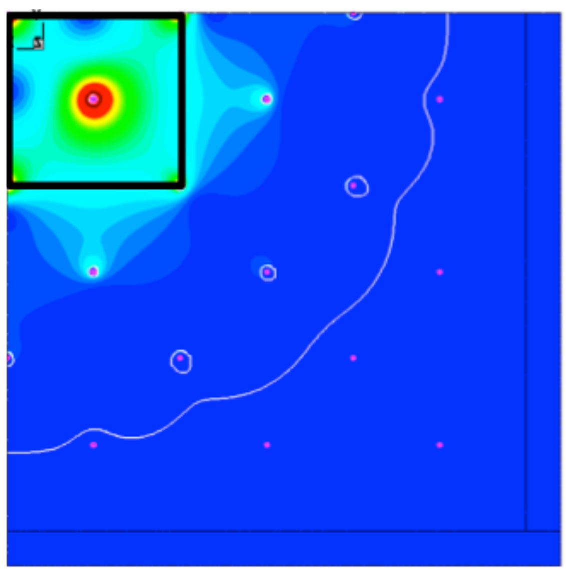


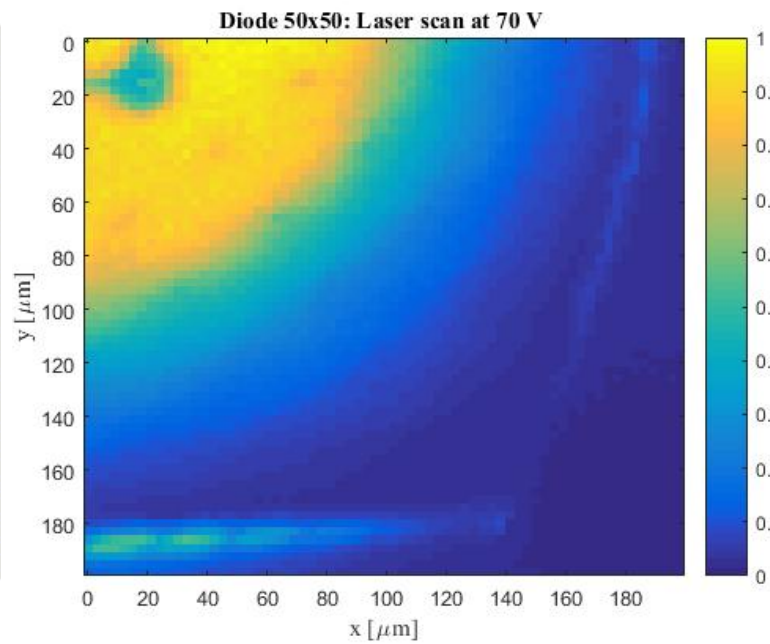
Slim edge laser test



- Slim edge based on multiple ohmic columns developed for IBL (~200 µm) M. Povoli et al., JINST 7 (2012) C01015, here made slimmer (~100 µm) with reduced inter-electrode spacing
- Safe operation of 3D diode (50 µm x 50 µm design) tested with position resolved laser system
- High signal indicates extension of the depleted volume at the corner (~80 µm at 70 V), in good agreement with simulations

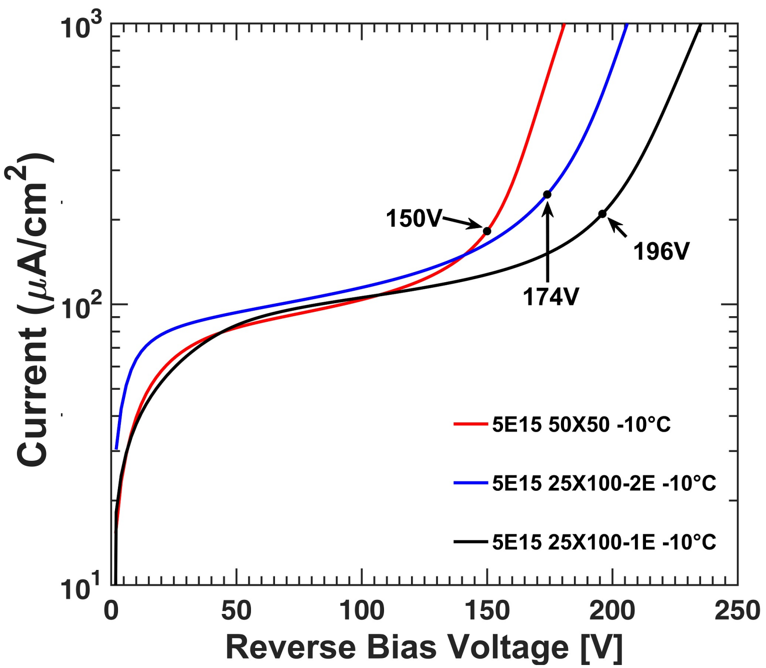


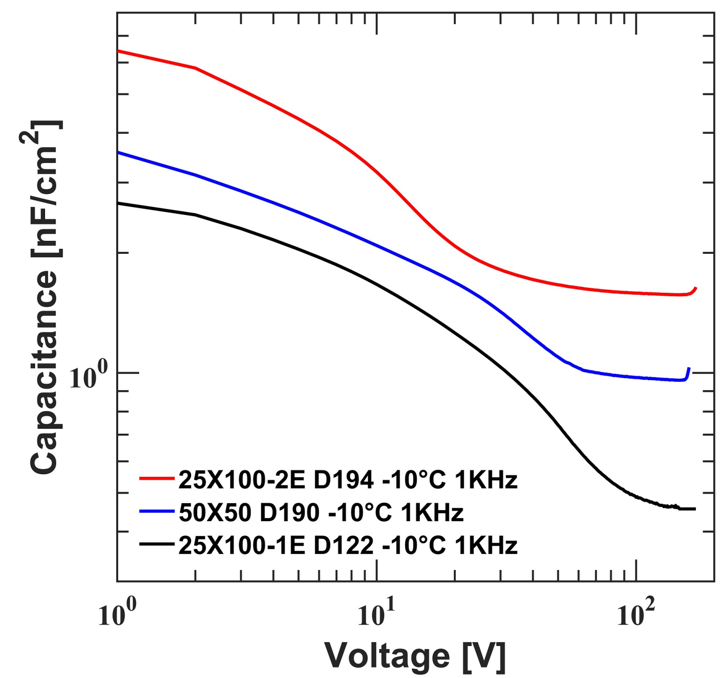




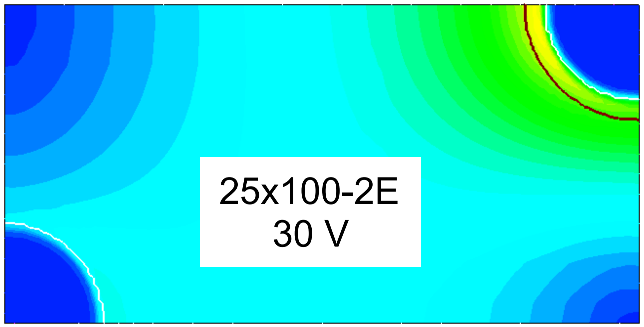
3D diode neutron irradiation

Neutron irradiation at $5x10^{15}$ n_{eq}/cm^2 (JSI Lubiana, thanks to V. Cindro)





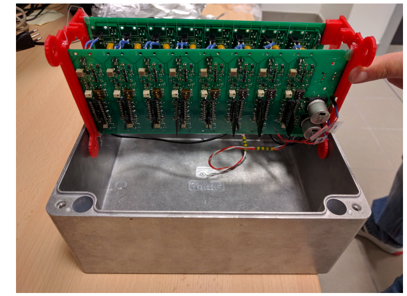
- Leakage current increases as expected:
  - Damage constant $\alpha \sim 4x10^{-17}$ A/cm
- Breakdown voltage also increases and is large enough wrt depletion voltage

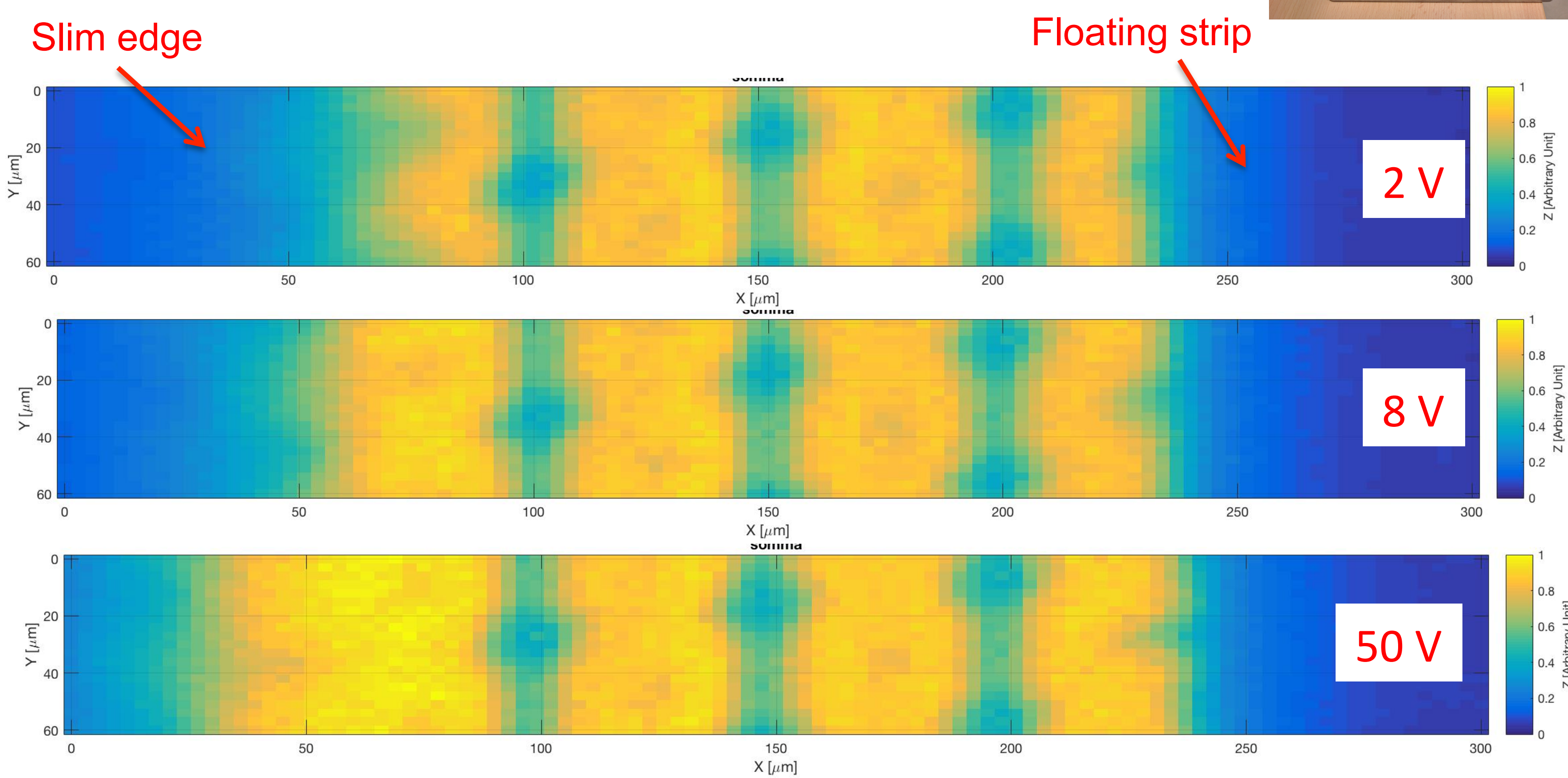


Preliminary results with 3D strips

R. Mendicino, TIFPA

- Position sensitive laser setup (λ=1064 nm)
- House made (discrete) read-out electronics
- High efficiency already at low voltage

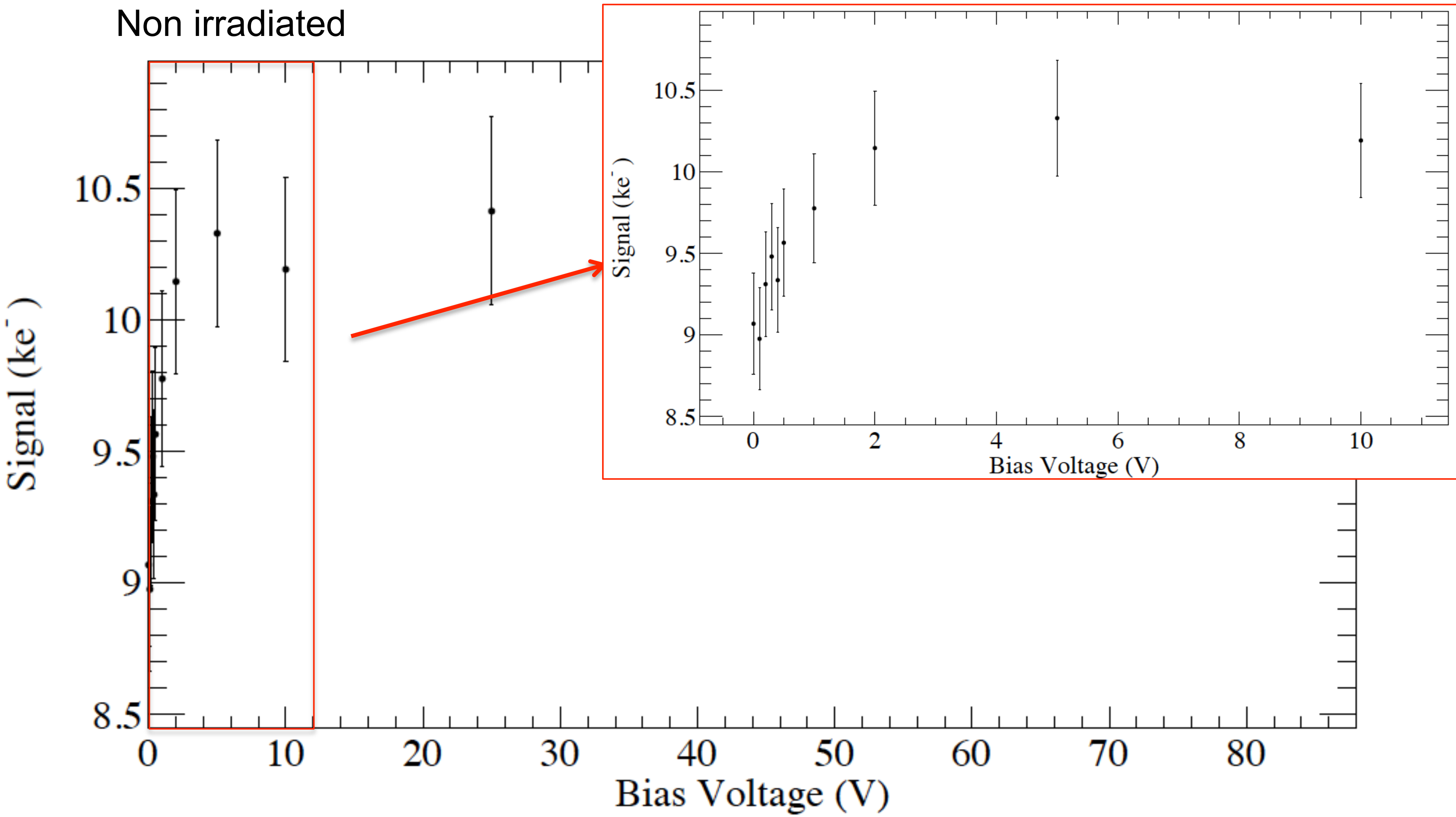




3D strips with Alibava: signal

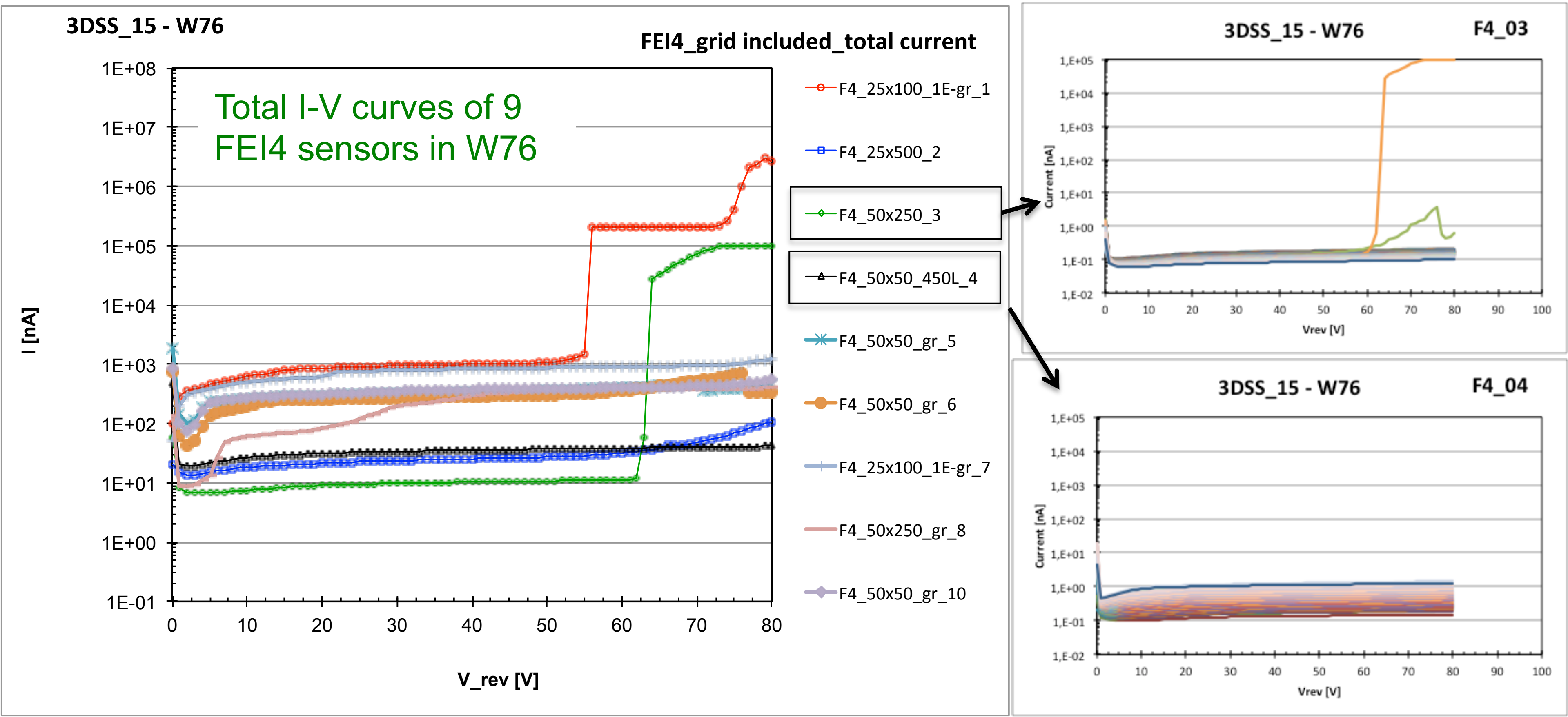
M. Hauser, U. Parzefall (Uni.Freiburg)

Non irradiated

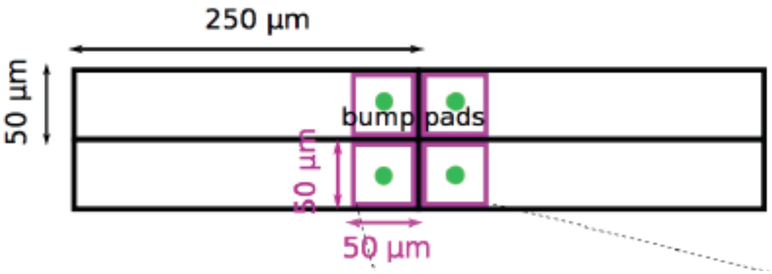


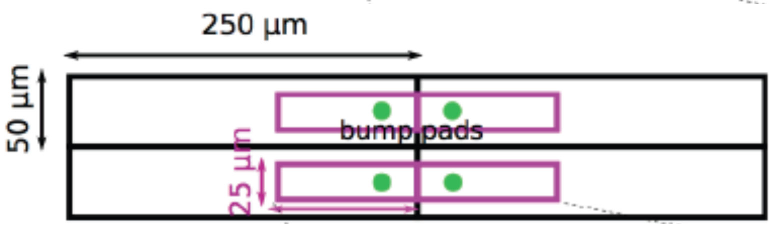
First 3D assemblies

- Wafers ranked according to overall yield from I-V curves (sorting by leakage current, breakdown voltage and slope)
- Two wafers (76, 78) sent to “Selex” for bump bonding
- First 9 sensors assembled in Genova and being tested

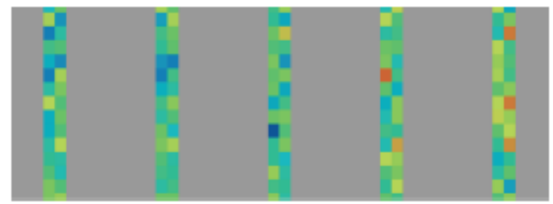


Test beam at CERN, Aug. 2016

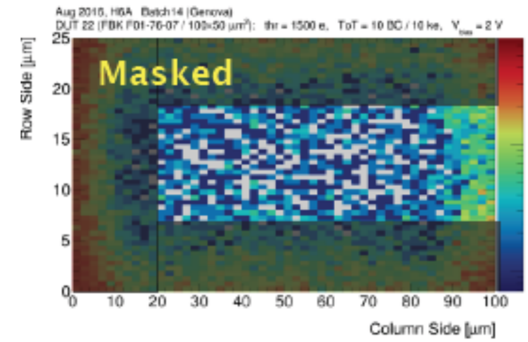


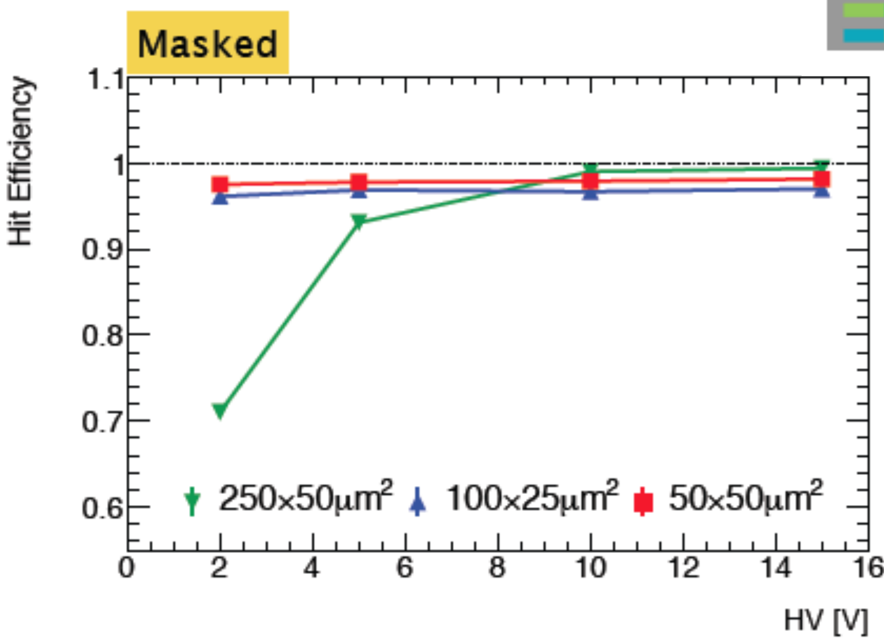


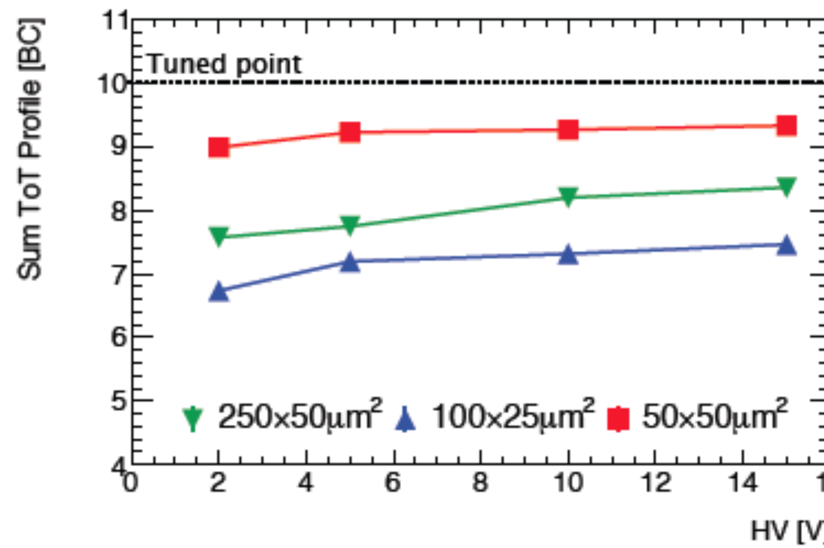
zoom of 50x50



zoom of 100x25



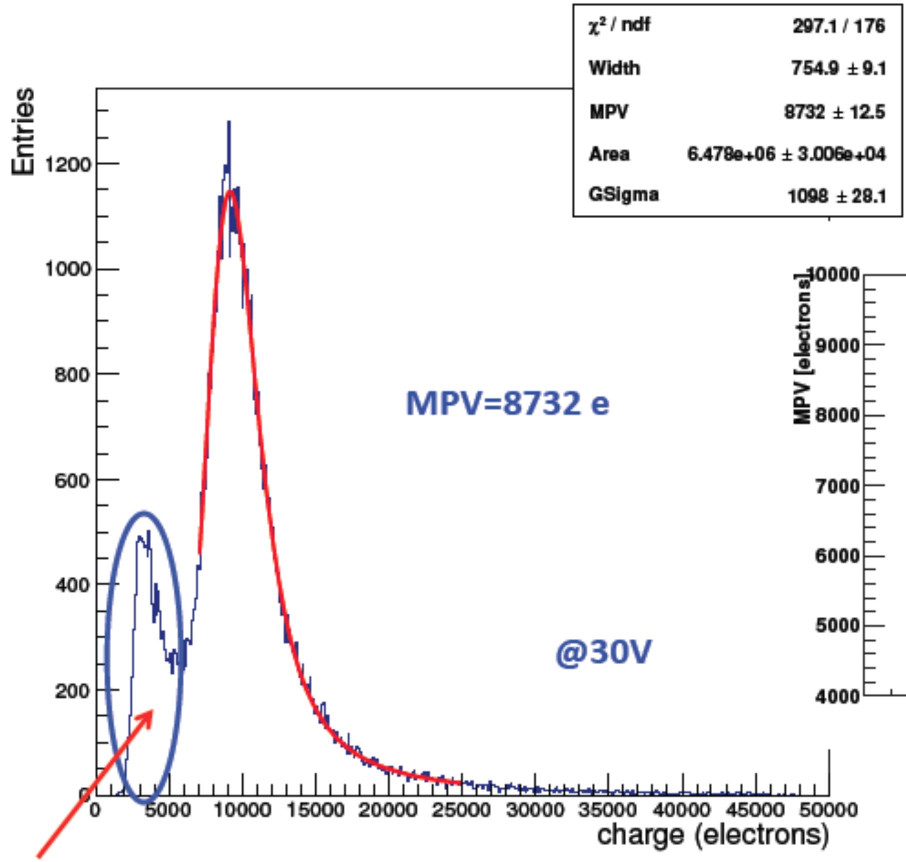


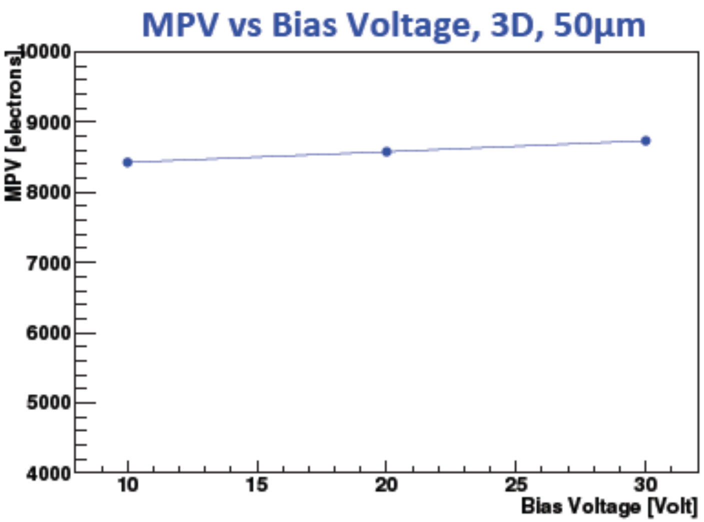


CMS test beam at Fermilab, Dec. 2016

3D Pixels with 50x50μm² pitch

- Preliminary results
- Sensors from same W76 worked at "Selex"



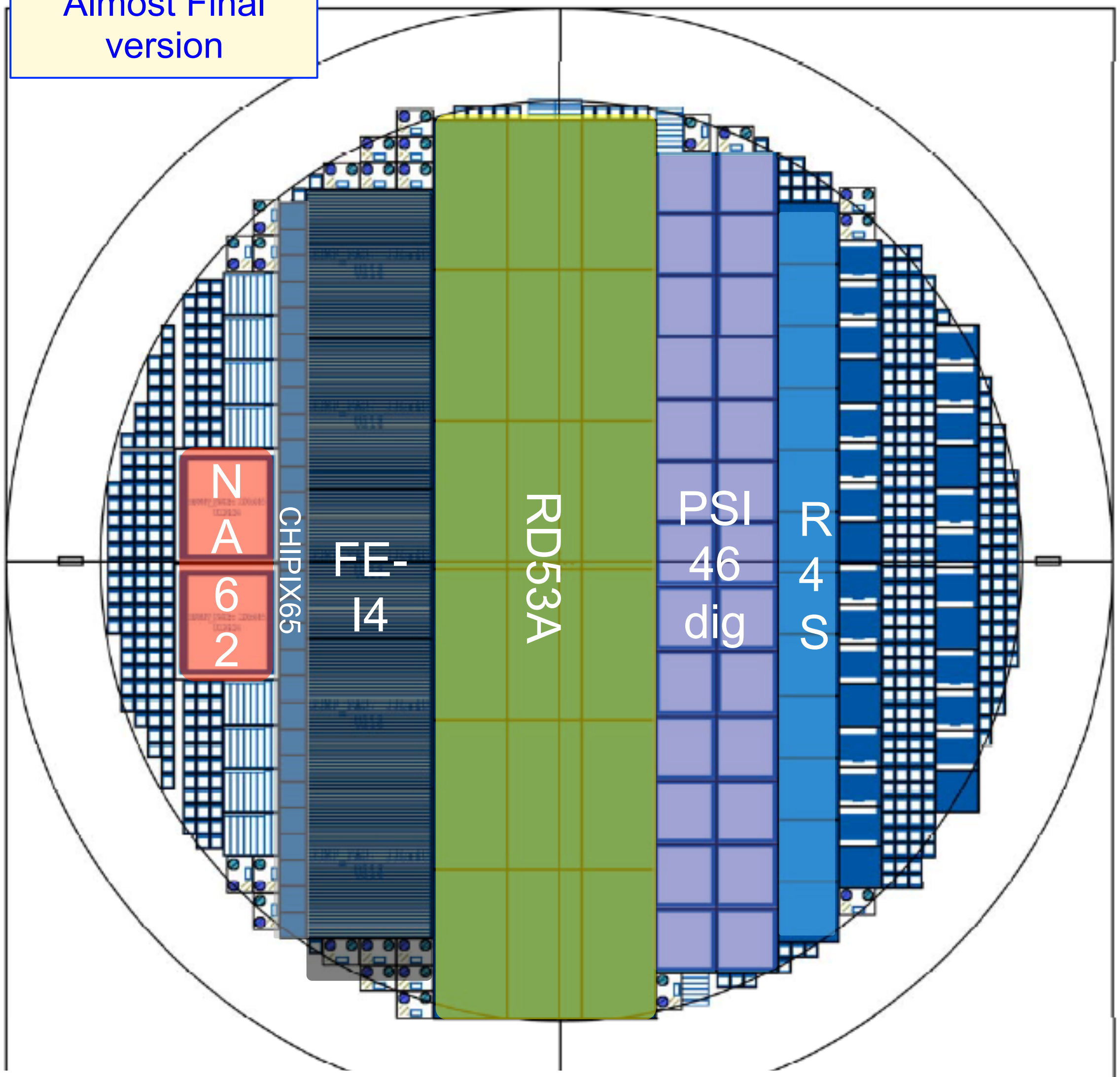


Charge shared by non connected adjacent pixels. This charge will not be there when reading out every single small pitch pixel

- No problem with I-V curves after BB
- Efficiency > 99% at 10V with std pixel sizes (100x150 um², 2E and 3E)

New 3D Pixel Wafer Layout

Almost Final version



DMS Sultan, UniTN

- FE-I4
  - 50 x 250 (2E) std
  - 50 x 100 (1E+9E)
  - 50 x 50 (5E)
- PSI46dig (also with BOC option)
  - 100 x 150 (2E and 3E) std
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
- R4S
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
- RD53A
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
- CHIPIX65
  - 50 x 50 (1E and 2E)
  - 25 x 100 (1E and 2E)
- NA62
  - For timing studies

+ Test structures (strip, diodes, etc)

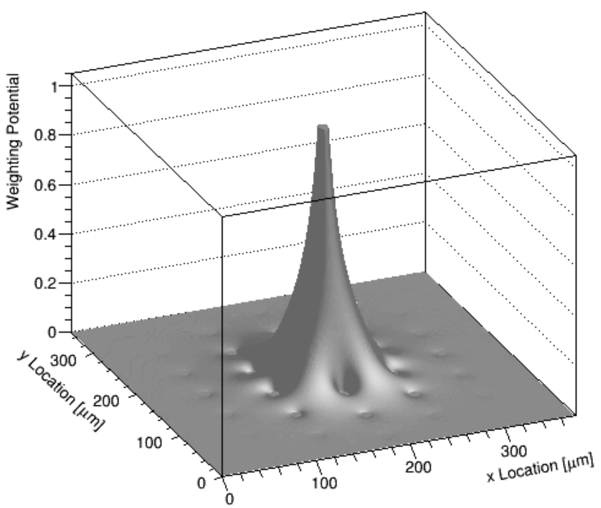
Batch funded by AIDA2020 and INFN

3D Sensor MC Simulation: weighting potential

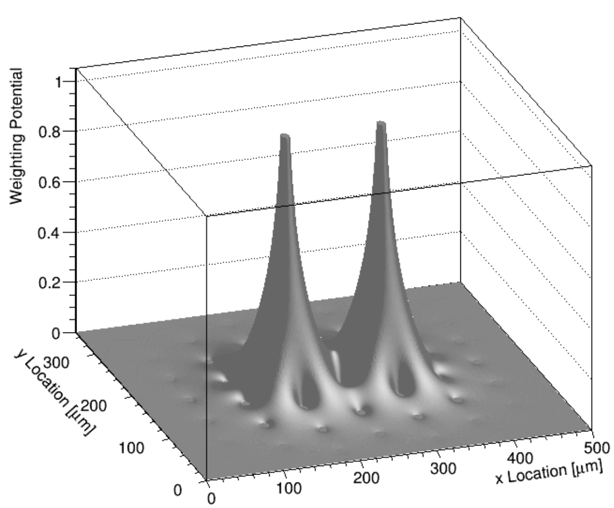
G. Giugliarelli, UniUD

- IBL 3D sensor geometry (2E pixels)
- Full 3D simulation of electrical quantities
- Accurate weighting potential calculation:
    - 1 column simulation
    - potential “duplication” by superposition

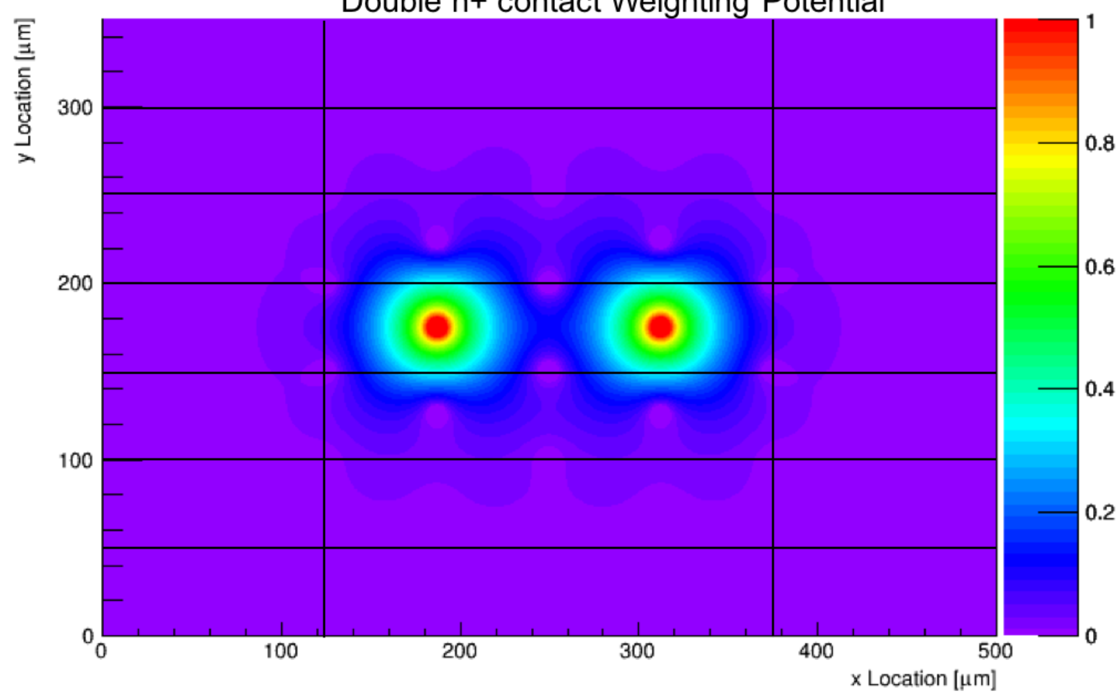
Weighting Potential for a single n+ contact



Weighting Potential for a pair of neighbour n+ contacts

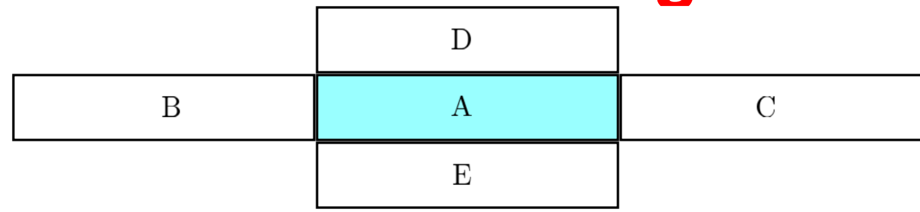


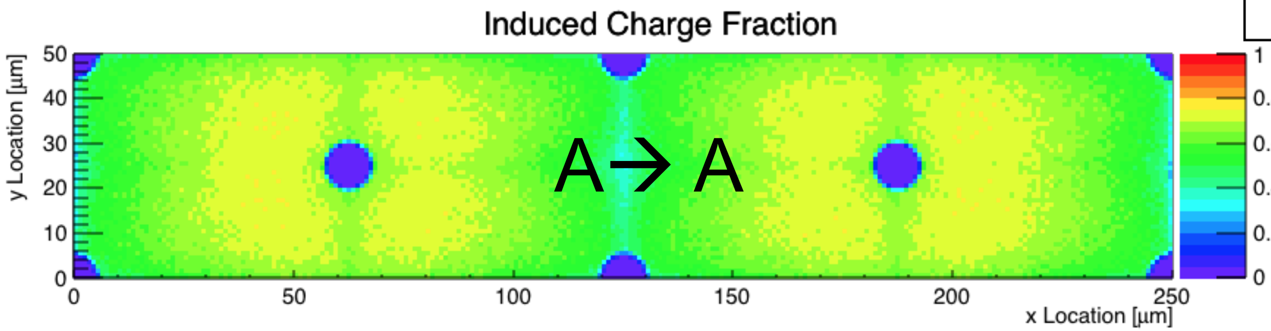
Double n+ contact Weighting Potential



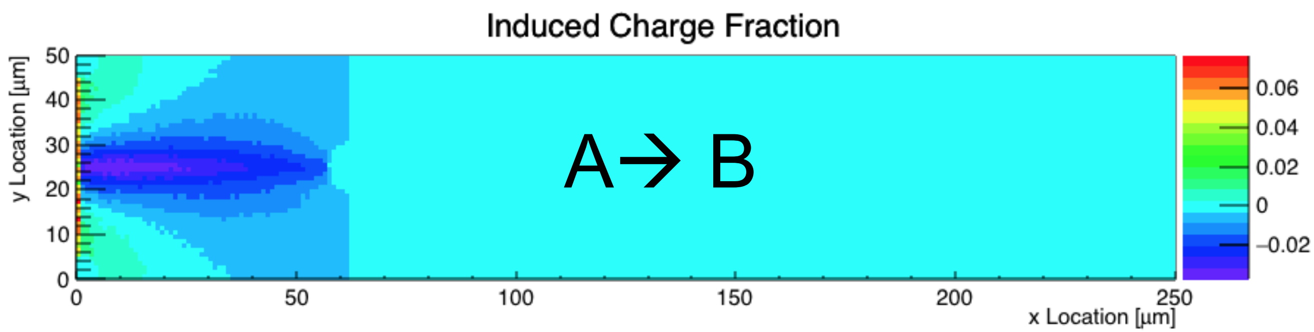
3D Sensor MC Simulation: induced charge

G. Giugliarelli, UniUD

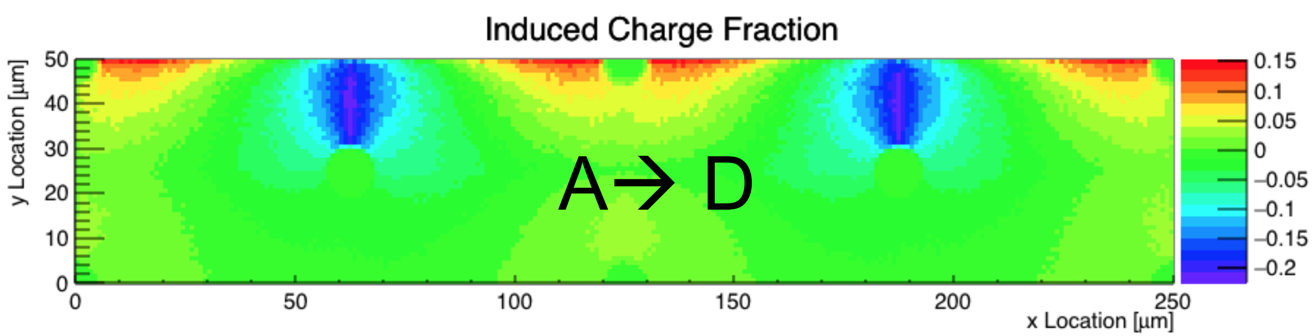




Irradiated at 5×10^{15} n_{eq} cm^{-2}



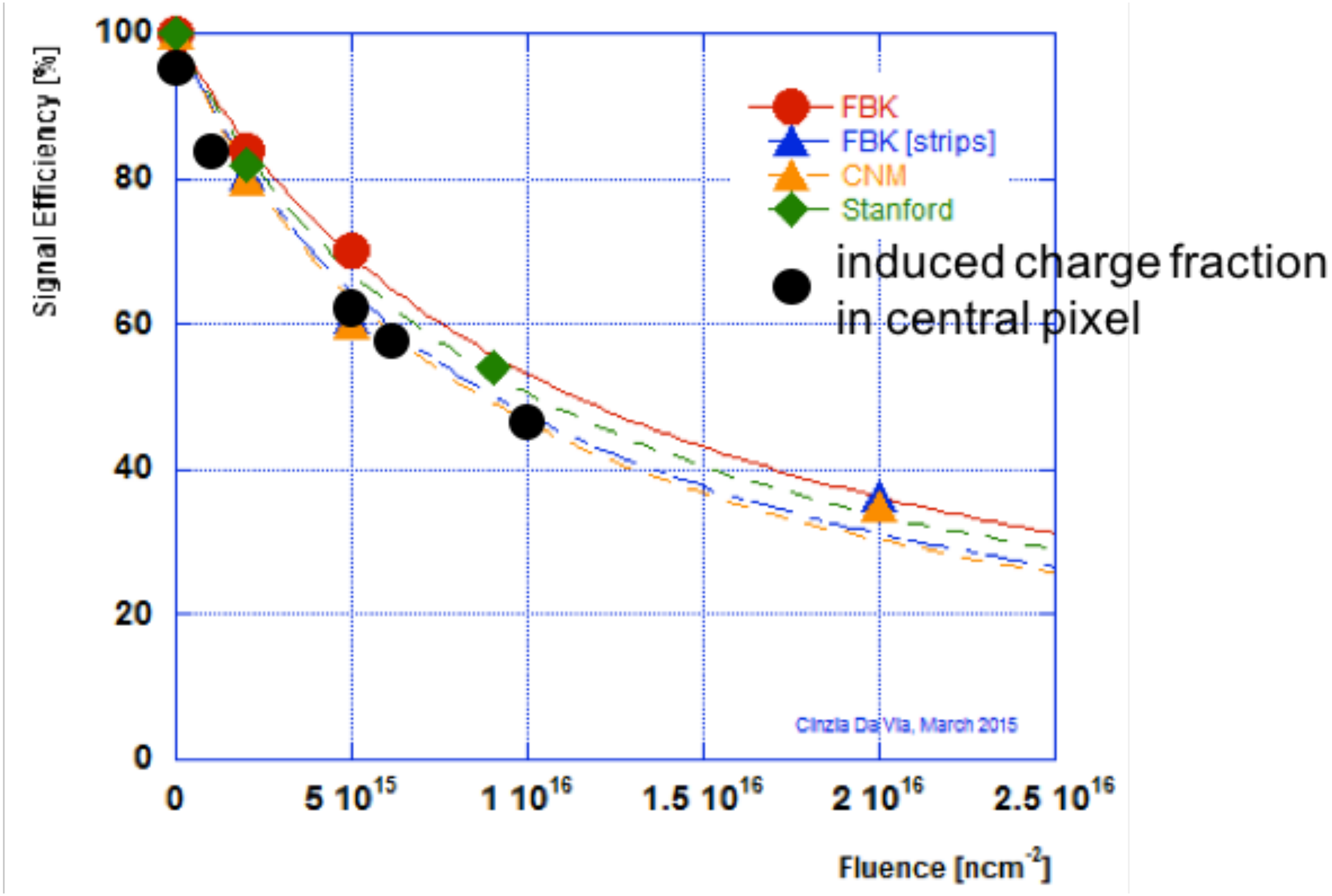
Negative signals induced on B by A with hits close to edge



Positive and negative signals induced on D by A with hits close to edge

Signal efficiency

G. Giugliarelli, UniUD



Conclusions

- Sensors from the 1st 3D-SS batch at FBK have shown very good results in terms of electrical characteristics, charge collection, and hit efficiency before irradiation
- From tests on 3D diodes and strips, the electrical characteristics are also very good after irradiation (in particular, large operation voltage range possible)
- Charge collection and hit efficiency to be assessed in irradiated devices
- Wafer layout for the 2nd batch ready, fabrication to start at FBK in February 2017
- Important progress with 3D sensor MC simulation