Waveform digitizing with fast analog memories developed by LAL & IRFU

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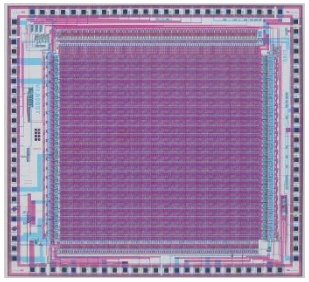
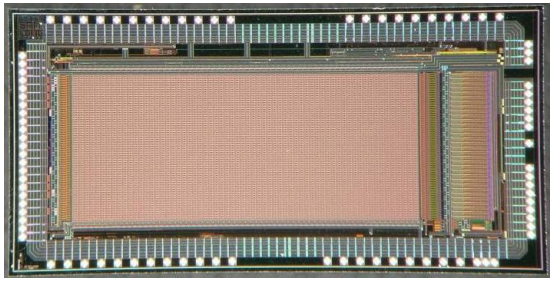
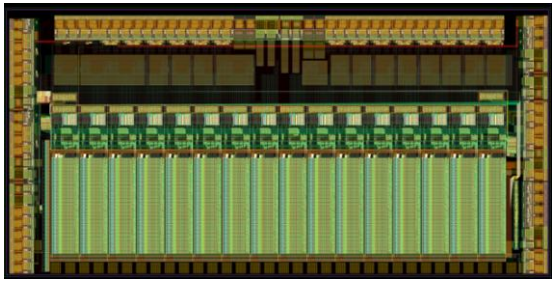
E.Delagnes, H.Grabas (CEA/IRFU)

Introduction

- Marlène asked me to present you today a panorama of our developments of fast digitizers based on analog memories

- These developments are for a big part based on requests from the projects of the community (nuclear, particle and astro-particle physics, medical imaging), but also the result of pure R&D (a great thanks to P2I/P2IO).

- A lot of the recent improvements in the systems I will present to you are the results of the rich and necessary feedback from users.

- We are still upgrading the existing elements (whenever possible) and keep developing new ones …

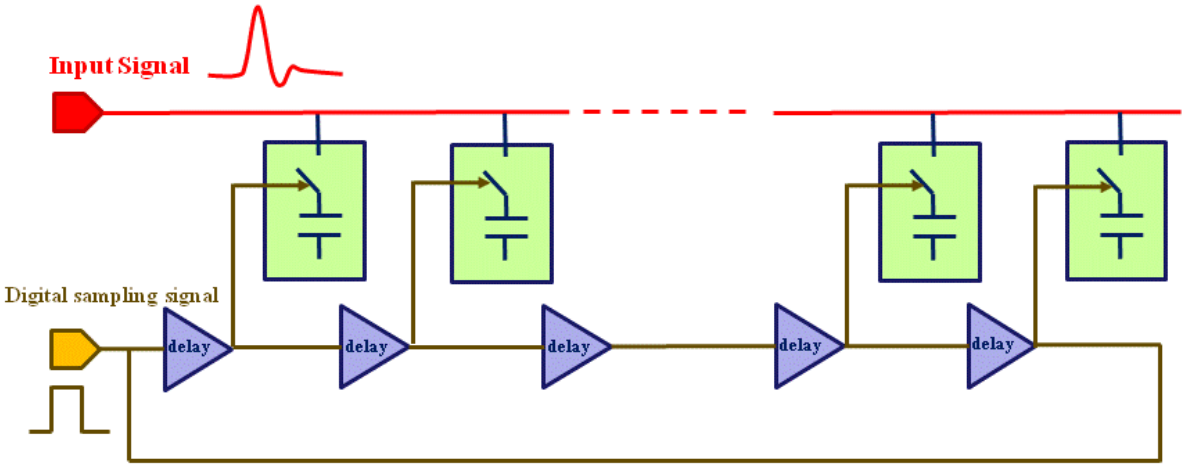
State of the art: digitization

- New trends in data acquisition are to digitize the signal as soon as possible in the chain and to perform a digital treatment of information
  - Waveform indeed contains all information (if properly digitized)
  - Depending on the information requested (amplitude, charge, time, FFT, …), different types of algorithms will be used
  - A very challenging goal has now become to find the simplest effective algorithms which could be integrated within companion FPGAs
  - Waveforms can be used for designing high performance TDCs
  - Signal to noise ratio is always an issue, even for a for TDC

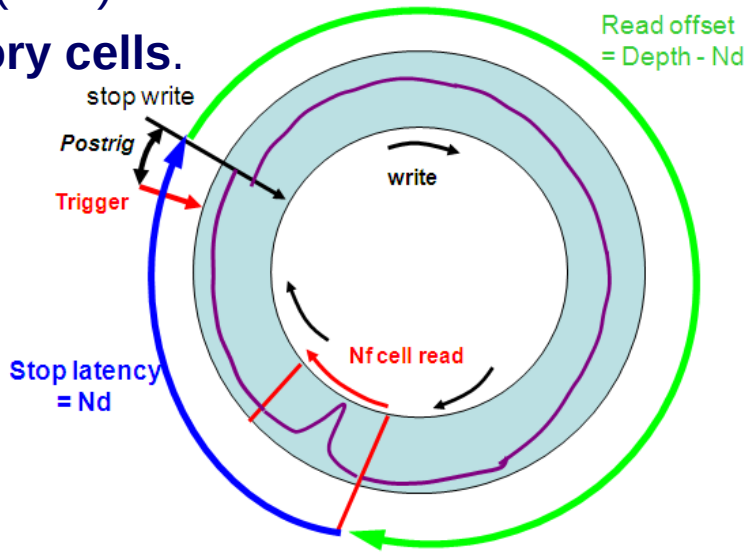
- In some cases, it is mandatory to use ADCs
  - When the trigger is performed on digitized data
  - When a constant data stream is necessary (even if the latter will end up in the companion FPGA) => real time FFT for instance
  - But whenever a short time window and a « reasonable » hit rate are present, analog memories really seem to be a good answer…

Circular analog memories: basic principles

An analog memory can record waveforms at very high sampling rate (>>GS/s)
After trigger, they are digitized at much lower rate with an ADC (5/10/20/… MHz)



- A write pulse is running along a folded **delay line** (DLL).
- It drives the recording of signal into **analog memory cells**.
- Sampling stops upon a **trigger signal**.
- **Readout** can target an area of interest, which can be only a **subset** of the whole channel
- **Dead time** due to readout should remain as small as possible.

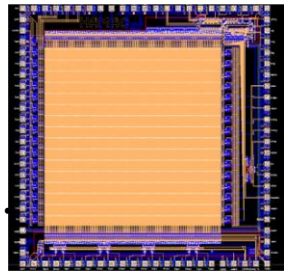


Our favourite solution: a Sampling Matrix

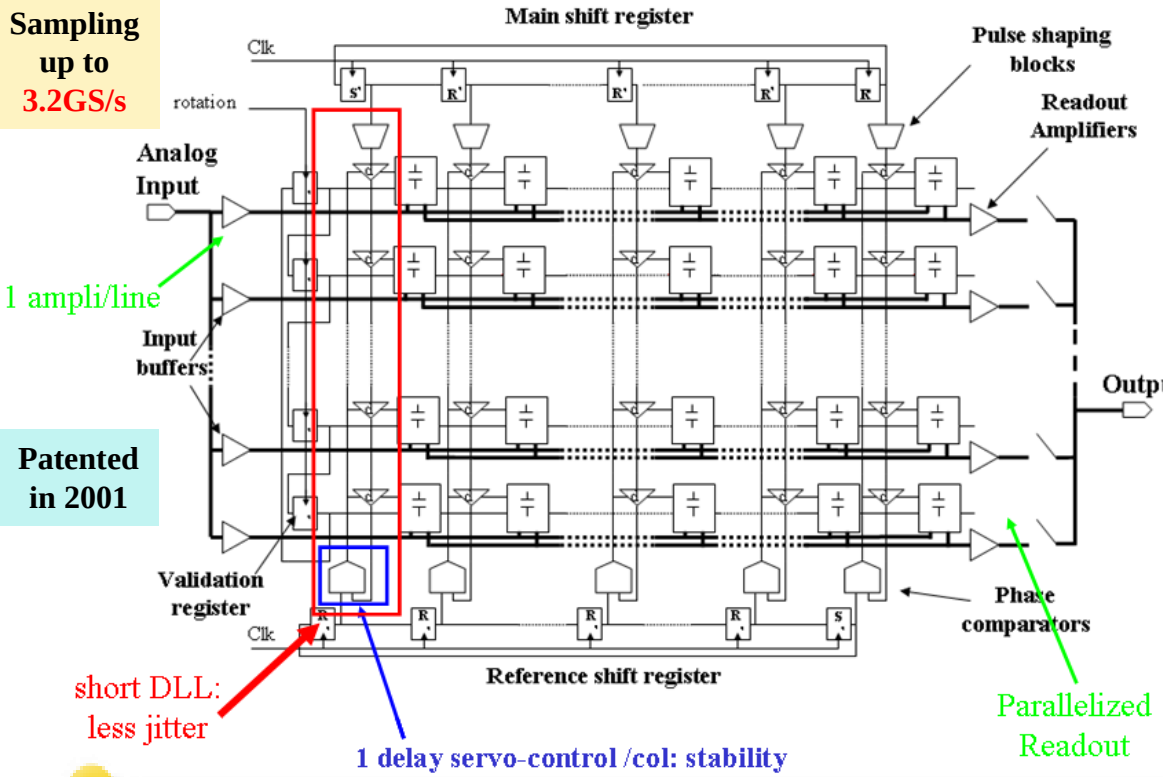
• We started designing analog memories in 1992 with the first prototype of the Switched Capacitor Array (SCA) for the ATLAS LARG calorimeter. 80,000 HAMAC chips produced in 2002 and mounted on the boards which **measured the Higgs energy**. They are still on duty on the LHC for long…

• Since 2002, many new generations of fast samplers have been designed (ARS, MATACQ, SAM/SAMLONG, SAMPIC): more than 50,000 chips in use.

HAMAC
1998-2002



Sampling up to 3.2GS/s

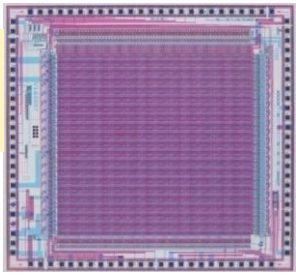


Readout 12/14 bits 5/10/20 MHz

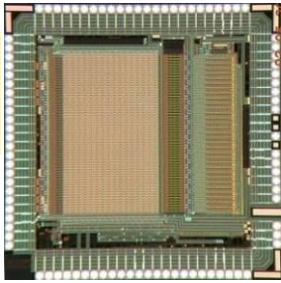
ADC

Patented in 2001

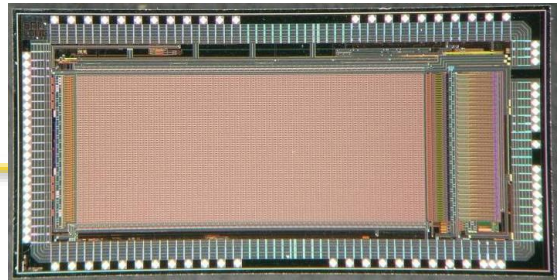
MATACQ
2000-2003



SAM
2005



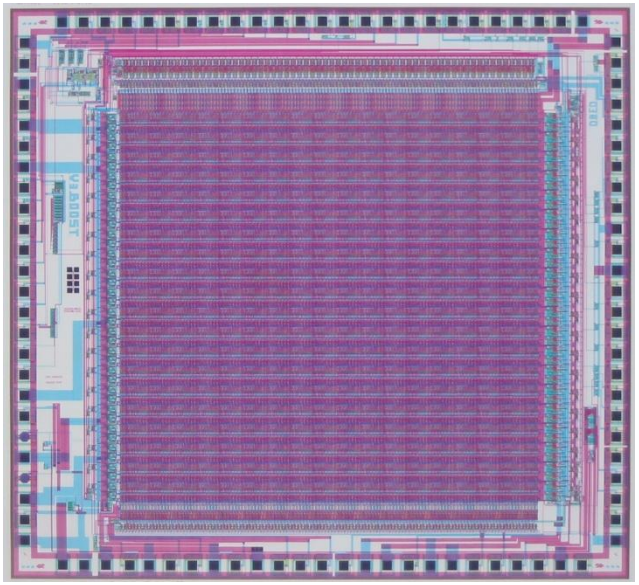
SAMLONG
2010-2012



Analog memories vs ADCs

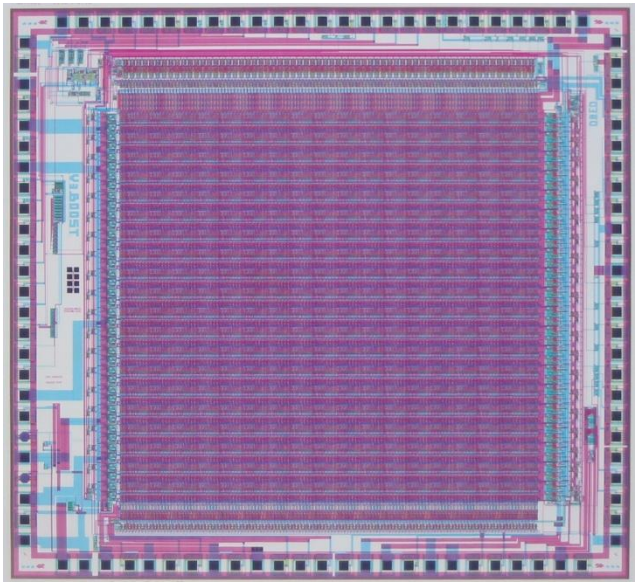
- **Analog memories** actually look like perfect candidates for **high precision measurements** at **large scale**:
  - Like ADCs they catch the signal waveform
  - TDC is built-in (position in the memory gives the time)
  - Only the useful information is digitized (vs ADCs) => **reduced dataflow and power**
  - Any type of digital post processing can be used
  - Main design difficulties: signal **bandwidth** and **integrity**
- Their drawbacks:
  - The limited recording **depth**
  - The readout **dead-time** limiting the input rate
- But:
  - Only a few samples/hit can be read => this may limit the dead time
  - **Simultaneous write/read** operation is feasible, which may further reduce the dead time

Board and system developments based on MATACQ.



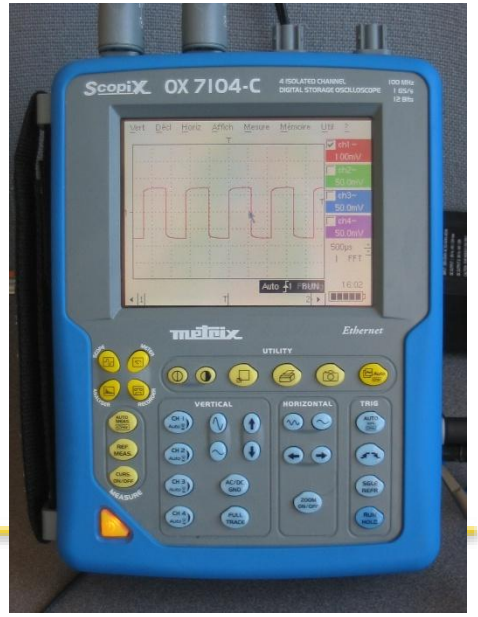
The MATACQ chip

- Technology: AMS CMOS 0.8µm
- First prototype submitted in November 1999.
- Final version submitted in 2003.
- **1 fully differential channel, 100M to 2GS/s, 300 MHz bandwidth, 2560 sampling cells, 14 bits of dynamic range, readout at 5 MHz**
- 1W @ 300MHz down to 0.25W @ 200 MHz



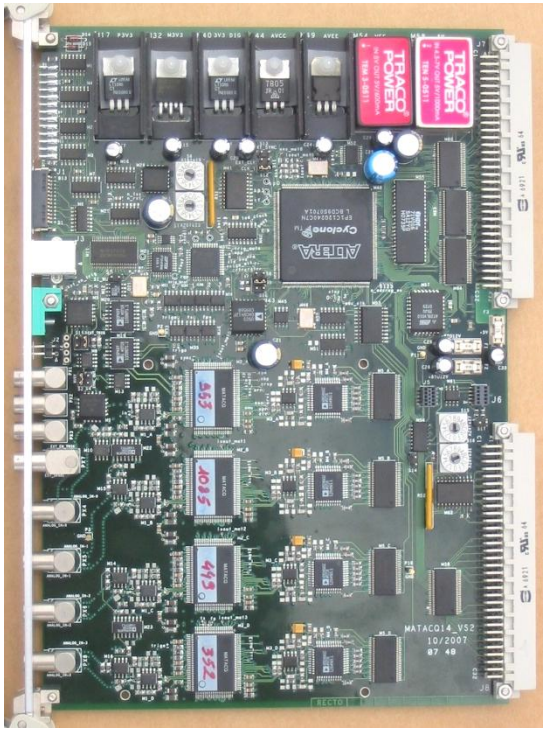
- Packaging: 100-pin PQFP, pitch of 0.5 mm

- Heart of the ScopiX oscilloscope series (still) commercialized by Chauvin-Arnoux since **2004**.

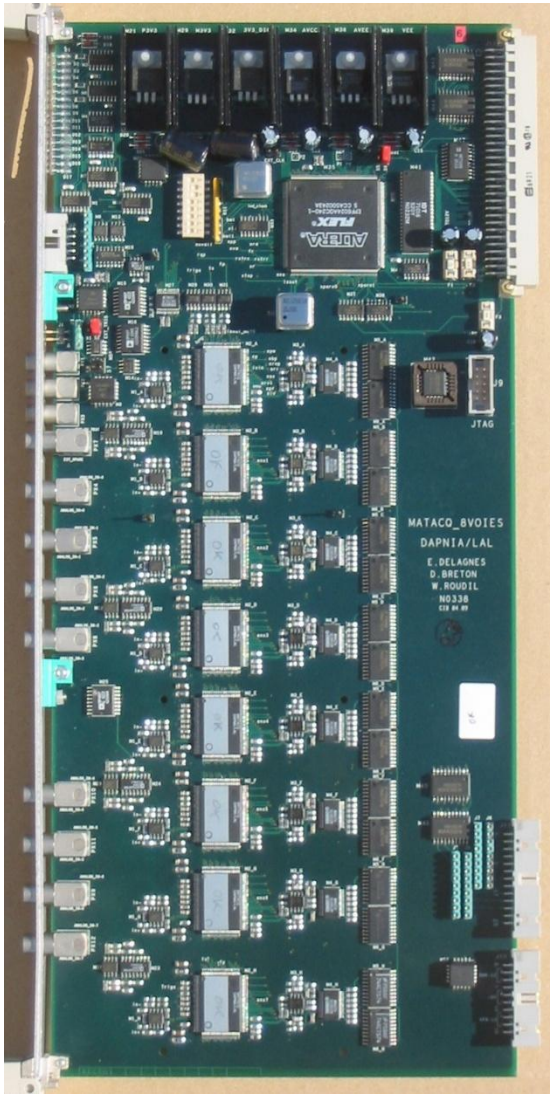


The MATACQ boards

12 bits / 4 channels



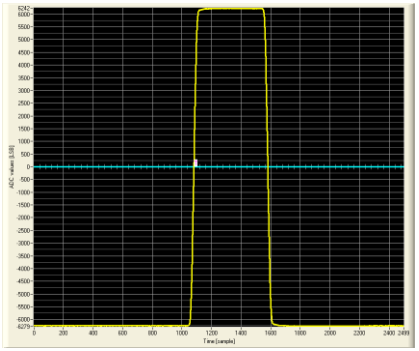
14 bits / 4 channels with USB



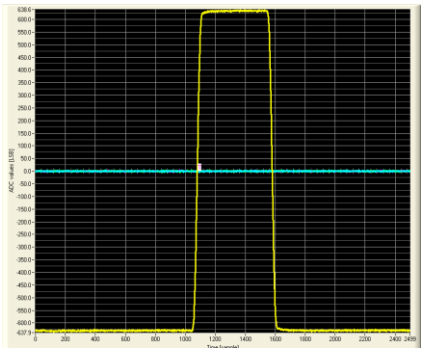
12 bits / 8 channels

- 3 main versions all with VME and GPIB interfaces.
- Used since 2005 at IPNO and GANIL.
- More than 250 boards produced.

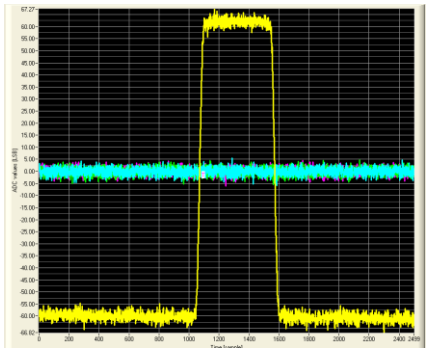
MATACQ board performances



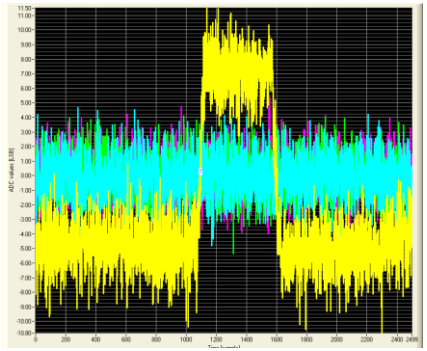
1.5 V pulse



Divided by 10

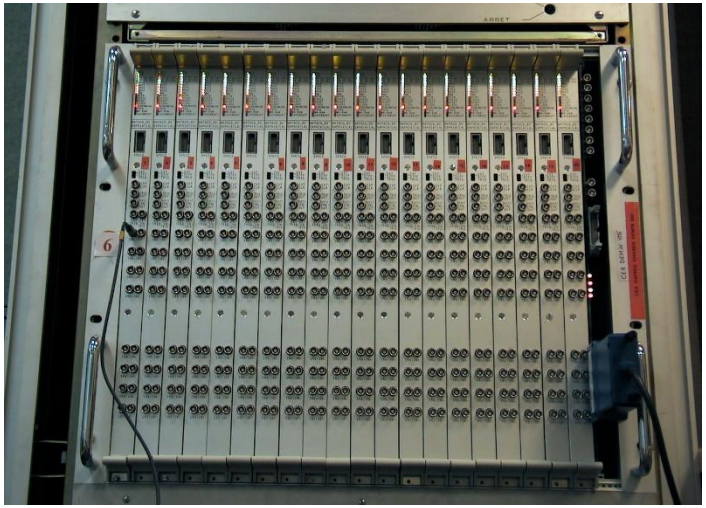


Divided by 100

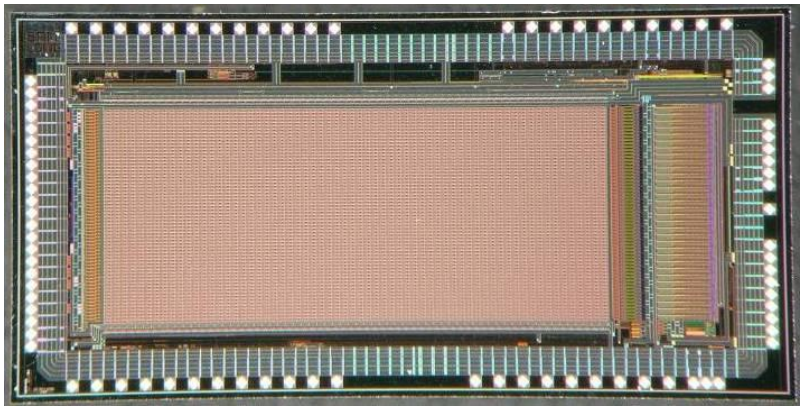


Divided by 1000

- 14-bit MATACQ board was perfectly adapted for wide range signals.
- 2V dynamic range, Noise level < 180 µV rms
- Readout @ 80Hz in GPIB, up to 500Hz in USB and 32-bit VME with block transfers
- Its main drawback was its conversion dead-time after trigger of 650 µs.



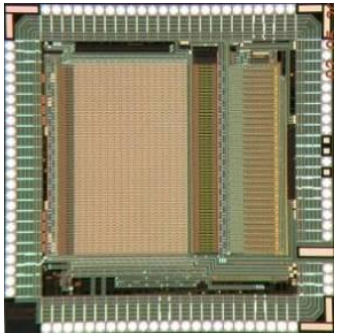
160 channels in a crate:
Omega @ Rochester (USA)



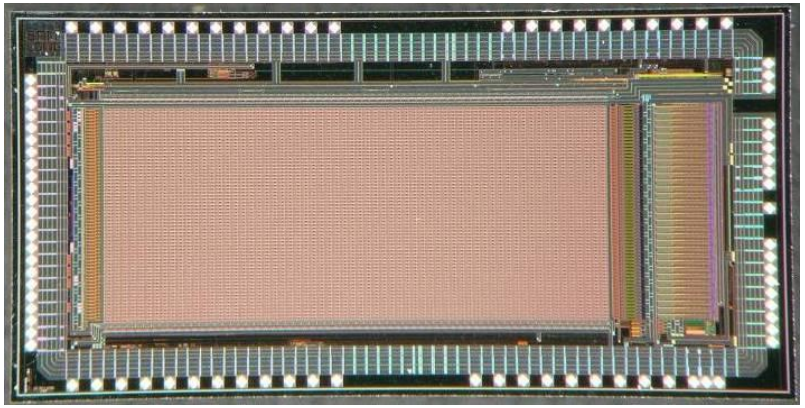
Board and system developments based on SAMLONG: The **WaveCatcher** Family

SAM & SAMLONG chips

- Technology: AMS CMOS 0.35µm
- SAM (2x256 cells) submitted in 2005 for HESS experiment.
- First version of SAMLONG submitted in 2010.
- Current version submitted in 2012.
- An updated version is discussed…
- **2 fully differential channels, 0.4 to 3.2GS/s, 500 MHz bandwidth, 1024 sampling cells, >12 bits of dynamic range, readout at 10 MHz (125 µs for the full waveform) or 20 MHz (66µs)**
- 300mW @ 500MHz down to 100mW @ 200 MHz
- Packaged in 100-pin PQFP, pitch of 0.5 mm



SAM



SAMLONG

The USB_WaveCatcher board (V6)

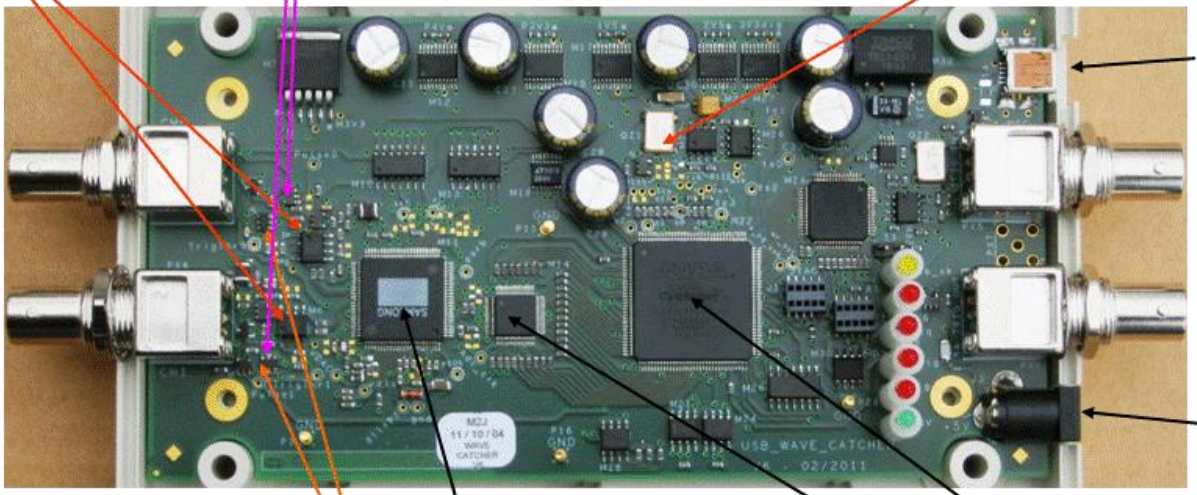
Pulsers for reflectometry applications

1.5 GHz BW amplifier.

Board has to be powered by USB
=> power consumption ≤ 2.5W

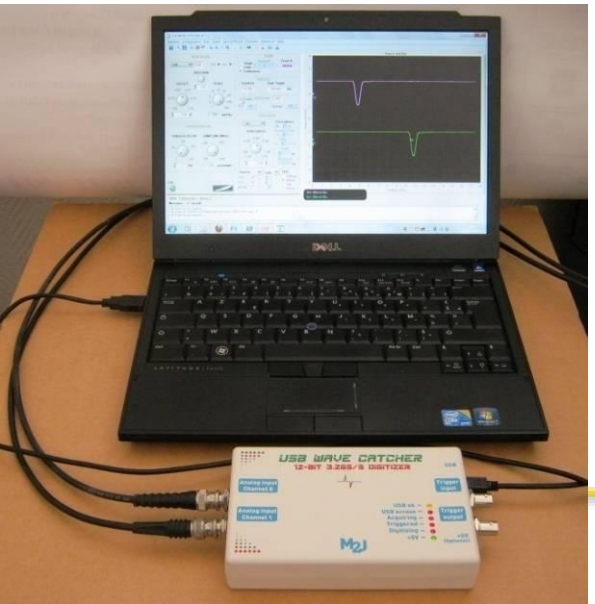
Reference clock:
200MHz => **3.2GS/s**

2008/2011



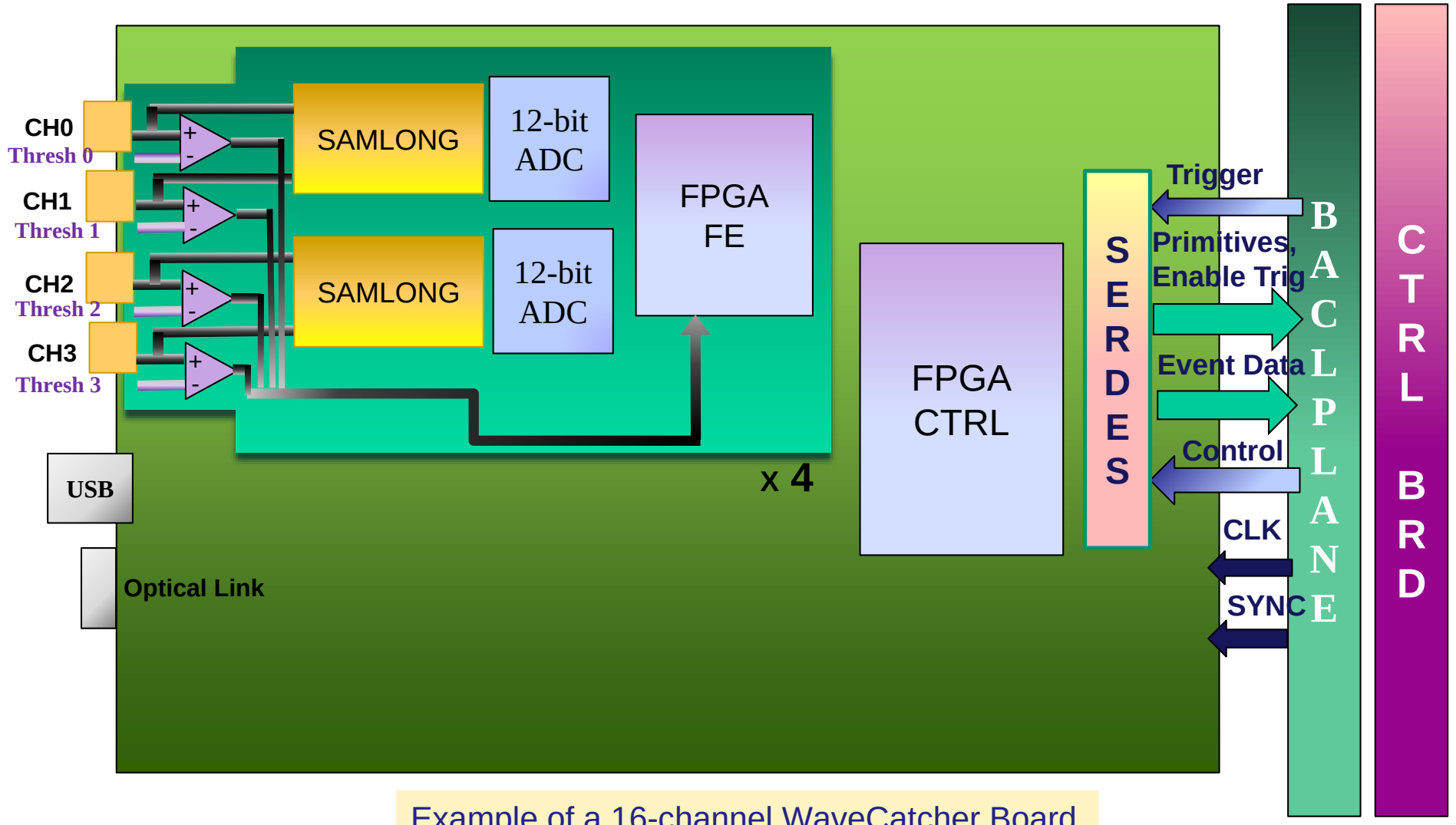
2 analog inputs. DC Coupled.

The autonomous test bench

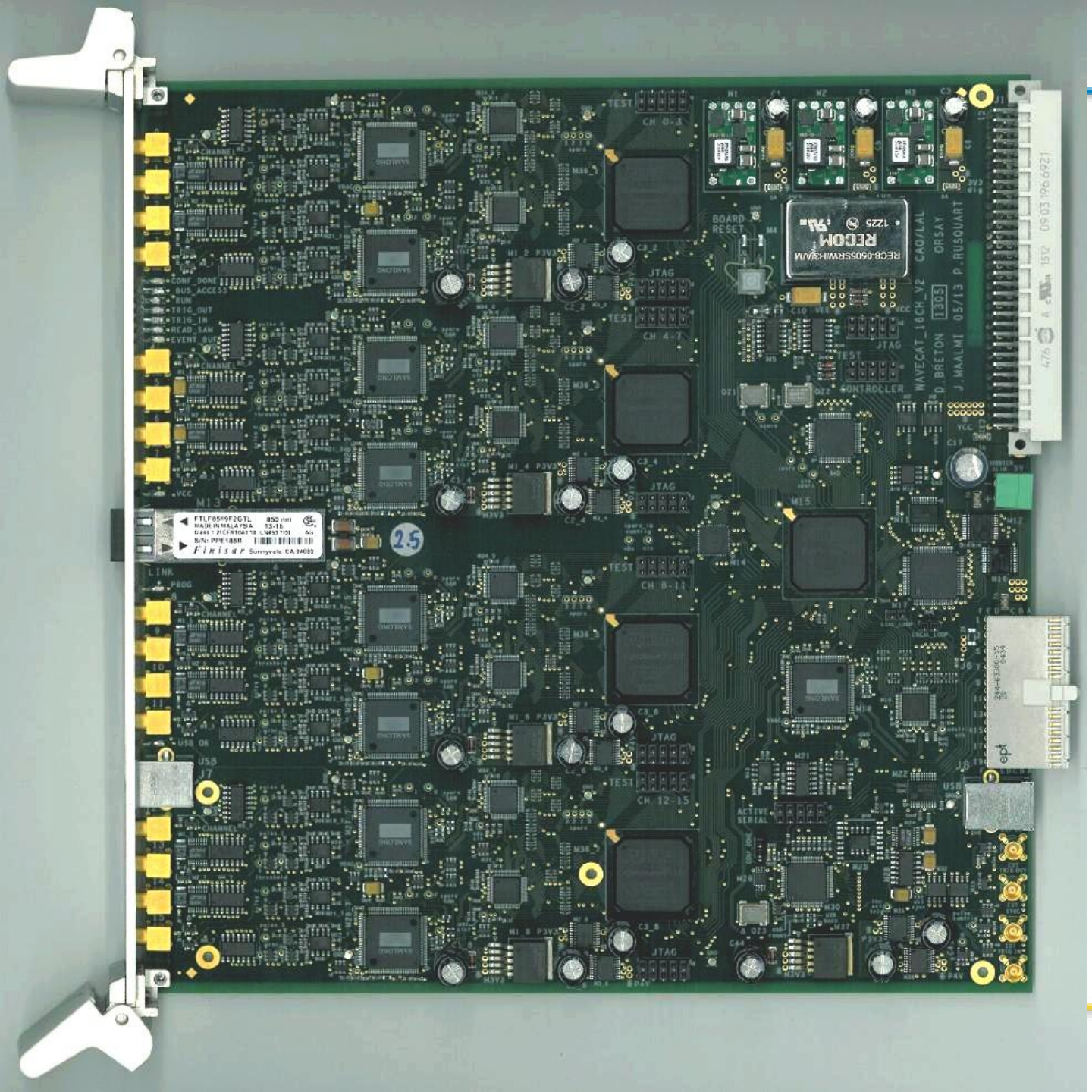


The historical 2-Channel module

WaveCatcher Front-End Block Diagram



Example of a 16-channel WaveCatcher Board



The 16/18-channel board

- 1.6mm thick
- 10 layers
- 233 x 220 mm²
- **3200 components**
- 25 power supplies (5 global, 20 local)

- Four **4-channel blocks** (can be used as **mezzanines** on other boards)

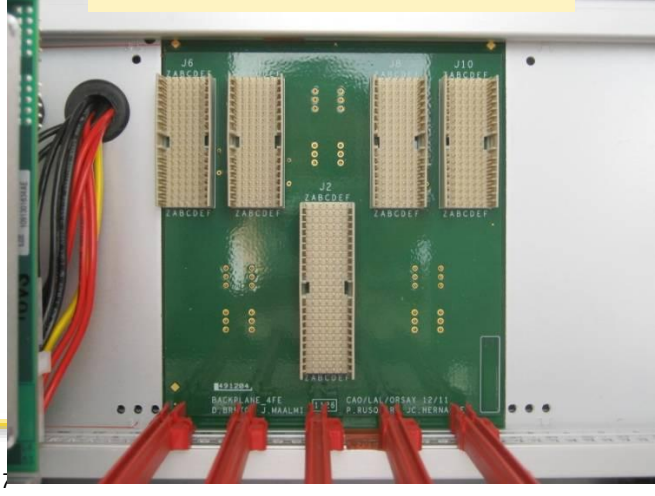
- **2 extra channels dedicated to « digital » signals**

The 64+8-channel digitizer

2013

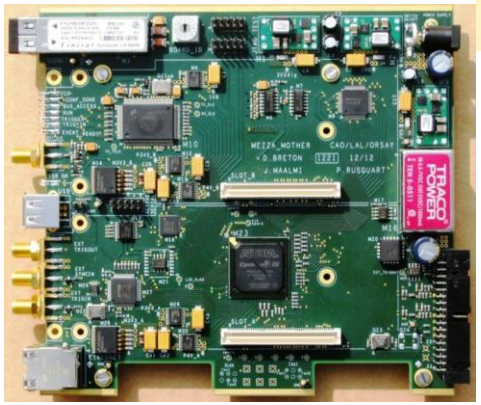
Up to 4
16-channel
boards

Custom backplane for
fast trigger & DAQ links



Controller board:
interface with
trigger and DAQ

The 8-channel and 16-channel modules



Motherboard

4-channel mezzanine

2014

x2

2016

- Autonomous plug and play desktops with USB (both) and secured Gbit UDP (8-channel) interfaces.
- 8-channel module is the most demanded.
- In constant firmware and software evolution thanks to users' feedback.

System features (not exhaustive)

- Possibility to add an **individual DC offset** on each channel
- **Individual trigger discriminator** on each channel
- Integrated **hit rate counter** on each channel
- External & internal trigger + many smart modes for **coïncidence triggering**
- **2 extra memory channels** for « digital » signals on 16-channel board => **can be used as additional analog inputs**
- One individual **pulse generator** on each input
- **External clock** input for multi-board applications (8, 16 & 64-channel)
- Embedded **USB,** and **secured Gbit UDP** (8 & 64-channel)
- Possibility to upgrade the firmware via **USB**
- **Embedded feature extraction** (see next slide)

Feature extraction by firmware (1)

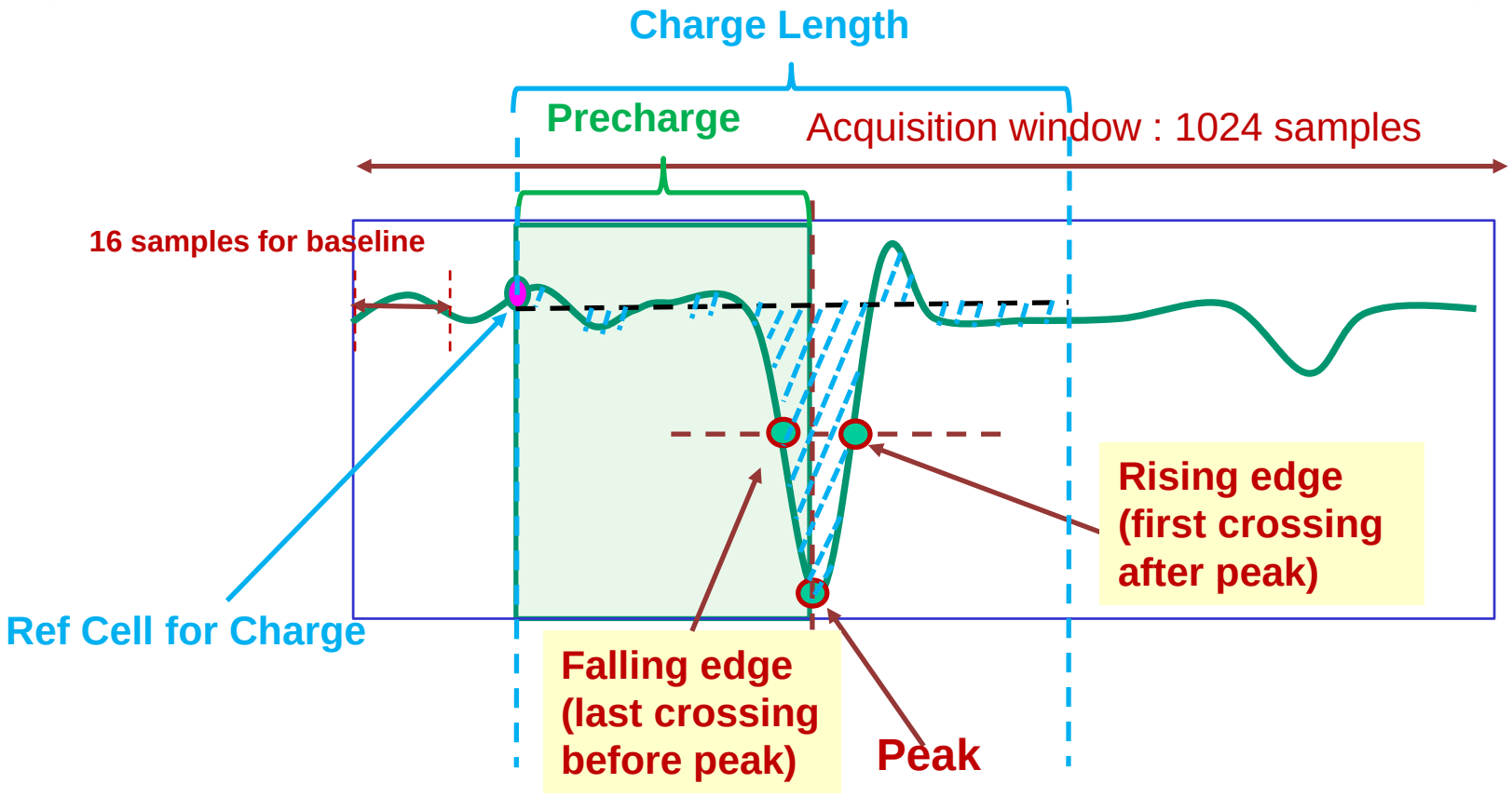
- **The very good level of performance of the SAMLONG chip without external correction permits implementing an effective on-the-fly calculation directly on the board (in its companion FPGA)** :

  This information is extracted from raw data directly coming from SAMLONG (after factory on-chip adjustment of the line offsets)

  - **Baseline** (16 bits)
  - **Peak** (16 bits)
  - **Peak time** (10 bits)
  - **Charge** (23 bits)
  - Real Digital CFD on Rising and Falling edge Time: (18 bits: bin of **1.22 ps**)
  - **Absolute Time**: given by the FPGA **40-bit TDC timestamp**

- When using the extracted parameters**, waveform transmission can be suppressed,** thus permitting **very high trigger rates (up to 30 kHz for 8 channels with reduced sampling depth)**

Feature extraction by firmware (2)



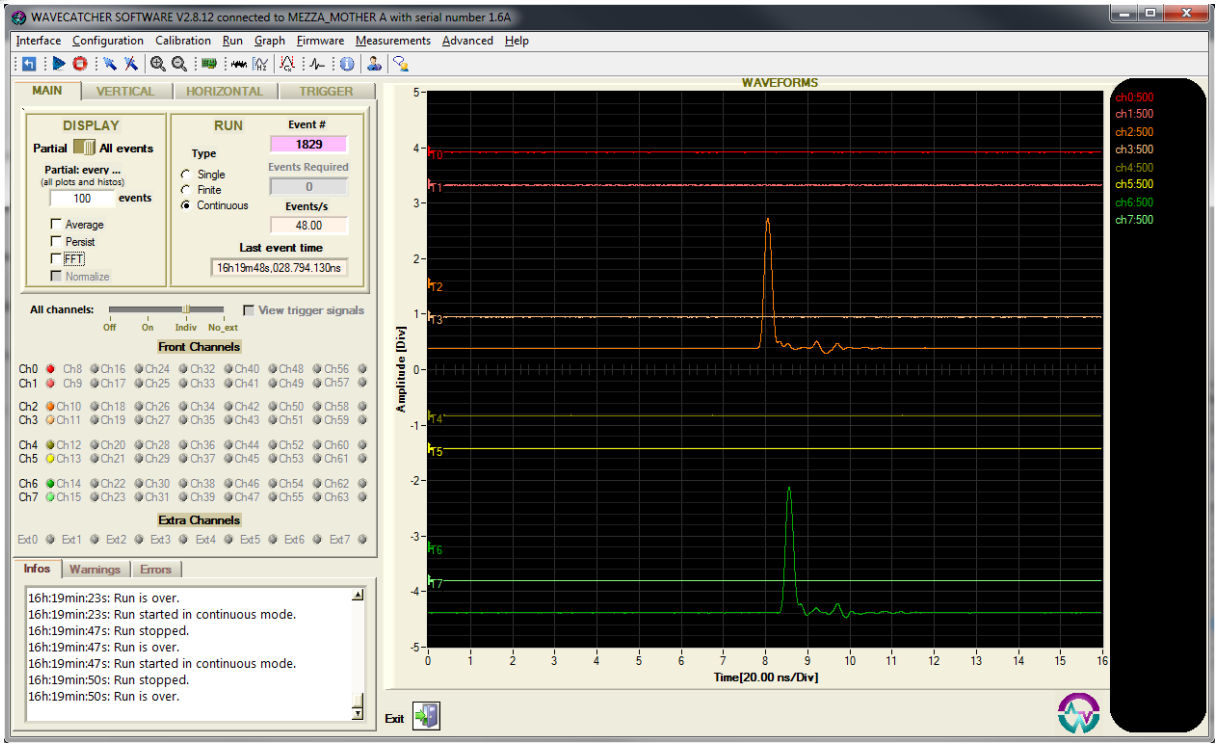
Programmable options :

- Peak polarity: Pos/Neg
- Forced/Extracted baseline
- CFD/Fixed Threshold
- CFD ratio (steps of 1/16)

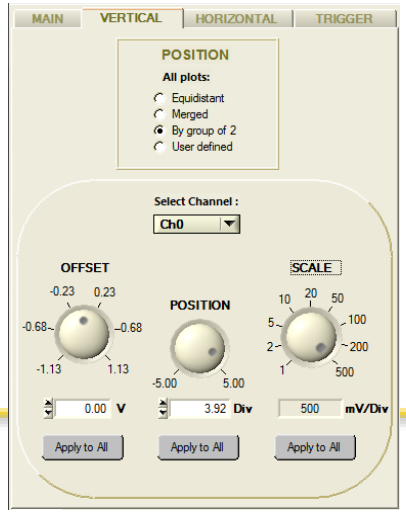
Charge Options :

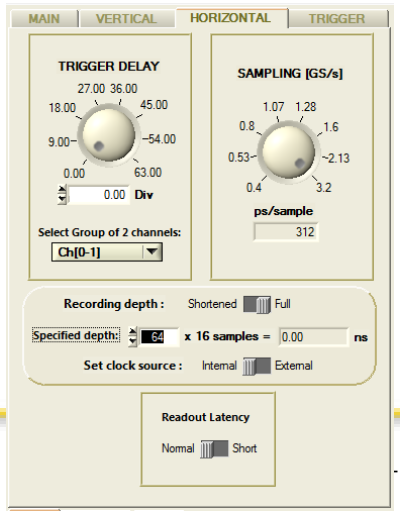
- Start from **Ref cell for Charge** or from **(Peak – Precharge)**
- PreCharge
- Ref Cell for Charge
- Charge Length

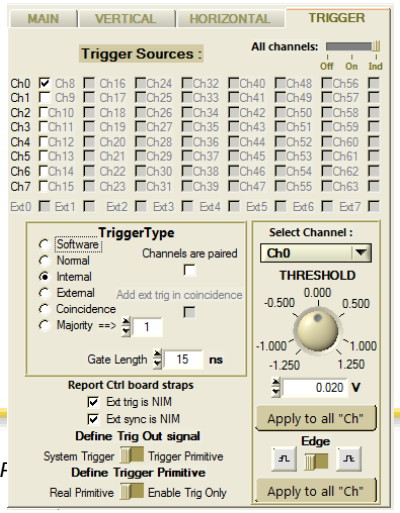
The WaveCatcher software



Main panel: oscilloscope like, but up to 64 channels !

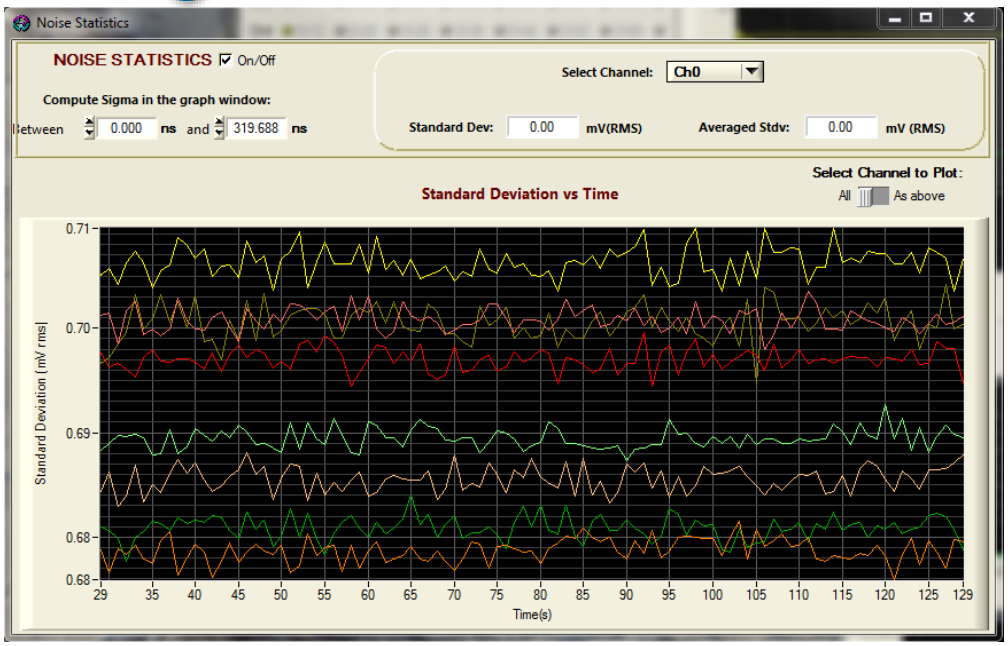






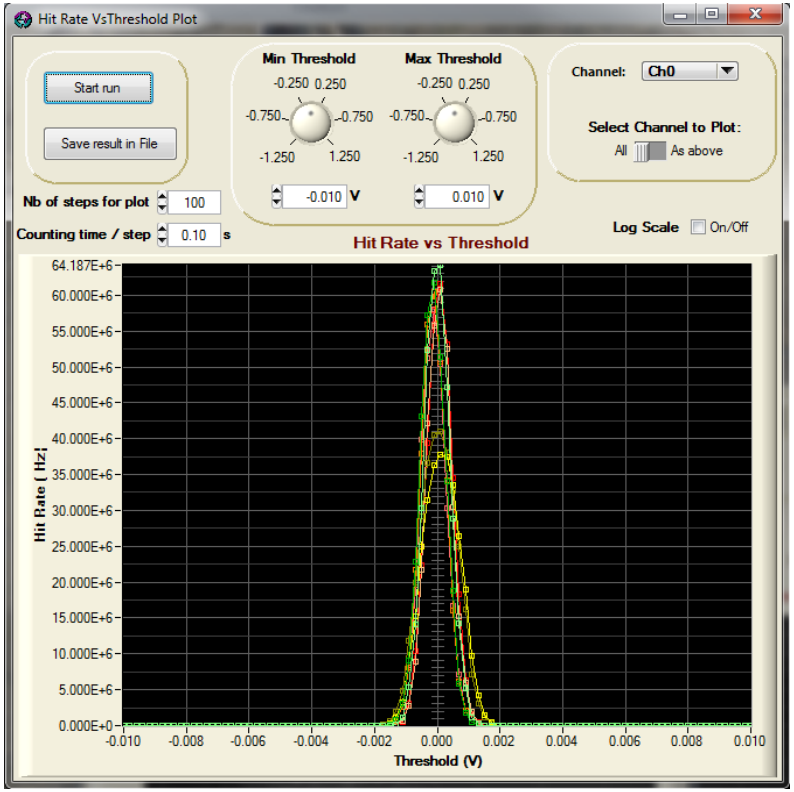
Vertical, Horizontal, and Trigger panels

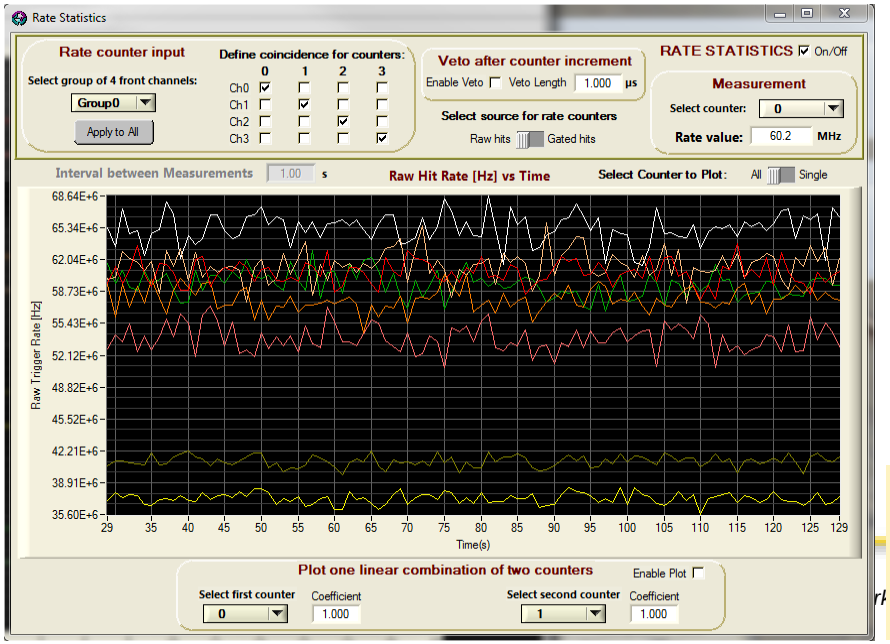
Real-time measurement display (1)



Noise statistics panel

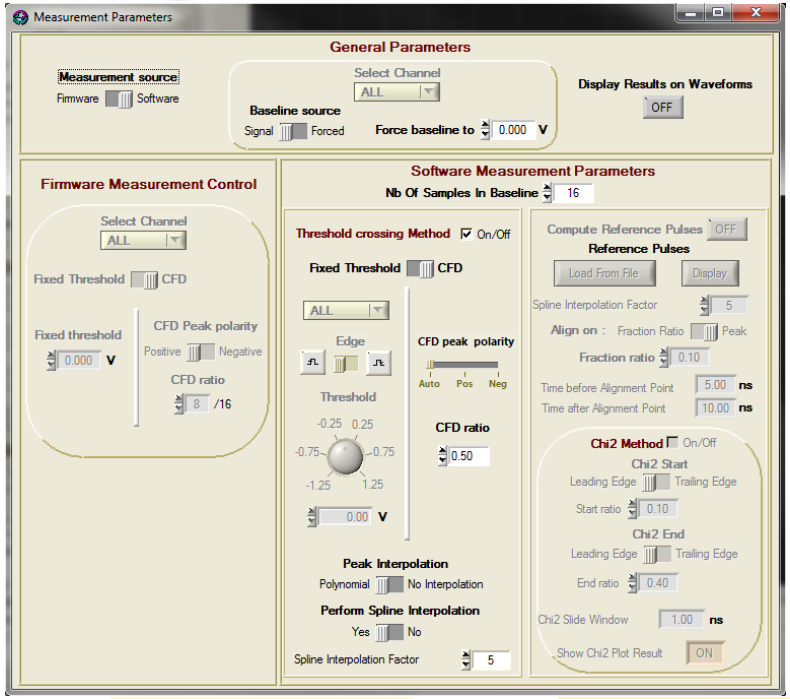
Rate vs Threshold plot





Rate statistics panel

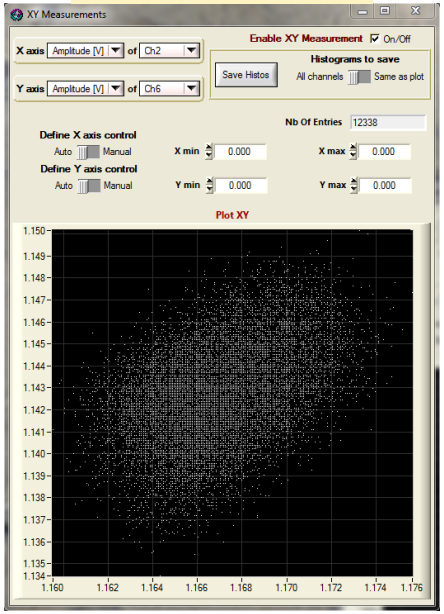
Real-time measurement display (2)



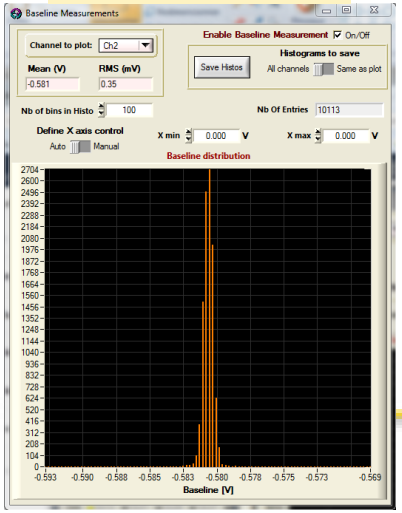
Measurement parameters panel

- Software also comprises a powerful time measurement panel (next slide)

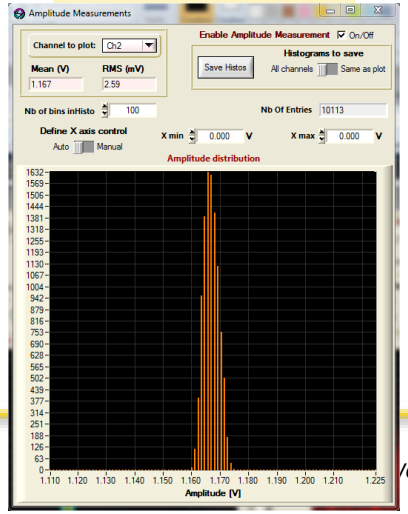
XY plot



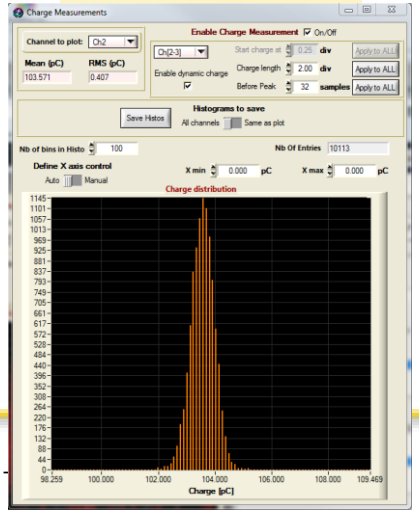
Baseline



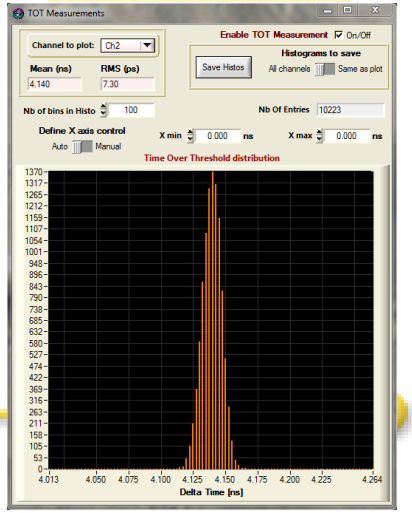
Amplitude



Charge



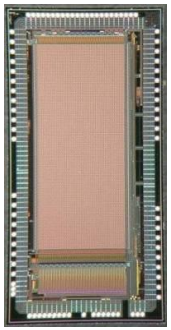
TOT



Jitter results with WaveCatchers

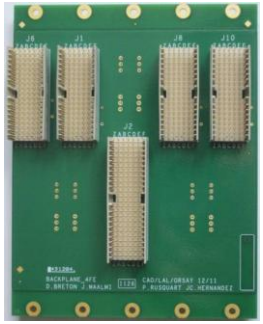
Delays are performed with cables to limit jitter. Trigger on signals.

- **Design difficulty here is the use of a backplane to distribute the clock.**
  - Central control board is the source of the 200 MHz clock

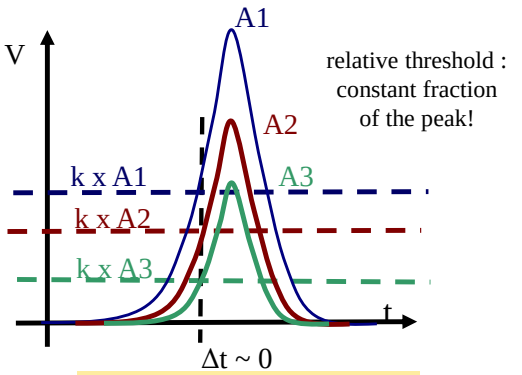


Ch0-Ch1

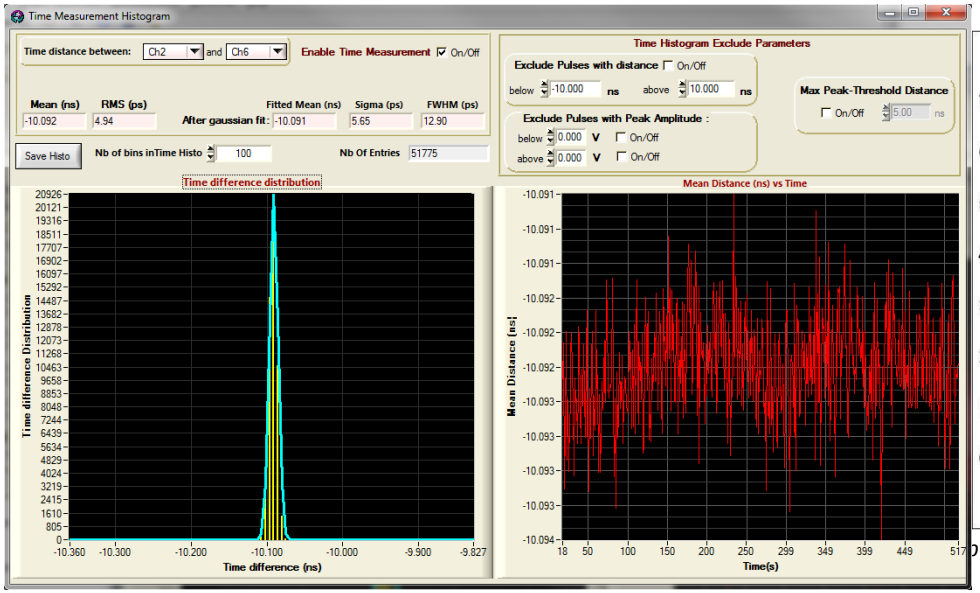
Ch0-Ch4

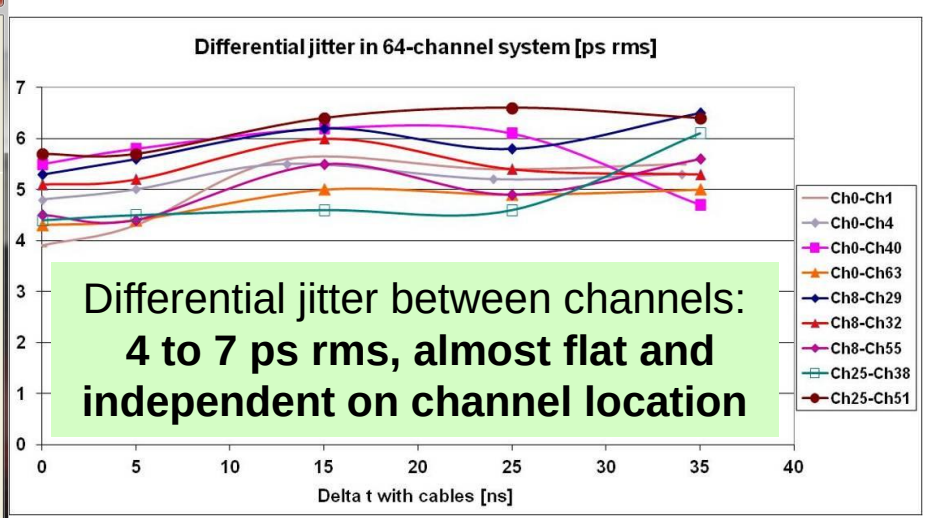


All other pairs



Constant Fraction Discriminator





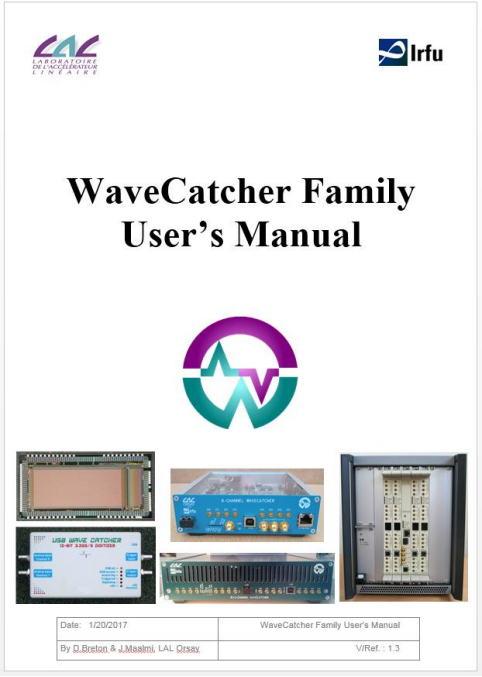
Differential jitter between channels:
4 to 7 ps rms, almost flat and independent on channel location

WaveCatcher: Performance Summary

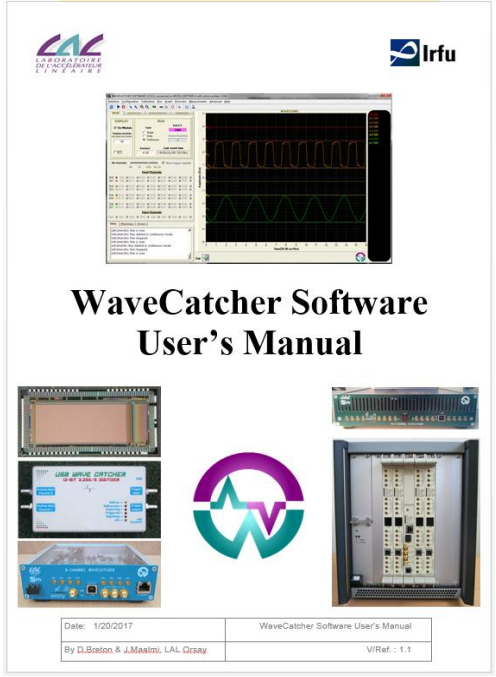
		Unit
SCA Technology	AMS CMOS 0.35µm	
SCA Number of channels	2	
SCA power consumption (max)	400 (3.3V supply)	mW
SCA noise	< 700	µV rms
SCA depth	1024	Cells
Sampling speed	0.4 to 3.2	GSPS
Bandwidth	500	MHz
Range (unipolar)	± 1.25	V
ADC resolution	12	bits
Total noise	< 700	µV rms
Dynamic range	~ 11.7	bits rms
Conversion time for full waveform (1024 samples)	125 (66 in fast mode)	µs
Readout capacity	30 (USB), > 100 (UDP)	Mbytes/s
Single Pulse Time precision before correction	~ 15	ps rms
Single Pulse Time precision after time INL correction	~ 3.5	ps rms

WaveCatcher documentation.

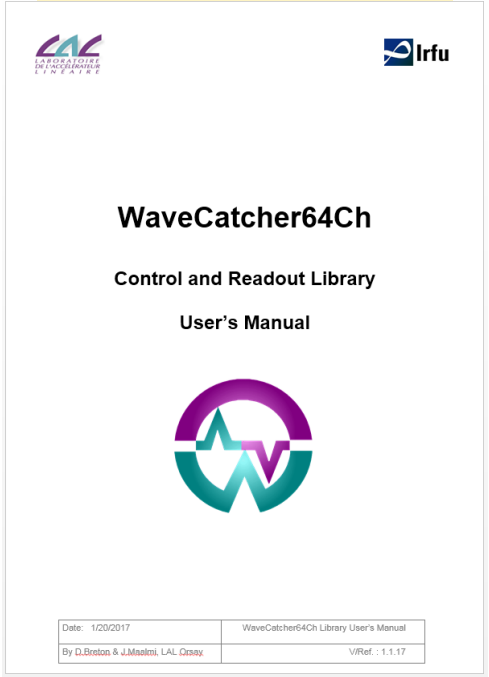
Hardware



Control & Readout software



C Library (Windows & Linux)



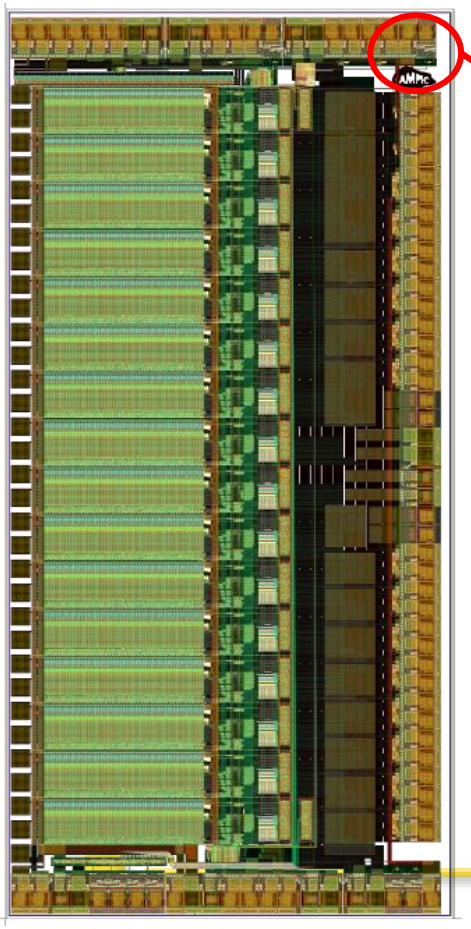
https://owncloud.lal.in2p3.fr/public.php?service=files&t=56e4a2c53a991cb08f73d03f1ce58ba2

Used worldwide by many projects, universities, labs and companies
(BiPo, SUPERNEMO, Codalema, CORTO, UA9, IRFU, CERN, INFN, PSI, BNL, Rochester, SLAC, Osaka, Barcelona, Dublin, LPSC, IPNO, IPHC, APC, CENBG, IMNC, Subatech, Nançay, Ganil, Cadarache, SENSL, GE, Hamamatsu, Solayl, PHIL, Eli_NP, ThomX, SHIP, …).

Both hardware and software have been valorized and CAEN sells under license the corresponding X743 family (see backup slide), as well as M2J (2-channel module).

Let's introduce SAMPIC ...

- SAMPIC presents an innovative architecture
- But first, why the hedgehog ?
- SAMPIC (Sampling Analog Memory for PICosecond timing)



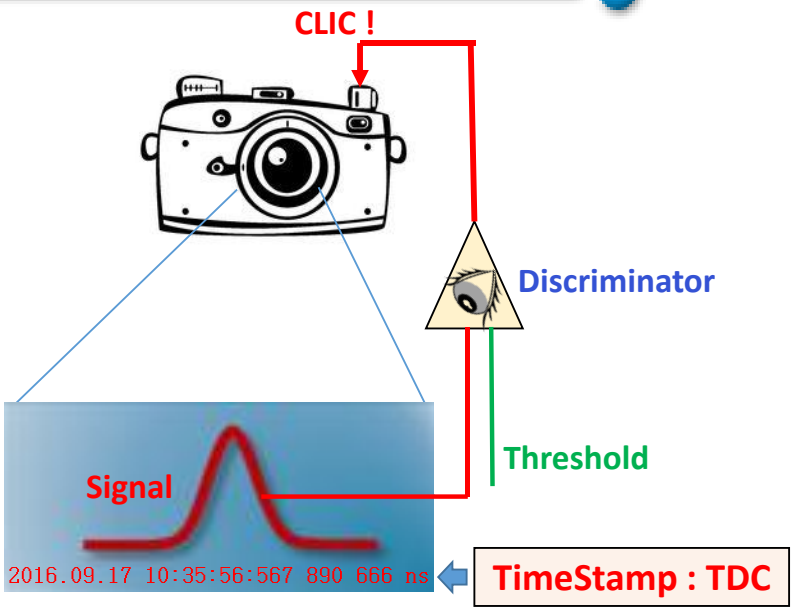
=> "ça me pique"

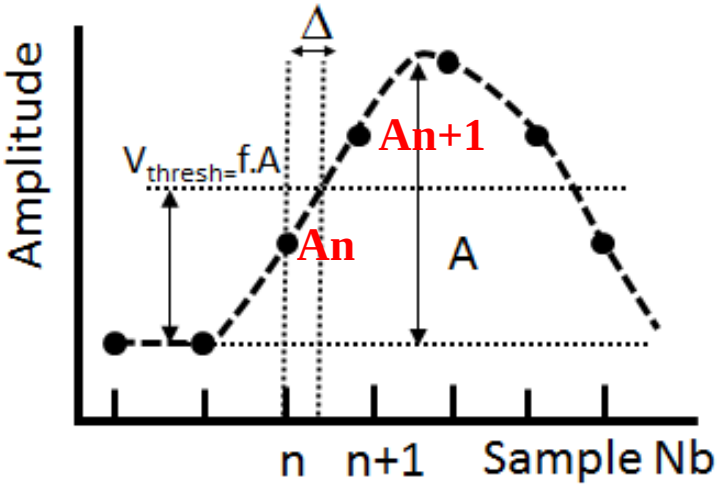
=> "That pricks me"

The « Waveform TDC » Concept (WTDC)

WTDC: a TDC which permits taking a picture of the signal. This is done via sampling and digitizing only the interesting part of the signal.

Based on the digitized samples, making use of interpolation by a digital algorithm, fine time information will be extracted.





$t_0 = (n + \Delta) * T_s$ with $\Delta = \frac{f*A - A_n}{A_{n+1} - A_n}$

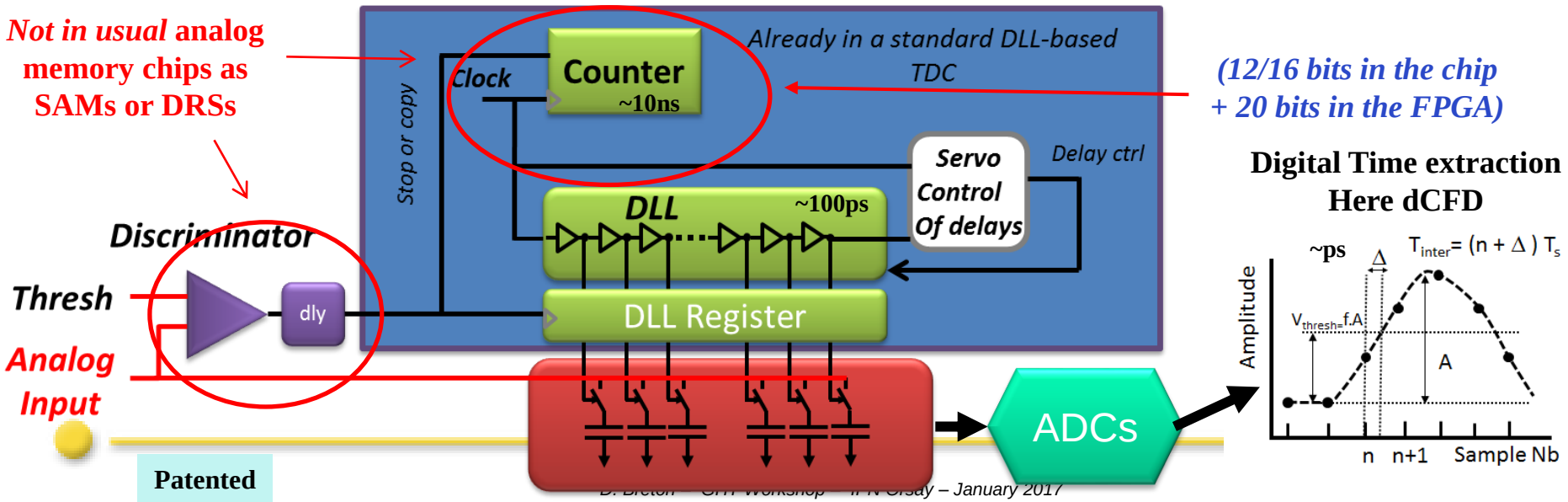
- **Advantages:**
  - **Time resolution ~ few ps**
  - **No "time walk" effect**
  - **Possibility to extract other signal features: charge, amplitude…**
- **Drawbacks:**
  - **dead-time linked to conversion and readout which doesn't permit counting rates as high as with a classical TDC**

The « Waveform TDC » structure

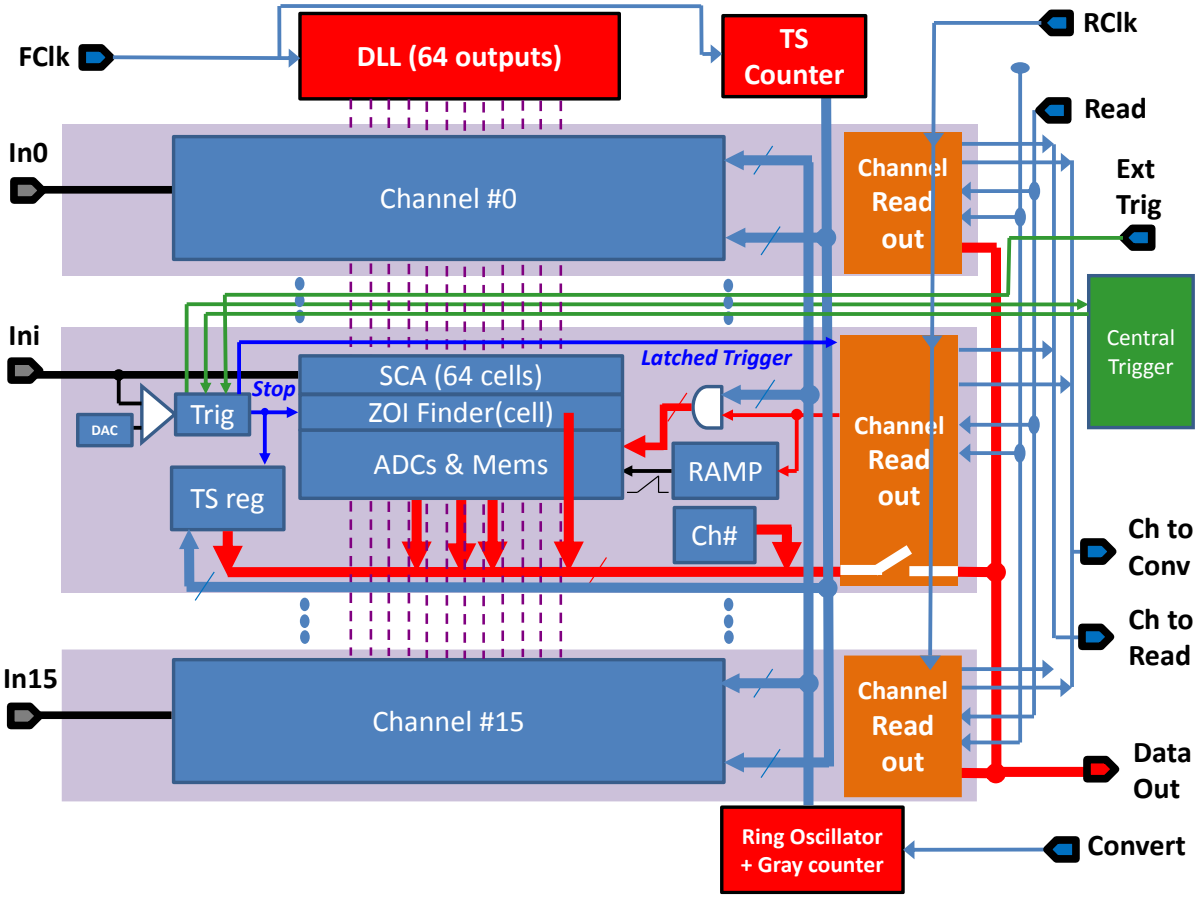
- Overall time information is obtained by combining 3 times :
  - **Coarse** = Timestamp Gray Counter (few ns step)
  - **Medium** = DLL locked on the clock to define region of interest (~100 ps step)
  - **Fine** = samples of the waveform (**digital algorithm** will give a precision of a few ps)

TDC

- **Discriminator is used only for triggering, not for timing => no jitter added on measurement, low power**
- **Digitized waveform available to extract other parameters (Q, amplitude,…)**



Global architecture of SAMPIC



- **One Common 16-bit Gray Counter** (FClk up to 160MHz) for **Coarse Timestamping**.

- **One Common servo-controlled DLL**: (from 1.6 to 10.2 GS/s) used **for medium precision timing & analog sampling**

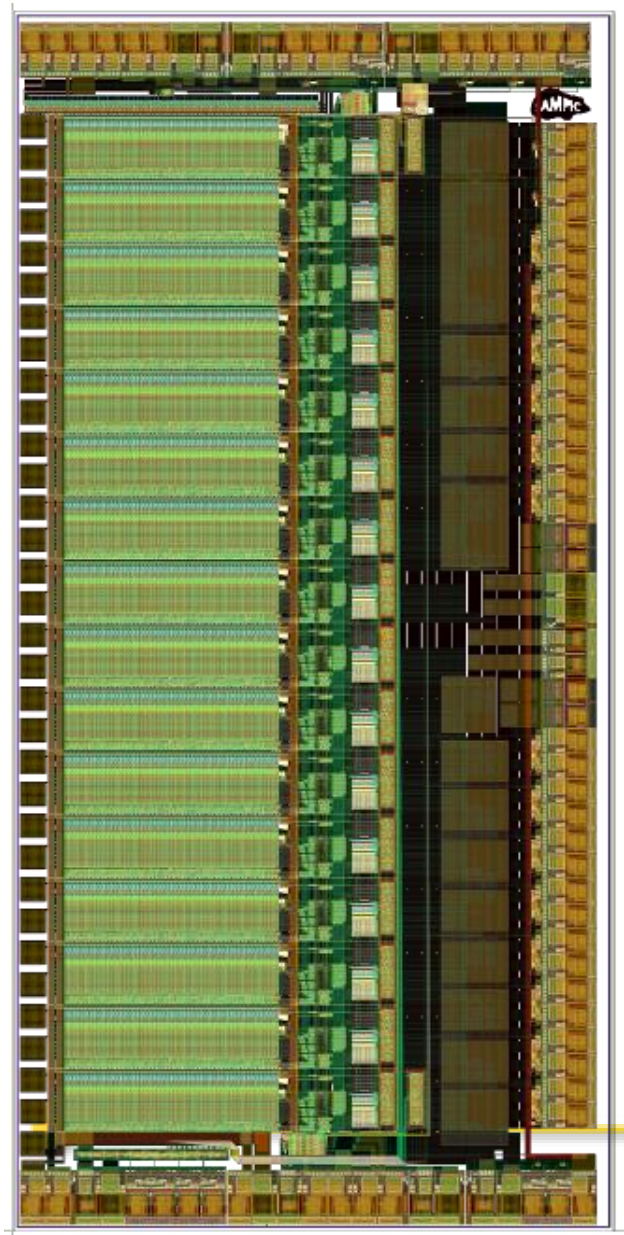
- **16 independent WTDC channels each with :**
  - ✓1 discriminator for self triggering
  - ✓Registers to store the timestamps
  - ✓64-cell deep SCA analog memory
  - ✓One 11-bit ADC/ cell

  (Total : 64 x 16 = 1024 on-chip ADCs)

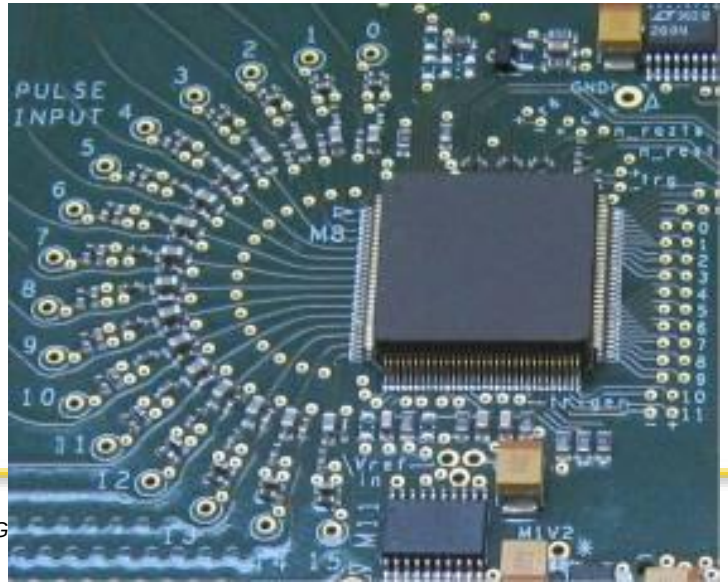
- **One** common 1.3 GHz oscillator + counter used as timebase for all the **Wilkinson A to D converters**.

- **Read-Out interface: 12-bit LVDS bus running at > 160 MHz (2 Gbits/s)**
- **SPI Link** for Slow Control

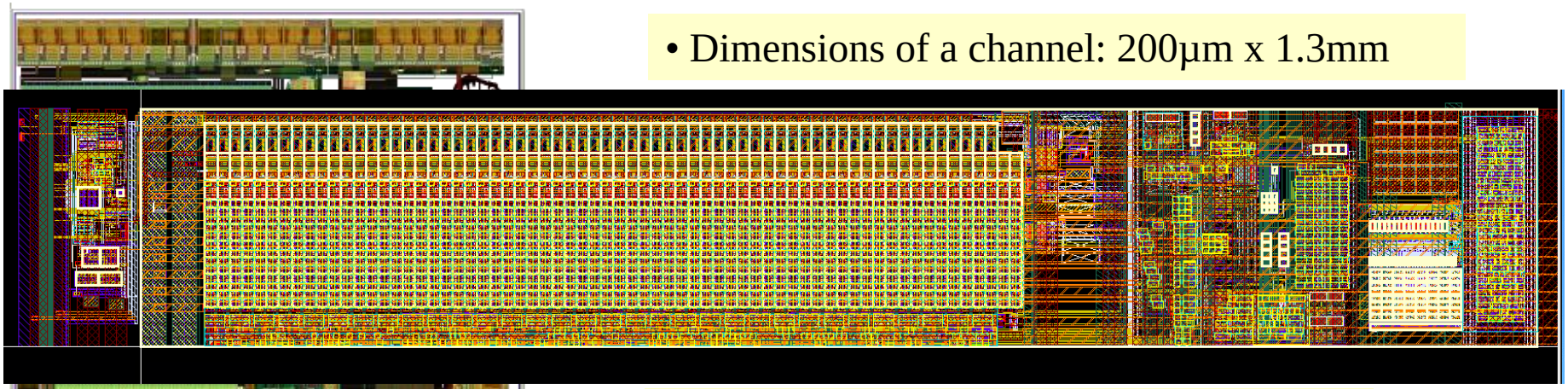
SAMPIC layout



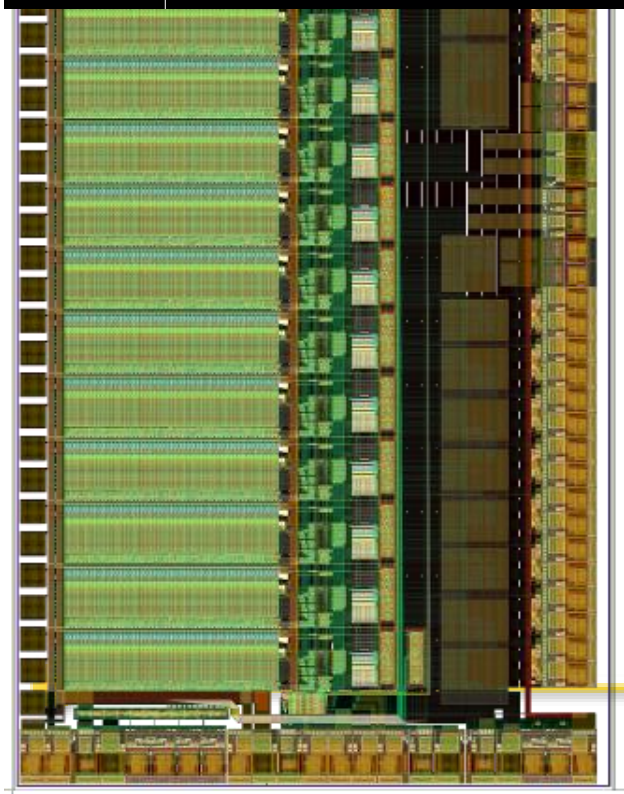
- Technology: AMS CMOS 0.18µm
- Surface: 8 mm^2
- Package: QFP 128 pins, pitch of 0.4 mm



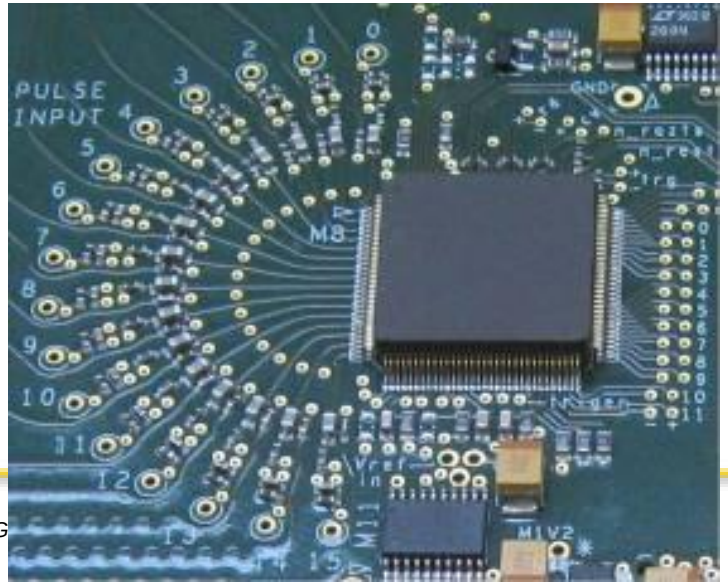
SAMPIC layout



- Dimensions of a channel: 200µm x 1.3mm



- Technology: AMS CMOS 0.18µm
- Surface: 8 mm^2
- Package: QFP 128 pins, step of 0.4mm

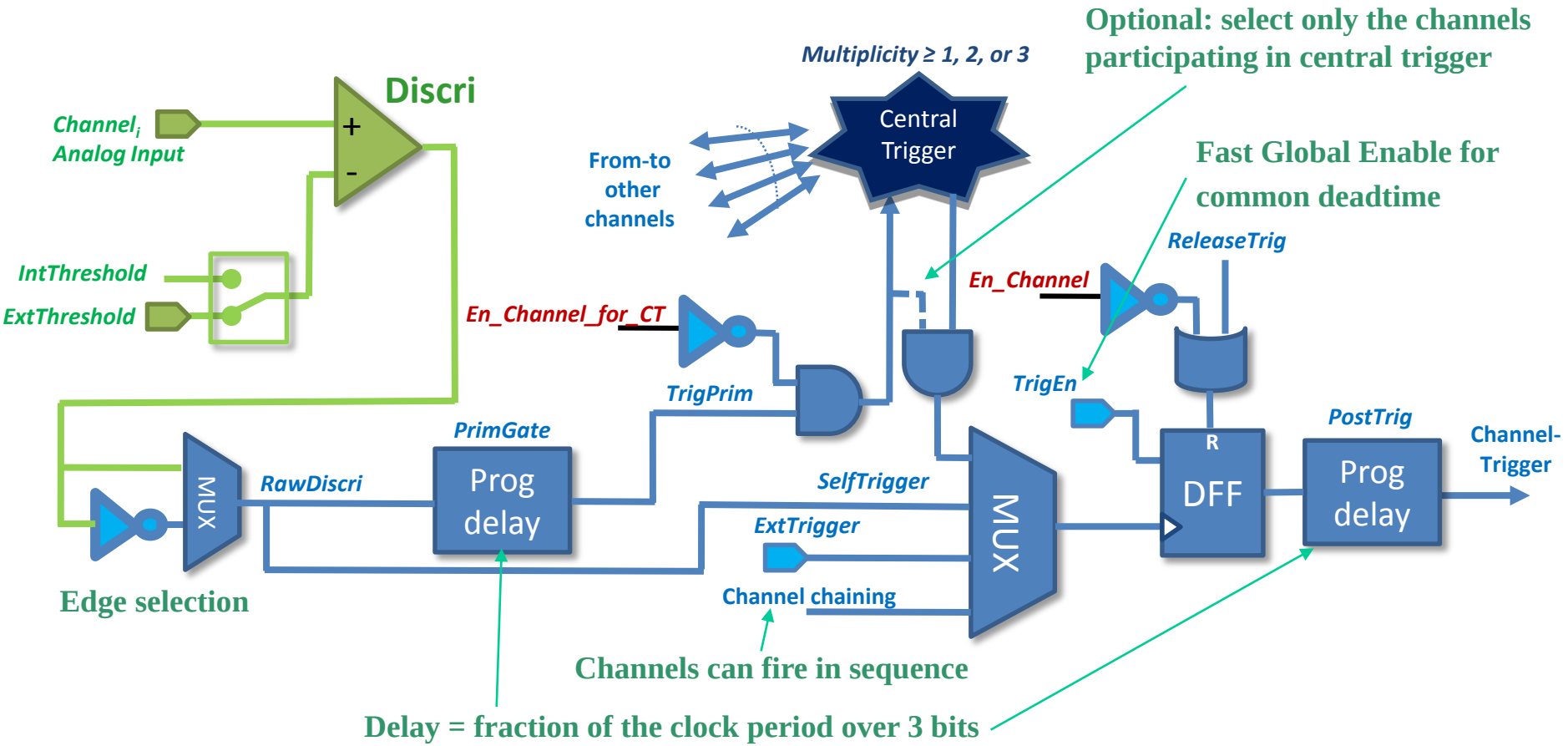


Main features of SAMPIC (not exhaustive)

- Last version of the chip submitted in **November 2016**
- **Wide range DLL**: 3 different sizes of starving transistors can be selected in the main DLL in order to optimize its INL and jitter
- Improved "central trigger" (OR, **multiplicity of 2 & 3**) with possibility of **common deadtime or selecting only channels participating in decision**
- **Channel chaining option**: user-defined sets of channels can be chained in time.
- **All DACs necessary for controlling the chip have been integrated**
  - ADC resolution **internally selectable between 7 and 11 bits**
- **Integrated TOT measurement**
- **"Ping-Pong" (toggling) mode:** channels work in pairs.
- **Translator input block** to deal with any digital signal (unipolar or differential)
- **Auto-calibration** (ADC and Time INL): dedicated signal sources are implemented in the chip in order to perform both calibrations in standalone.
- **New versions of the daughterboards** adapted to the new chips
- Constant improvements of **Firmware and DAQ software** thanks also to users' feedback
- **64-channel board and 256-channel (512?) mini-crate** under study.

Trigger options (simplified)

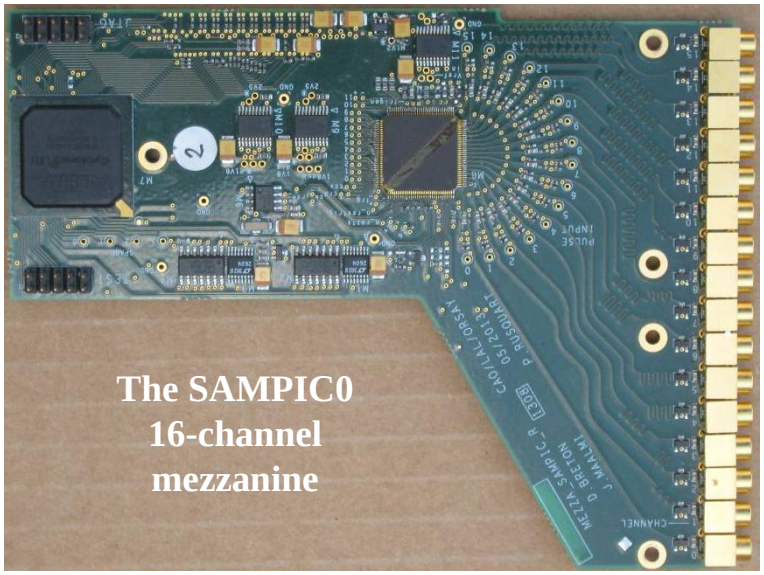
- **One very low power signal discriminator/channel**
- **One 10-bit DAC/channel to set the threshold (which can be external)**
- **Several trigger modes programmable for each channel:**



Only the triggered channels are in dead time

Modules & DAQ setup

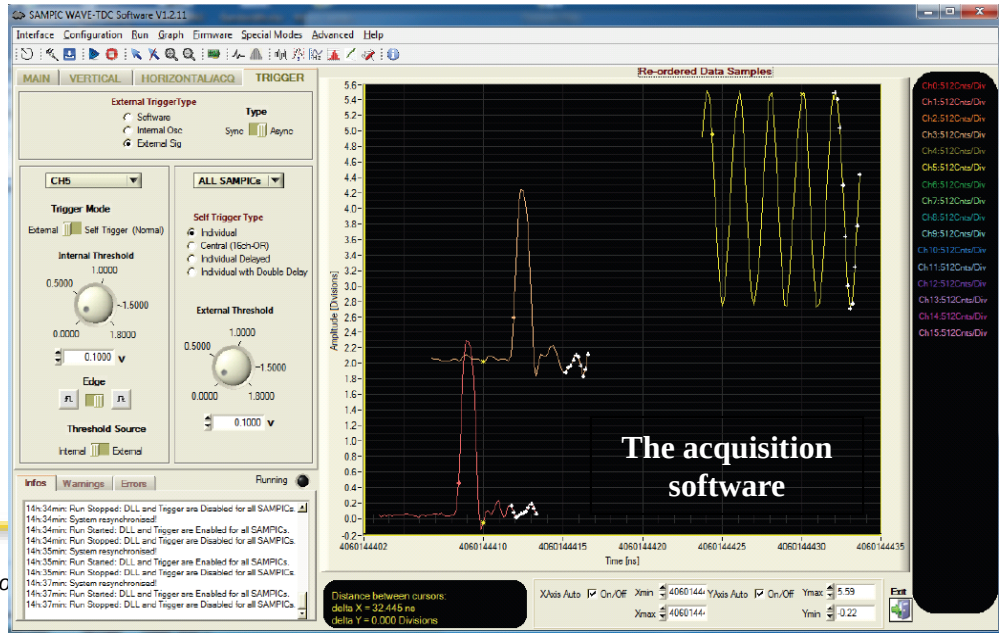
- **32-channel module integrating 2 mezzanines**
- **1 SAMPIC/mezzanine**
- **USB, Gbit Ethernet UDP (special secured version developed by Jihane with no data loss)**



- **Acquisition software** (& soon C libraries)

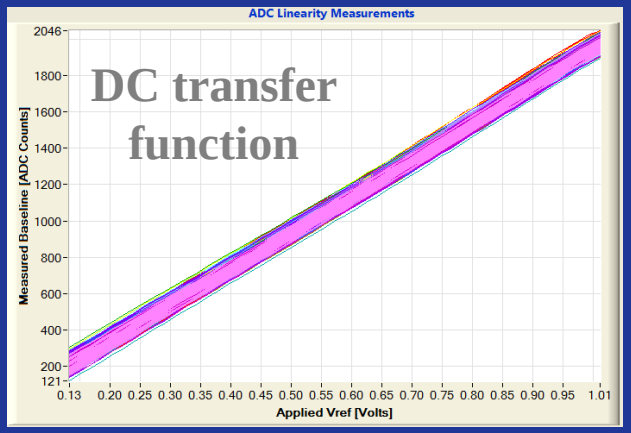
=> full characterization of the chip & module

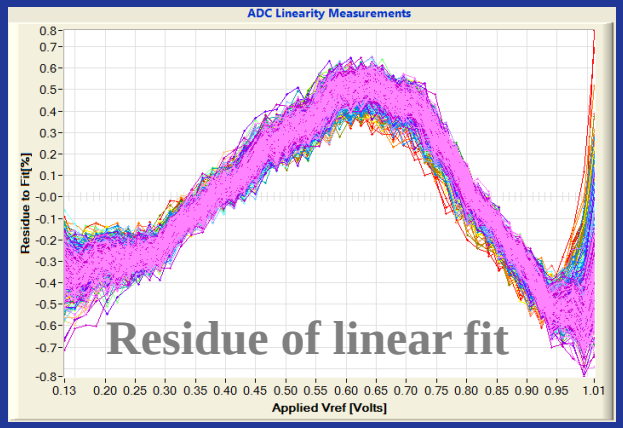
- Timing extraction (dCFD, interpolation…)
- **Special display** for **WTDC mode**
- Data saving on disk.
- Used by all SAMPIC users.



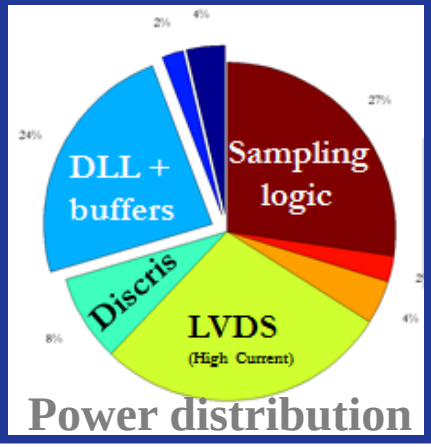
SAMPIC performances

- Wilkinson ADC works as expected with 1.3 GHz clock
- Dynamic range of 1V with a 0.5mV LSB when coding over 11 bits
- Gain dispersion between cells ~ 1% rms
- Non linearity <1.4 % peak to peak



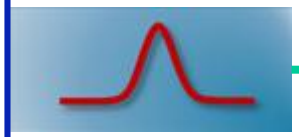


- After correction of each cell (linear fit) :
  → **noise = 0.95 mV rms** (∀ Fech)
  ≡ **~10 bits rms of dynamic range**
- **Discriminateur noise ~ 2 mV rms**
- **Power consumption: 10mW/channel**
- **3dB bandwidth: 1.6 GHz**
- **Counting rate > 2 Mevts/s (full chip, full waveform), up to 10 Mevts/s with ROI**



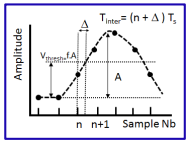
Time Difference Resolution (TDR)

800mV
300ps risetime
1ns FWHM

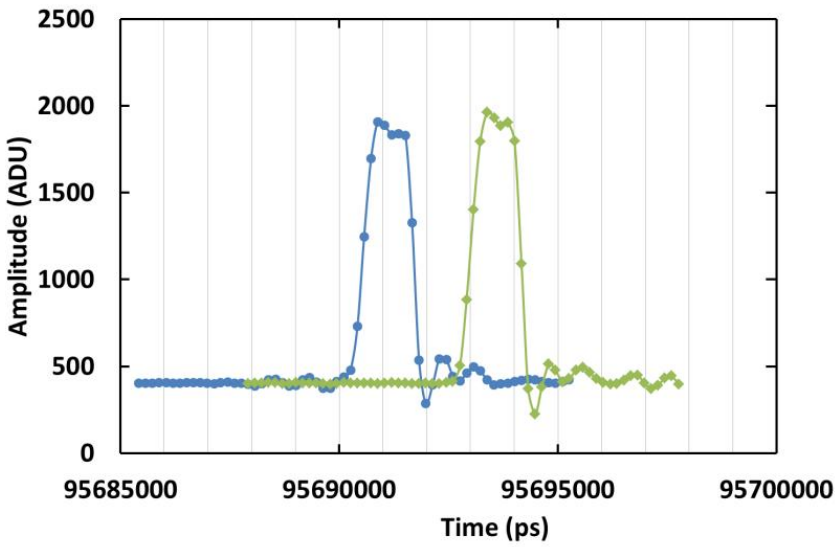


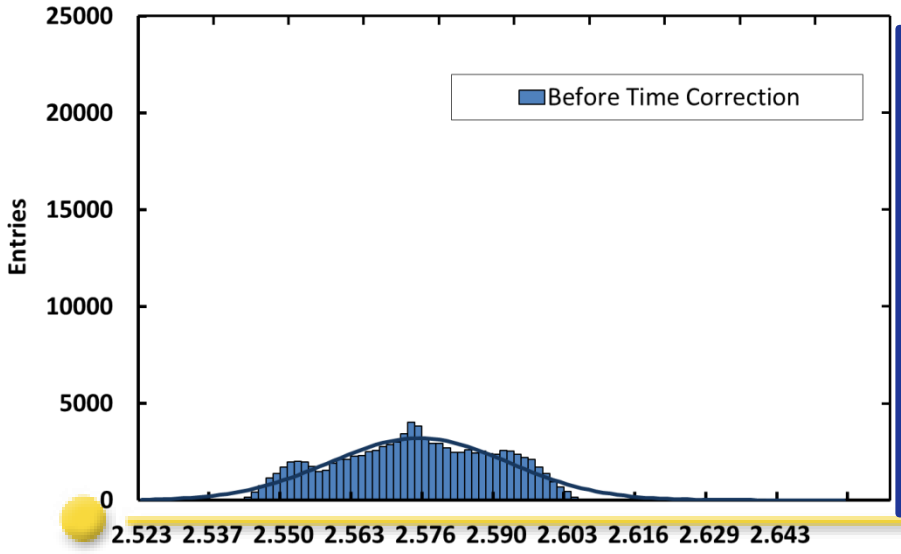
Delay by cable
(2.5ns)

6.4GS/s, 11bit
Self trigger
Single chip



dCFD algorithm
only (2 samples)





- **No out-of-time event**
- **TDR = 18 ps RMS before any time correction**
- **Non gaussian distribution due to DLL non uniformity (TINL)**
- **Can be easily calibrated and corrected (with the sinewave crossing segments method shown in the backup slides)**

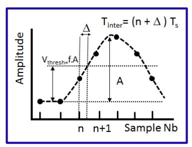
Timing Difference Resolution (TDR)

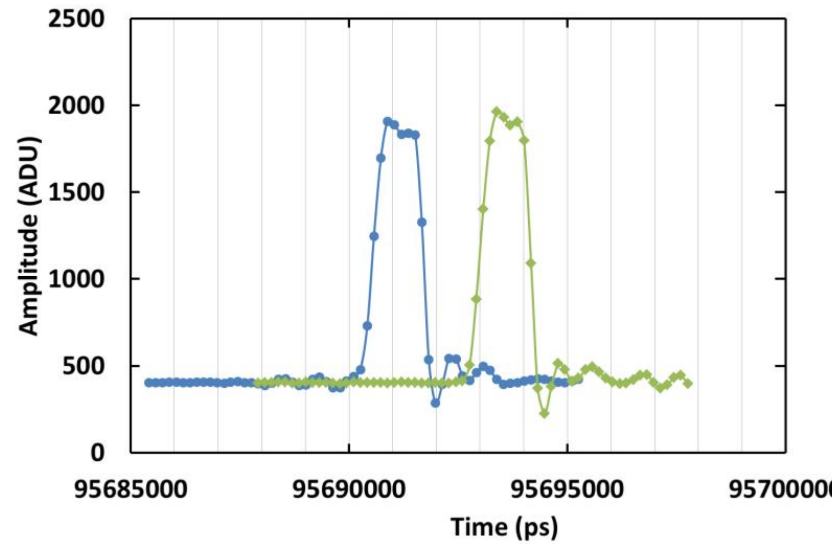
800mV
300ps risetime
1ns FWHM

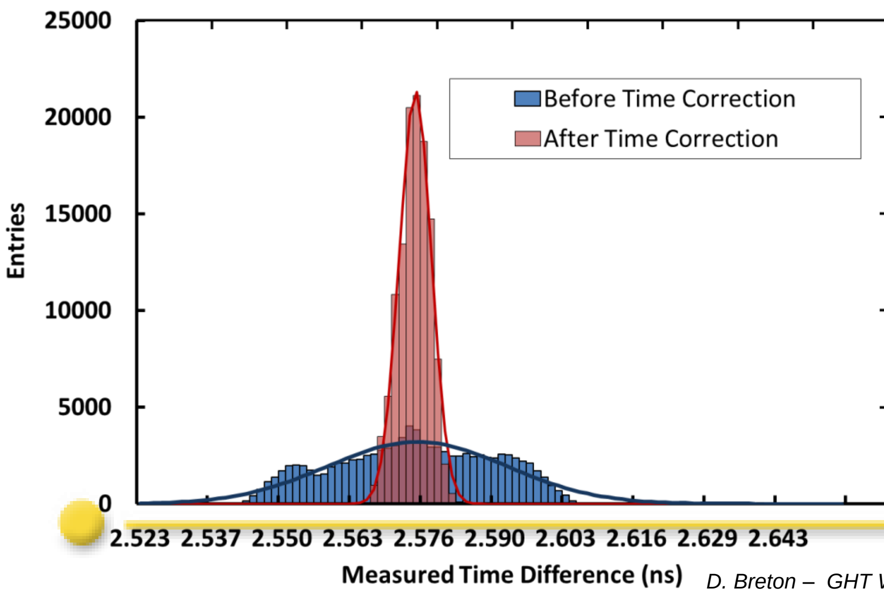
Delay by cable
(2.5ns)

6.4GS/s, 11bit
Self trigger
Single chip

dCFD algorithm
Only (~2 samples)







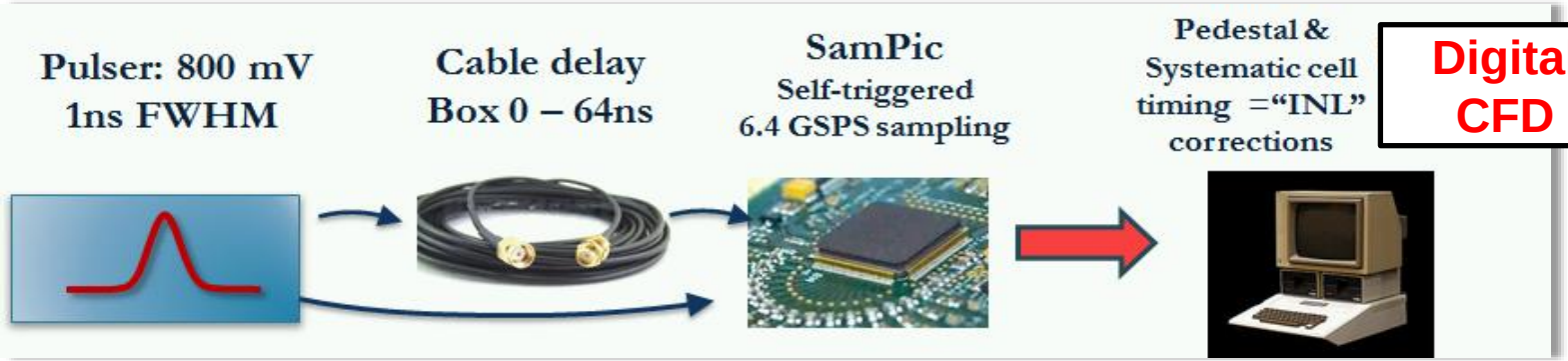
- **No out-of-time event**
- **TDR = 18 ps rms before any time correction**

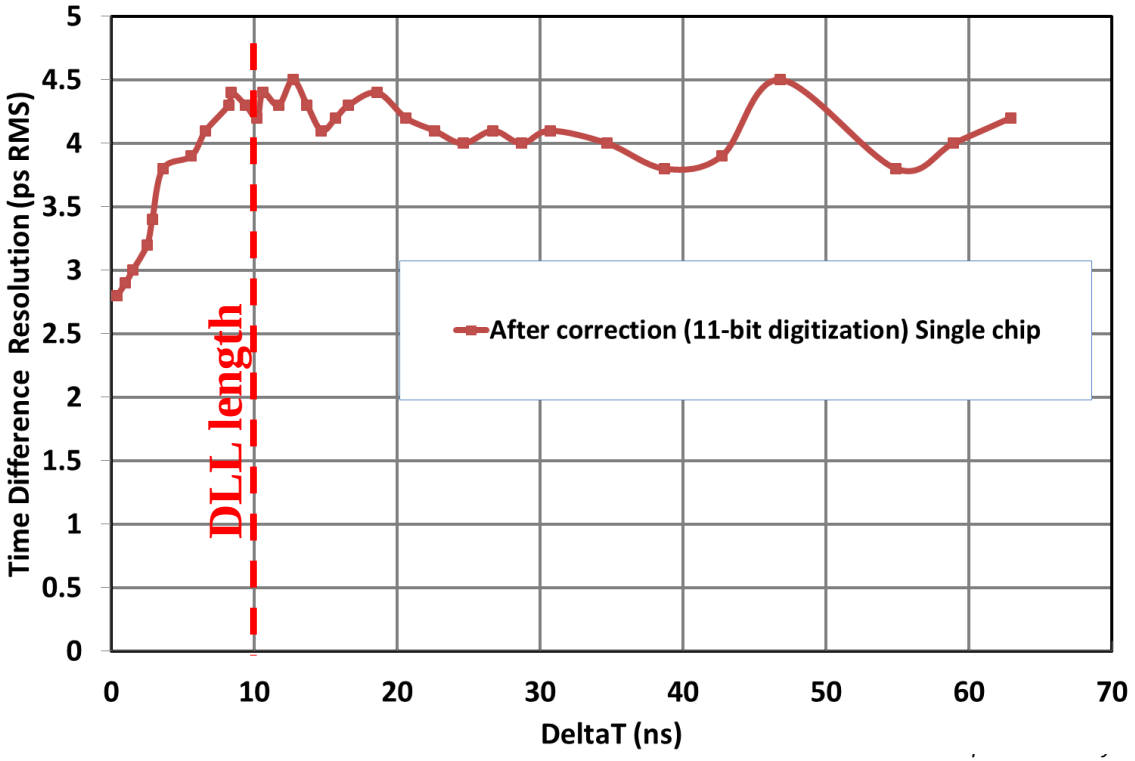
- **Non gaussian distribution due to DLL non uniformity (TINL)**
- **Can be easily calibrated and corrected (sinewave crossing segments method [1])**

- **TDR = 3.5 ps rms after correction**

[1] D. Breton et al, TWEPP 2009, p149

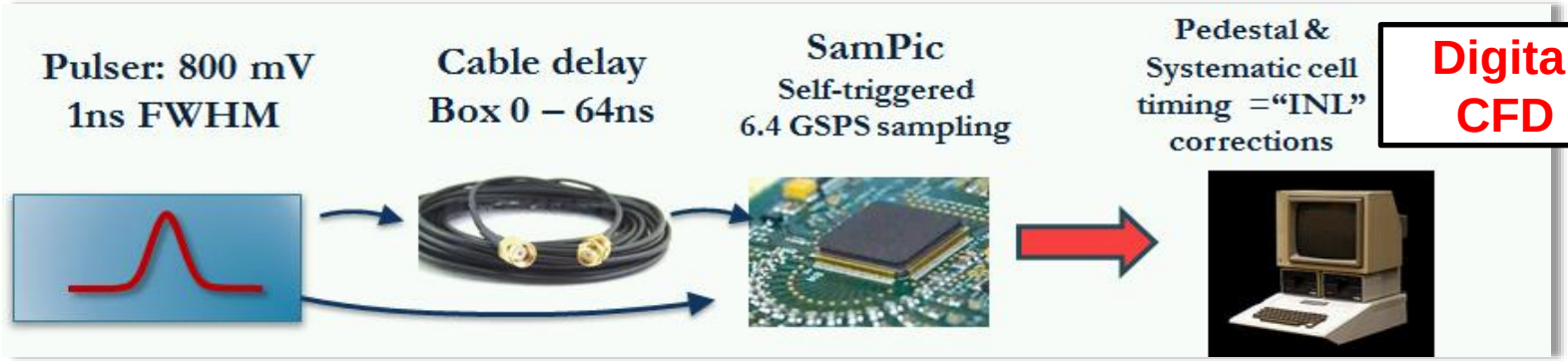
ΔT resolution vs delay

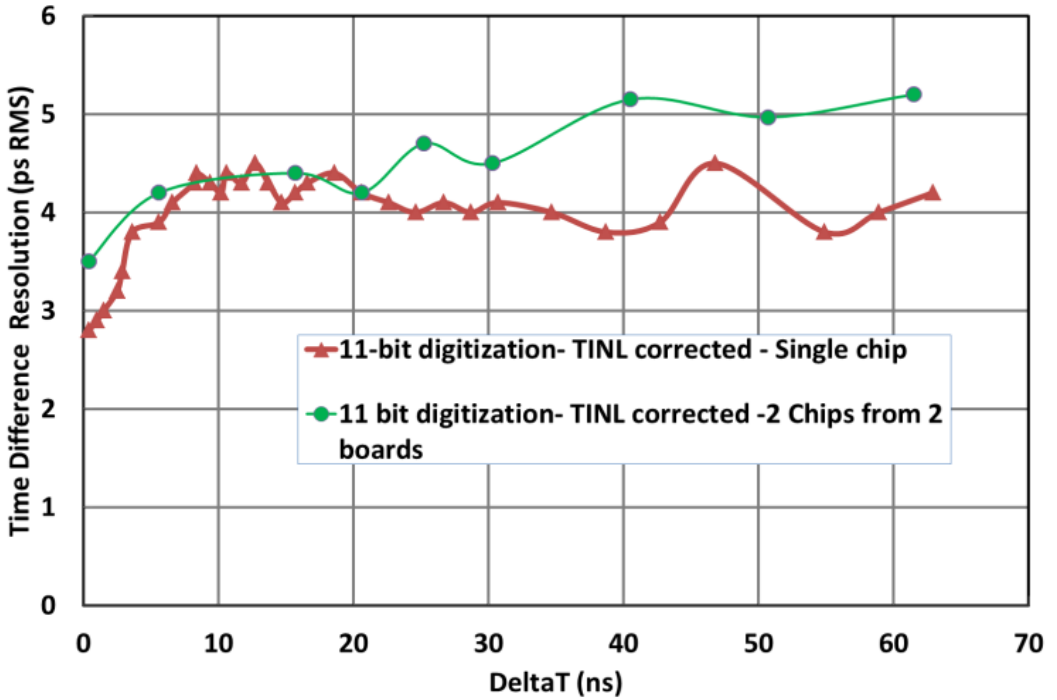




- **TDR < 5 ps rms after time correction.**
- **TDR is constant for Δt > 10ns**

ΔT resolution vs delay





- TDR < 5 ps rms after time correction.
- TDR is constant for Δt > 10ns

- ~ unchanged when using 2 chips from 2 mezzanines (slope here comes from slower risetime of 800ps)

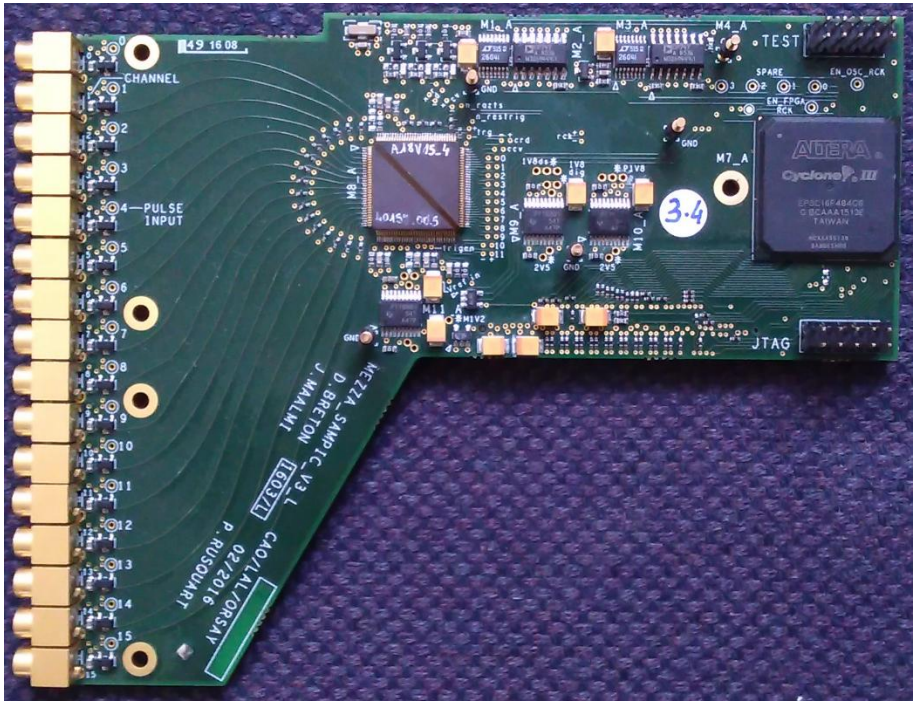
=> measurement are uncorrelated

=> channel single pulse timing resolution is < 3.5 ps rms (5 ps/√2)

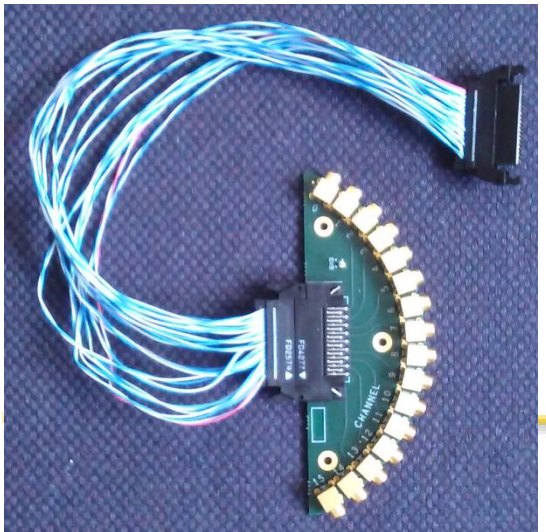
From these 2 types of measurements, we could extract the jitter from the motherboard clock source: ~ 2.2 ps rms

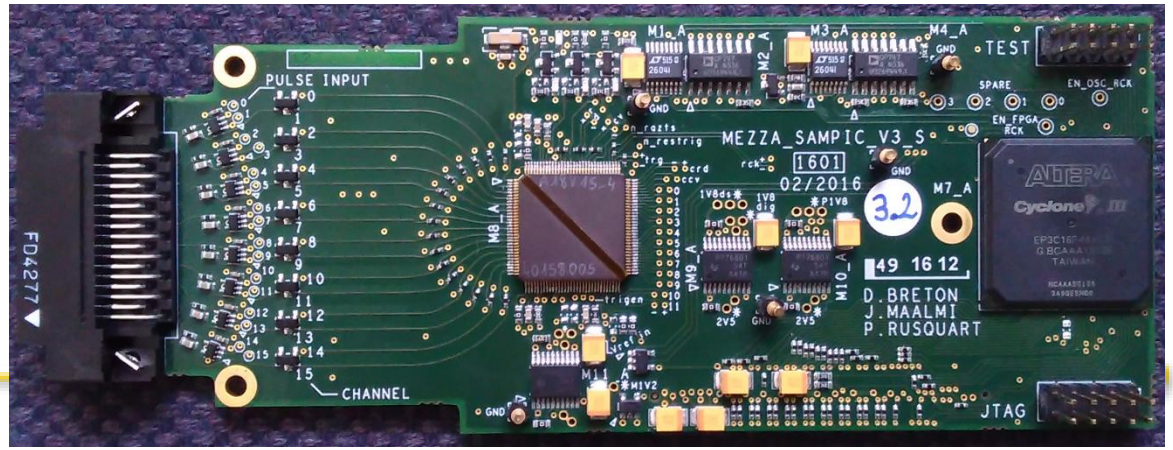
=> SAMPIC's own jitter < 2.5 ps rms

Recent daughterboards development



- New mezzanine cards have been developed for housing the new versions of the chip (including the digital differential option)
  1. Analog/digital input with MCX
  2. Analog/digital input with flat cable
  3. Differential digital input with flat differential cable
- Adaptors have also been developed





SAMPIC: performance summary

		Unit
Technology	AMS CMOS 0.18µm	
Number of channels	16	
Power consumption (max)	180 (1.8V supply)	mW
Discriminator noise	2	mV rms
SCA depth	64	Cells
Sampling speed	1 to 8.4 (10.2 for 8 channels only)	GSPS
Bandwidth	1.6	GHz
Range (unipolar)	~ 1	V
ADC resolution	7 to 11 (trade-off time/resolution)	bits
SCA noise	< 1	mV rms
Dynamic range	> 10	bits rms
Conversion time	0.1 (7 bits) to 1.6 (11 bits)	µs
Readout time / ch @ 2 Gbit/s (full waveform)	450	ns
Single Pulse Time precision before correction	< 15	ps rms
Single Pulse Time precision after time INL correction	< 3.5	ps rms

Taking data with detectors

- SAMPIC modules are already used with different detectors on **test benches or test beams.** Unfortunately, very little public data available until now …
- Tested with **PMTs, MCPPMTs, APDs, SiPMs, fast Silicon Detectors, Diamonds**: performances are equivalent to those with high-end oscilloscopes
- Different R&Ds ongoing with the **TOF-PET** community (CERN, …)
- SAMPIC has been used for test beams of **TOTEM and SHIP at CERN**
- It is also used for **fast mesh-APD** characterization and test beams
- **TOTEM** is currently developping a CMS-compatible motherboard housing SAMPIC mezzanines
- **SHIP** is testing SAMPIC for its fast timing detector. SAMPIC option is described in the technical proposal for the fast timing detector and calorimeter (two-gain version)
- SAMPIC is in use at Giessen for **PANDA EndCap DIRC** caracterization.
- It will soon be used for **ATLAS HGTD beam test at CERN**

Conclusion

- ✓With respect to ADCs**, waveform sampling with fast analog memories** permits **high precision measurements** at lower expense
  - ➢ Possible bothering drawbacks are sampling depth & readout dead-time
- ✓Since **1992**, we have been continuously developing such devices
- ✓We were pushed by technology and requests of physics community
- ✓Chips are becoming full systems like SAMPIC
  - ➢ **CMOS 0.8 µm** permitted a high speed (2GS/s), a wide dynamic range and a very low noise (**MATACQ**: up to 14 bits) but dead-time of 650 µs => well adapted for **"low rate" precision experiments**
  - ➢ **CMOS 0.35 µm** offers a reduced dynamic range (~ 2V => 12 bits) but permitted increasing the sampling rate to 3.2 GS/s and reducing dead time (125 µs) with a few ps rms resolution => **multipurpose systems: WaveCatchers**
  - ➢ **CMOS 0.18 µm** permits reaching very high rates (> 10 GS/s) but dynamic range goes down to 1V => 10 bits with a very fast embedded ADC with a latency of only 1.5 µs, a few ps rms resolution and a very low power consumption => **SAMPIC**, optimized for **high rate & large scale time measurement** (like PET)

What's next …

- ✓ We will try to increase the SNR of the WaveCatchers to propose a version more adapted to the "replacement" of the MATACQ boards
- ✓ We think about submitting a new version of SAMLONG with a higher SNR and a few other improvements (not yet fully decided)
- ✓ We will develop a slower version of SAMPIC with sampling frequencies between ~ 200 MHz and 1 GHz, adapted to signals with a few ns risetime or more.
- ✓ …

Thank you ☺

Backup slides

NIM paper recently published

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Measurements of timing resolution of ultra-fast silicon detectors with the SAMPIC waveform digitizer

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ABSTRACT

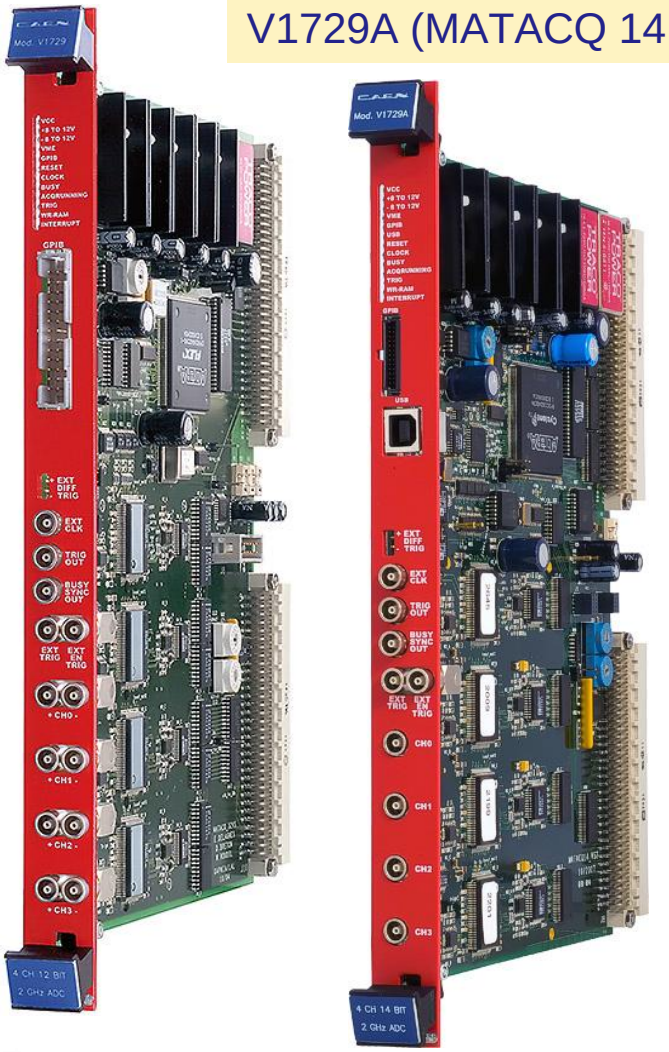
The SAMpler for PICosecond time (SAMPIC) chip has been designed by a collaboration including CEA/IRFU/SEDI, Saclay and CNRS/LAL/SERDI, Orsay. It benefits from both the quick response of a time to digital converter and the versatility of a waveform digitizer to perform accurate timing measurements. Thanks to the sampled signals, smart algorithms making best use of the pulse shape can be used to improve time resolution. A software framework has been developed to analyse the SAMPIC output data and extract timing information by using either a constant fraction discriminator or a fast cross-correlation algorithm. SAMPIC timing capabilities together with the software framework have been tested using pulses generated by a signal generator or by a silicon detector illuminated by a pulsed infrared laser. Under these ideal experimental conditions, the SAMPIC chip has proven to be capable of timing resolutions down to 4 ps with synthesized signals and 40 ps with silicon detector signals.

http://arxiv.org/abs/1604.02385

CAEN products based on MATACQ & SAMLONG

V1729 (MATACQ 12 bits)

V1729A (MATACQ 14 bits)



X743 family (based on SAMLONG)

Optimization of Software Online data treatment

For systems with a high number of channels, the type of software data treatment is constrained by three factors that are linked to the system :

1. **Trigger Rate :** the data rate is directly linked to it
2. **Capacity to save data on disk** : the more data per event, the bigger the time to store it and the bigger space needed on disk
3. **Capacity to perform online treatment :**
   - Takes time **but** reduces the data flow
   - If complex → takes more time

An ideal optimized system would follow the trigger rate and store on disk only data fulfilling the experiment requirements.

This is why for High Trigger Rate systems, online data treatment has to be as limited as possible, nevertheless offering a very good precision (for instance, high-degree polynomial fit of signal does not seem to be a reasonable option for on-line calculation, but ok for off-line studies)

For very fast acquisition system, **firmware extracted data is the ideal solution (→ no software online treatment)**: with the WaveCacher systems it gives an almost similar time precision (up to 64 channels as of today)

→ event rate with 16-ch board > **10 000 evts/s**.