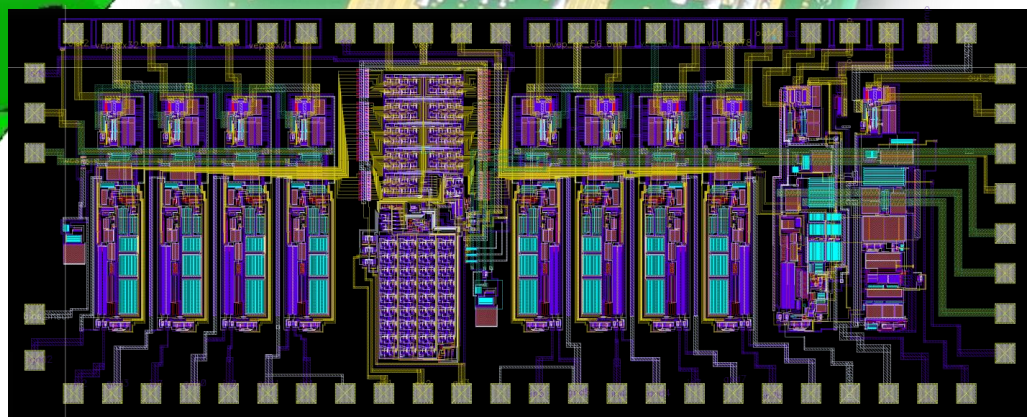
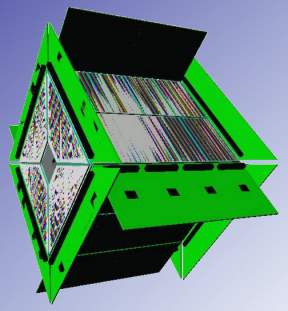
# The low-noise low-power multi-channel ASIC preamplifier of TRACE: design, results and perspectives



GHT workshop 2017 @ Orsay
23-24 January

S. Capra, A. Pullia



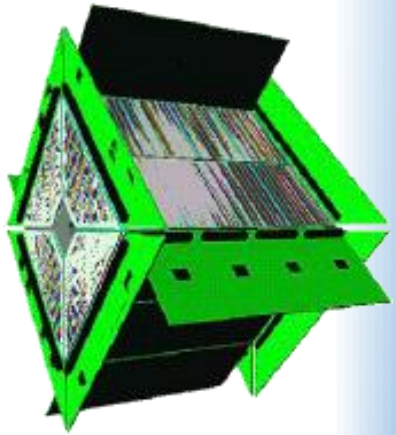
# The low-noise low-power multi-channel ASIC preamplifier of TRACE: design, results and perspectives

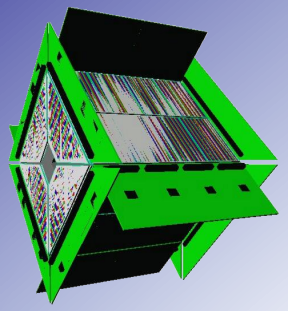
## Context

- New generation of nuclear-physics experiments with radioactive ion beams.
- A technical advance for the FEE applied to the new highly segmented telescopic silicon detectors is required.

## Goal of the research

- High-resolution spectroscopy of charged particles implementing a FEE based on a dedicated multichannel CSP ASIC.



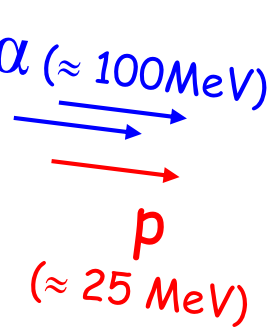


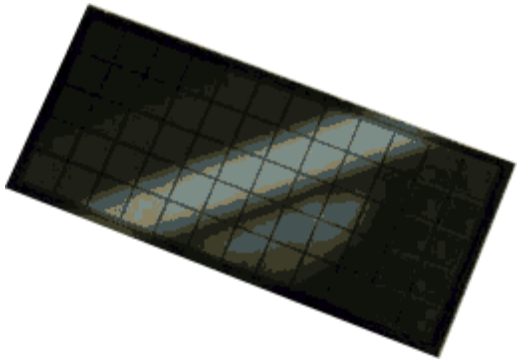
# TRACE detector array specifications

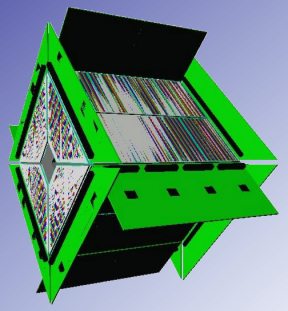
- Fit inside a sphere of 24 cm of diameter
- All the FEE electronics must fit inside the same volume
- Rise time of ~ 25 ns for 200 μm thick ΔE layer
- Transparent to γ radiation: coupled with γ spectrometer
- More than 1000 output channels

- 4π configuration
- 4x4 mm and 8x8 mm segmentation
- Detection of light charged particles, neutron, heavy ions
- Particle discrimination and gamma doppler correction
- Decay spectroscopy

extremely hostile background of highly energetic charge particles in next-generation nuclear physics experiments with high-intensity beams



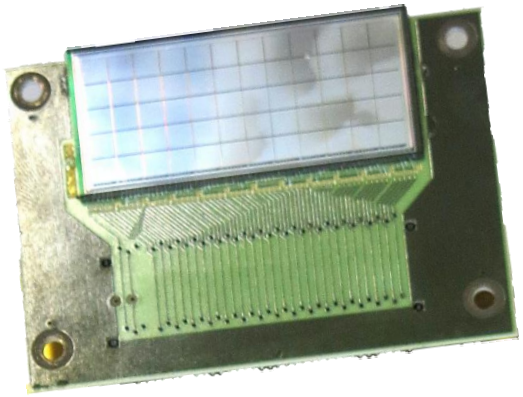



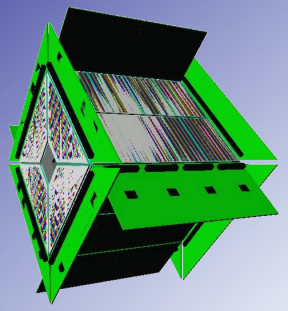


# Silicon pad detector specifications

- Detector thickness: E pad **1-1.5mm**, ΔE pad **200µm**
- Operated at **room temperature** (no need for cryogenic temperatures)
- Single pad capacitance value: ~ from **4 pF** to **15 pF**
- Energy dynamics for detected particles: ~ **100 MeV** for a – particles, **25 MeV** for protons
- Intrinsic energy resolution**: ~ 20 keV** @ **5.5 MeV** for a – particles in 200 **µm** detector
- Segmentation: **~ 4x4 mm** geometry (or strips?)

In the final design, the pitch of a preamplifier channel should not exceed the one of a front pad





# Specifications for the front-end electronics

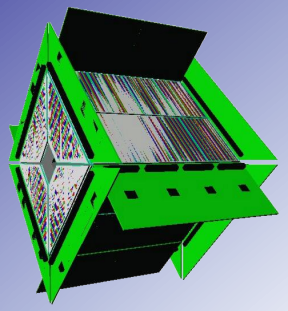
- low noise (no more broadening than the intrinsic one)
- **10 mW** of single - channel power consumption
- wide bandwidth: rise time of ~ **10 ns** (pulse shape analysis)
- low power consumption (large number of channels operated in vacuum)
- High stability of the gain and of the shape of the preamplifier response (loop gain~$10^3$)
- **LARGE DYNAMIC RANGE**:

  - at least ~**$10^5$** : from a **few keV** to **100-200 MeV** (or above)

  - minimization of the dead time in a larger energy range up to some **hundreds of MeV**

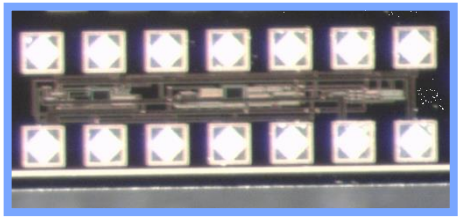
Given such specifications, the choice of an integrated solution became mandatory

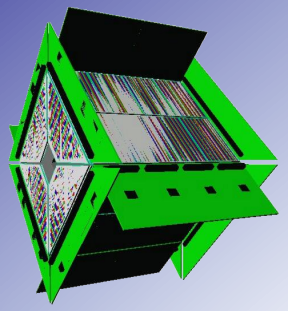
The requested dynamic range cannot be covered with an integrated CSP following a traditional design



# 2012: First prototype with hybrid (discrete-integrated) structure

- The hybrid solution was due to the very good noise performance of the discrete input transistor **BF862**
- Fairly high power consumption (>= 15mW)
- Some other external components required
- Risetime of 15ns (10%-90%)
- Non-zero DC bias point
- External bias resistances
- Very good resolution (1keV with 6us of shaping time)





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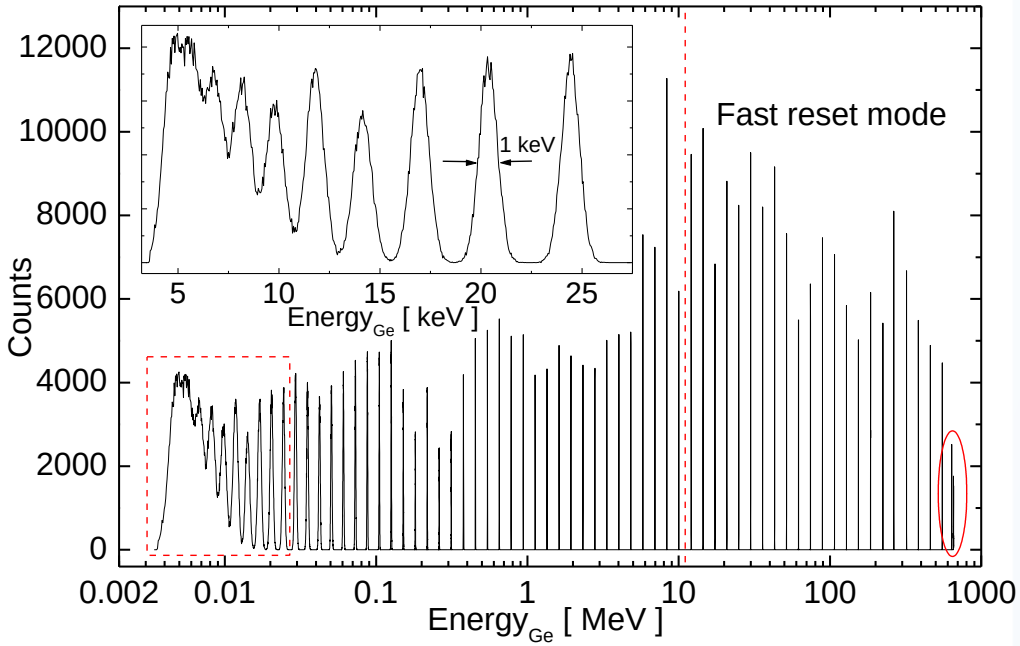
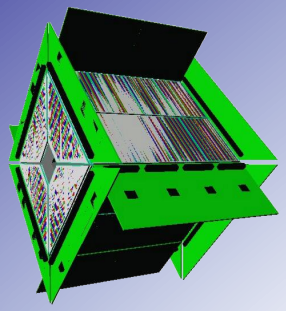
- Some other external components required
- Risetime of 15ns (10%-90%)
- Non-zero DC bias point
- Very good resolution (1keV in germanium, 1.22keV in silicon) with 6us of shaping time

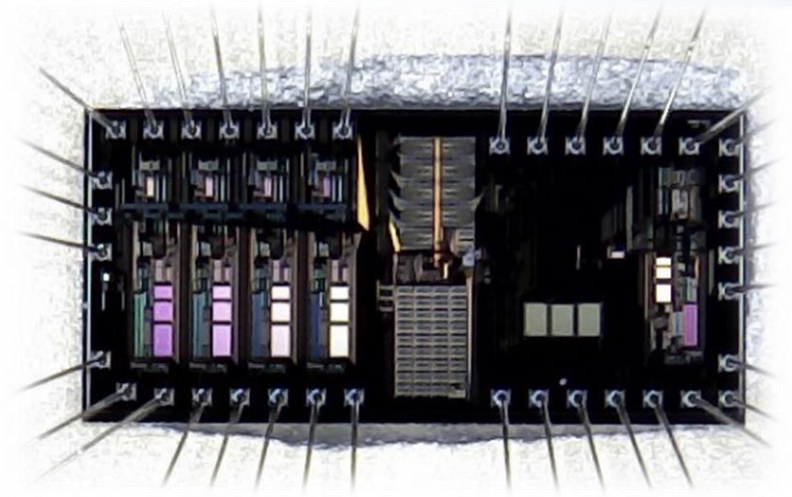




# 2014: second prototype with all-integrated multichannel structure

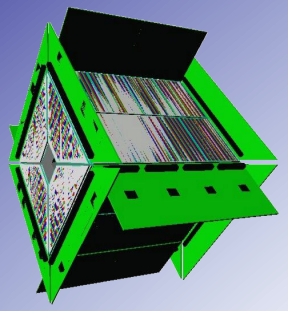
## *ASIC details*

- Technology: AMS C35B4C3
- Dimensions: 1.5 mm X 3.3 mm
- Power supply: from ± 2.5 V to ± 2.6 V



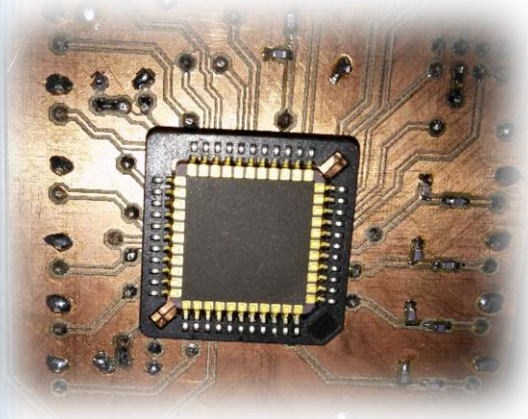
## *ASIC features*

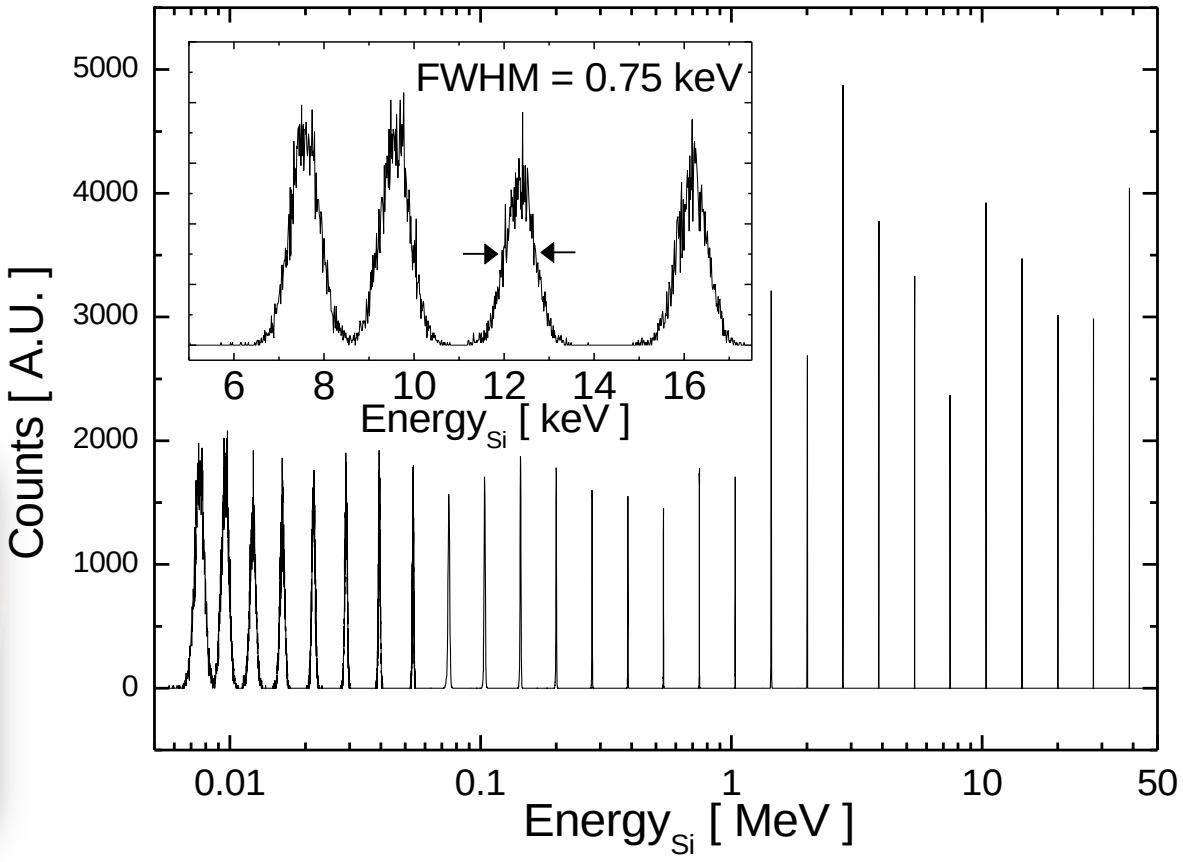
- Four channels specifically designed for hole signals: front channels
- One channel specifically designed for electron signals: back channel
- Integrated differential input
- 0V DC bias point
- 11mW static power consumption
- Two independent bias networks with bootstrap device
- The back channel separately powered from the rest of the chip
- $I^2C$ engine
- $I^2C$ address selectable with 3 address pin

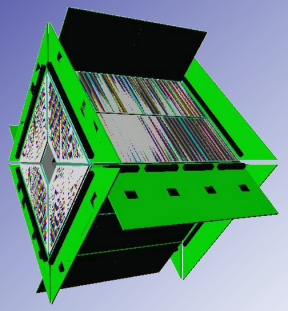


# Pulser spectrum acquired from the **front channels** of the 2014 CSP ASIC for TRACE: **BEST CASE EVER**

After having mounted the ASIC on a custom-designed PCB we evaluated its spectroscopic performance with a pulser and a traditional analog spectroscopic chain.

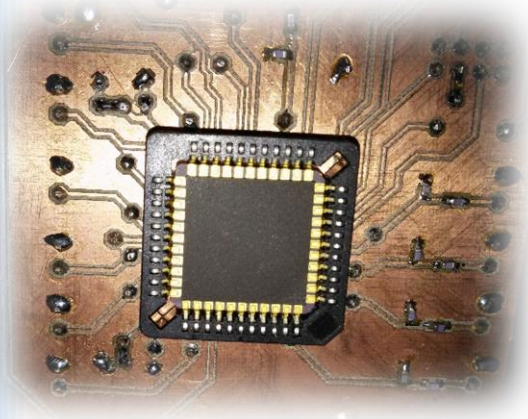


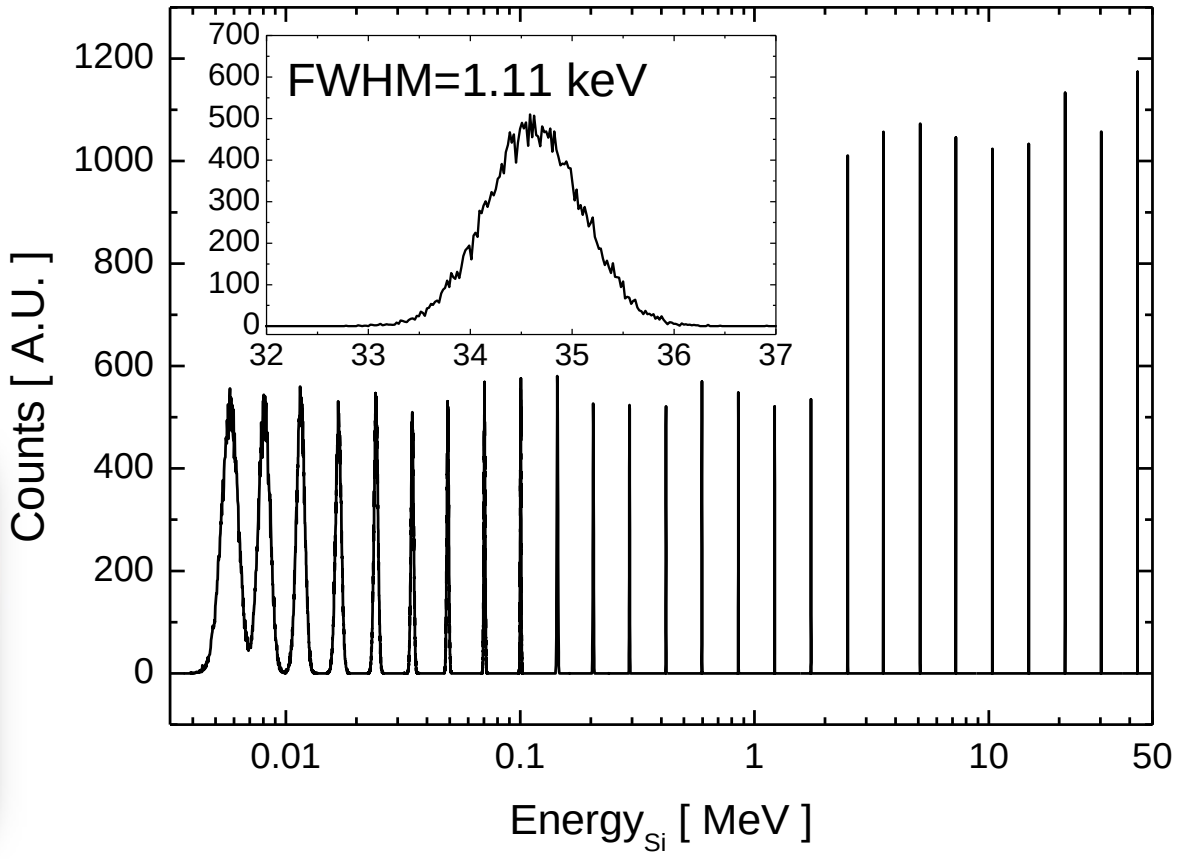


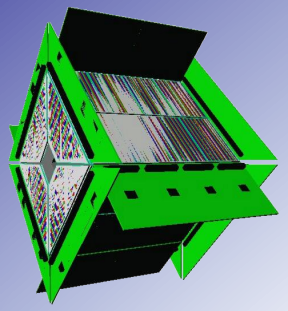


# Pulser spectrum acquired from the **front channels** of the 2014 CSP ASIC for TRACE: **TYPICAL CASE**

After having mounted the ASIC on a custom-designed PCB we evaluated its spectroscopic performance with a pulser and a traditional analog spectroscopic chain.

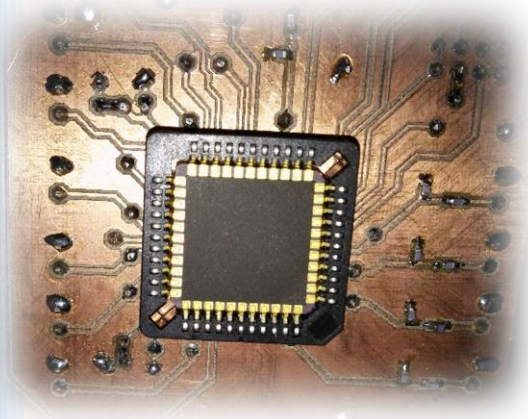


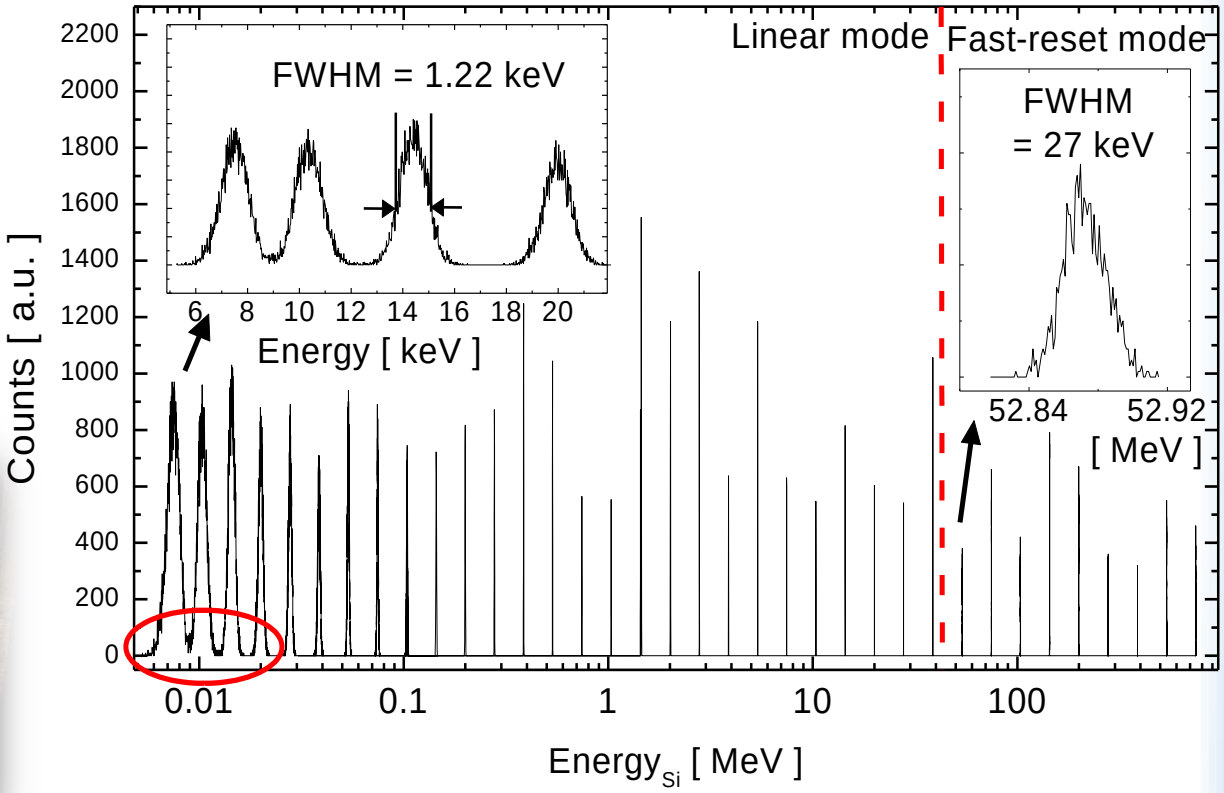


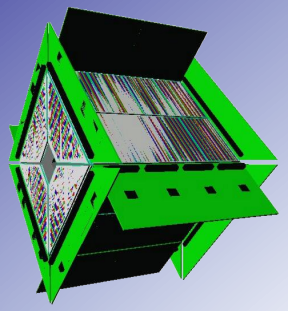


# Pulser spectrum acquired from the **back channel** of the 2014 CSP ASIC for TRACE: **TYPICAL CASE**

The over-threshold spectrum was obtained capturing the comparator signals with a scope and applying a TOT algorithm with MATLAB

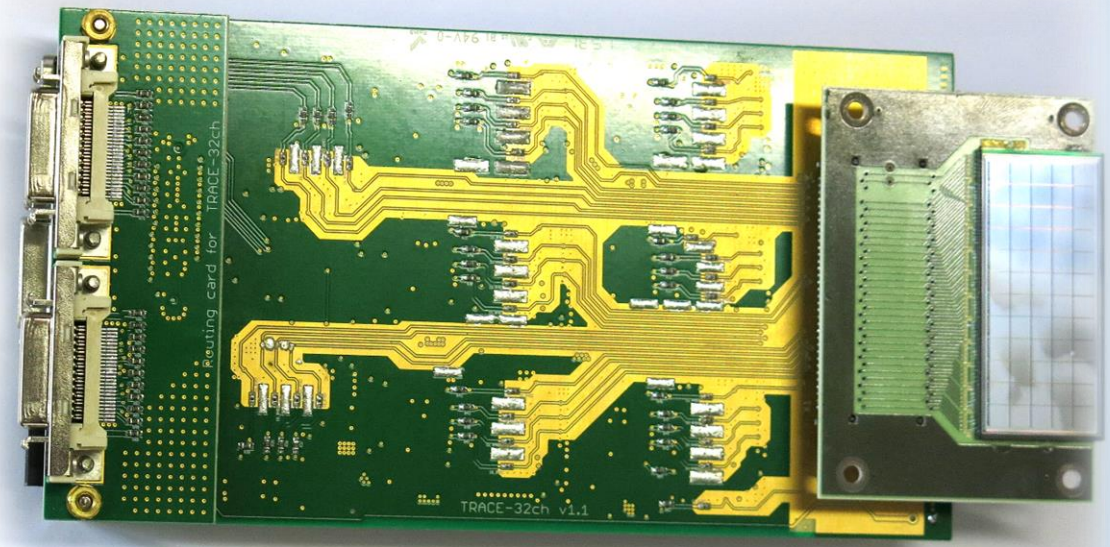


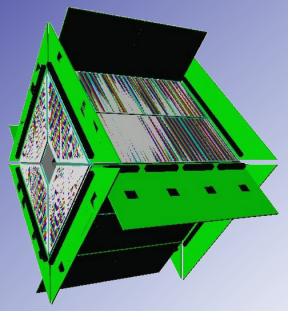




# 2015: Design and realization of the TRACE32ch v1.1 board

- Low-noise and low-electric dispersion laminate: Rogers RO4003C
- 6-layer design
- Minimization of the cross-talk between channels thanks to proper ground shielding
- Individual power supply filtering for each IC
- 8 ASIC for a total of 32 front channels and 1 back channel



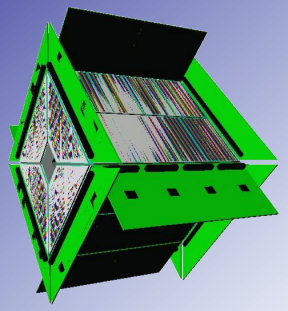


# Acquisition of the spectrum of an $^{241}Am^{244}Cm^{239}Pu$ alpha source @ LNL

- Acquisition of a triple alpha source $^{241}Am^{244}Cm^{239}Pu$

| Isotope | Peak Energy [ MeV] | Relative peak intensity [%] |
|---|---|---|
| Pu-239 | 5.105 | 11.5 |
| | 5.143 | 15.1 |
| | 5.155 | 73.4 |
| Am-241 | 5.388 | 1.4 |
| | 5.443 | 12.8 |
| | 5.486 | 85.2 |
| Cm-244 | 5.763 | 23.3 |
| | 5.805 | 76.7 |

- Digitizer: N1728A Caen modules (14-bit 100MHz)
- Trapezoidal filter: 500 samples shaping time
- Detector power supply: N1471 Caen module



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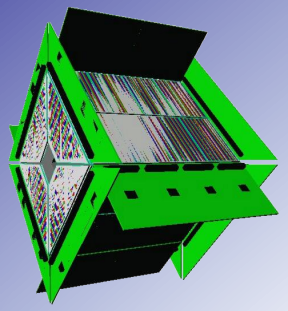
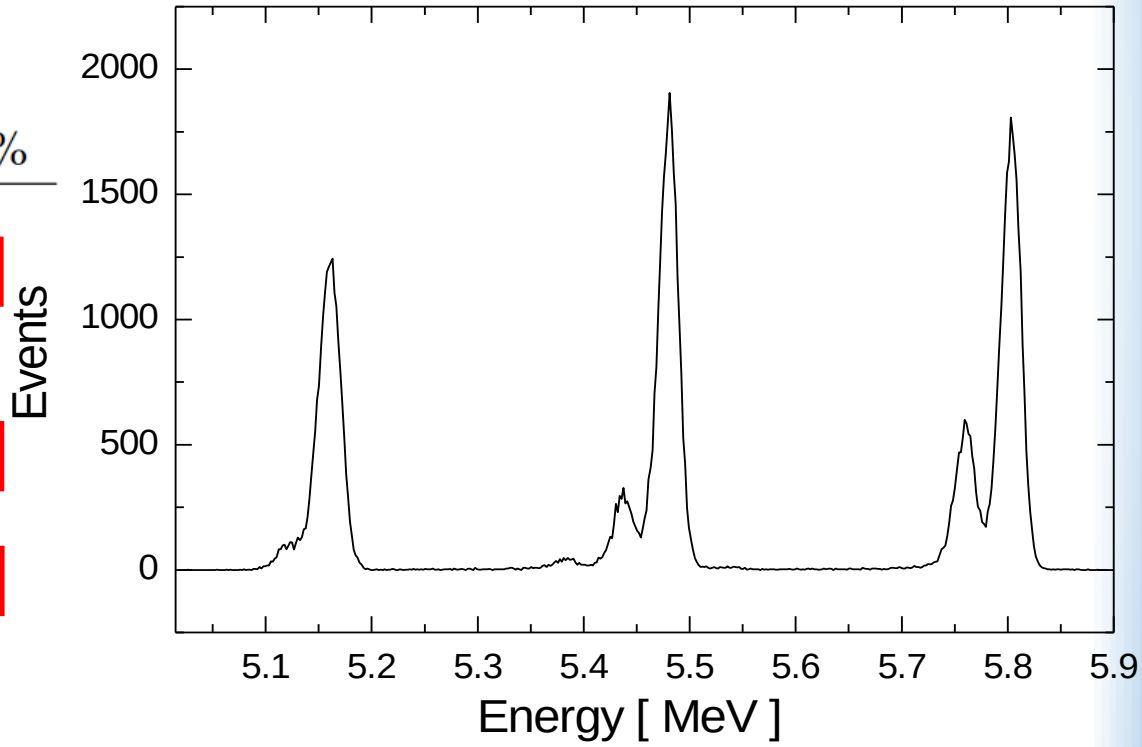
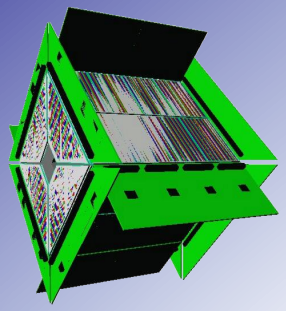


# Acquisition of the spectrum of an $^{241}Am^{244}Cm^{239}Pu$ alpha source @ LNL

- Front channel resolution

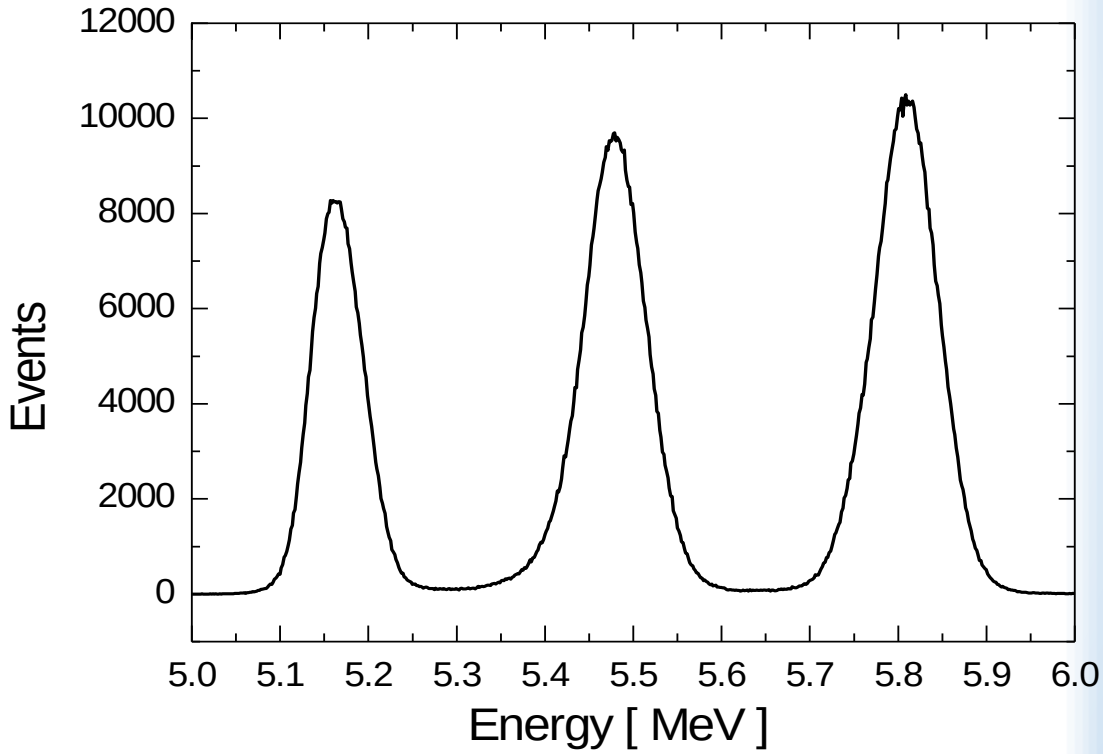
| E [ keV] | FWHM | FWHM % |
|---|---|---|
| 5143 | 39.45 | 0.77 |
| 5155 | 23.81 | 0.46 |
| 5388 | 135.36 | 2.51 |
| 5443 | 26.28 | 0.48 |
| 5486 | 21.56 | 0.39 |
| 5763 | 24.80 | 0.43 |
| 5805 | 22.02 | 0.38 |

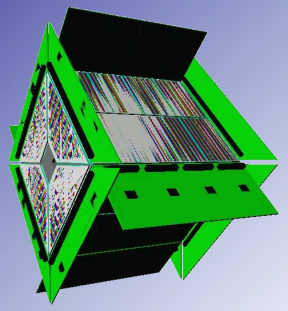




# Acquisition of the spectrum of an $^{241}Am^{244}Cm^{239}Pu$ alpha source @ LNL

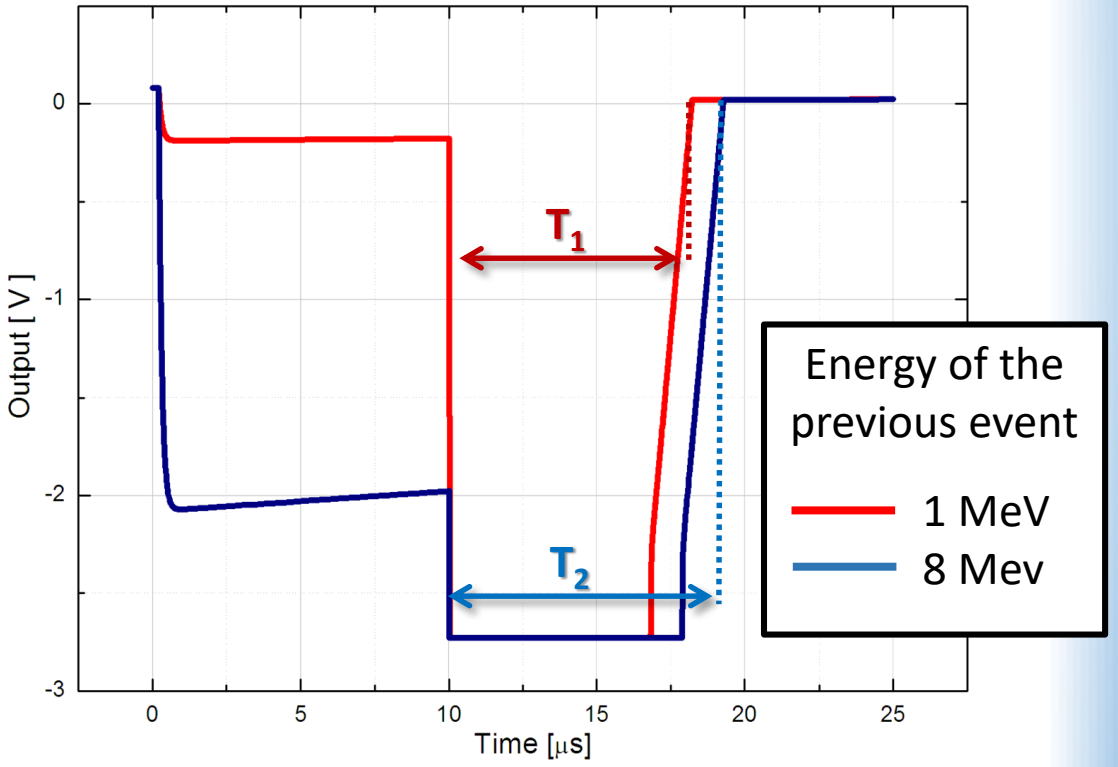
- Back channel resolution estimated around **70keV**





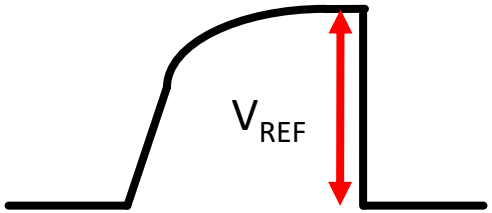
# Non idealities of the Time-Over-Threshold technique

- The digital TOT signal depends on the residual charge on $C_F$ before the reset process
- Need for an algorithm to correct this dependency
- Off-line digital correction: easy to implement but expensive in computational terms
- Our solution: an analog algorithm that performs the correction on-line

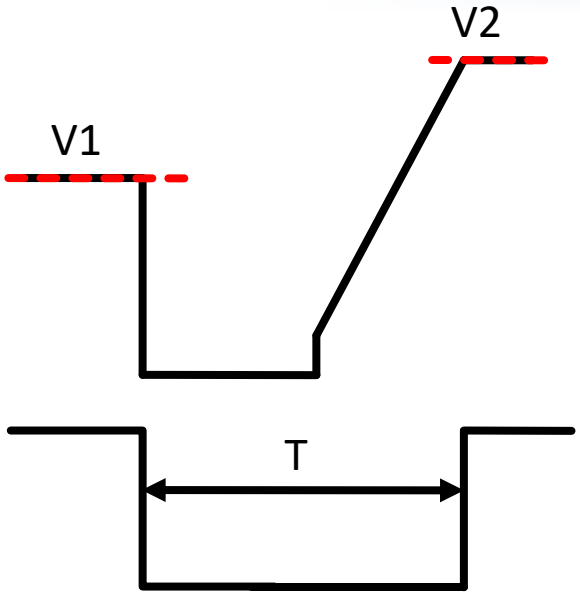


# Time-to-Amplitude Converter with correction algorithm

- Need to generate an auxiliary signal which amplitude VREF is directly proportional to the energy of the last physical event (and no longer depends on the residual charge of past events! )




Auxiliary signal Vout2




Vout 1

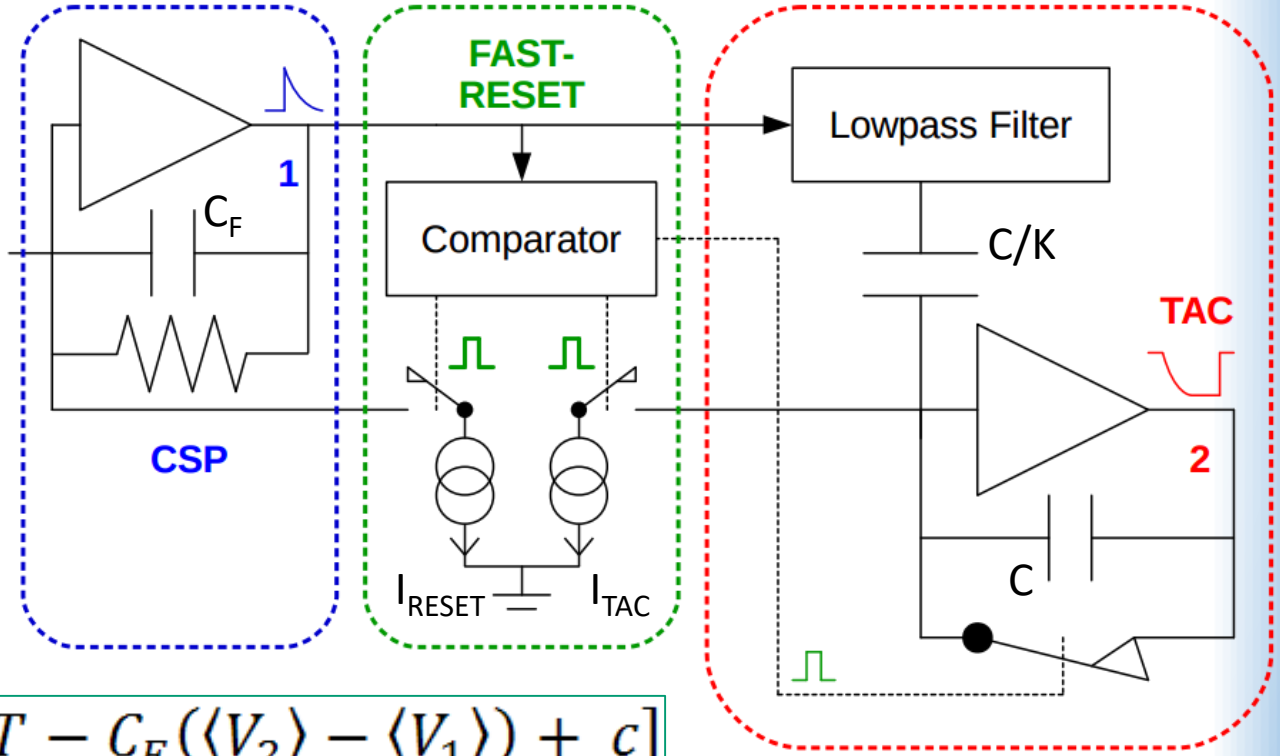
Comp out

$$E_{DET} \propto V_{REF} = \alpha[kT - C_F(\langle V_2 \rangle - \langle V_1 \rangle) + c]$$

# Time-to-Amplitude Converter with correction algorithm: **CIRCUIT IMPLEMENTATION**

$$V_{TAC} = \underbrace{\frac{I_{TAC} \cdot \Delta T}{C}}_{\text{Contribute of the } I_{TAC} \text{ current}} - \underbrace{\frac{1}{K}(V_2 - V_1)}_{\text{From low-pass filter}}$$

$$\frac{I_{TAC}}{C/K} = \frac{I_{RESET}}{C_F}$$

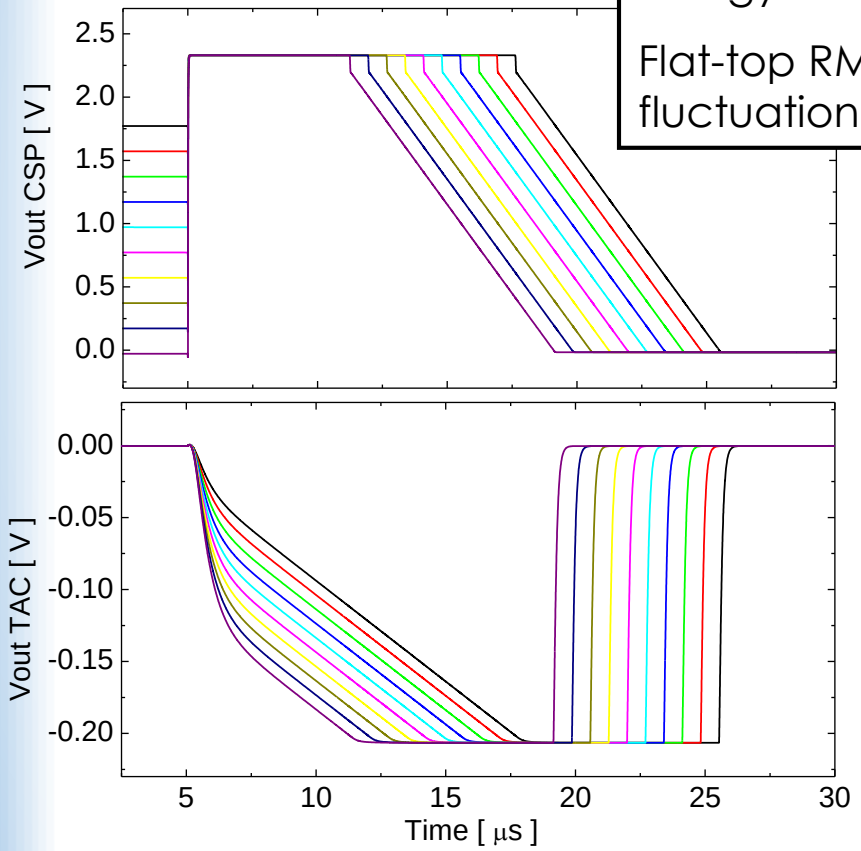



$$E_{DET} \propto V_{REF} = \alpha[kT - C_F(\langle V_2 \rangle - \langle V_1 \rangle) + c]$$

# Time-to-Amplitude Converter with correction algorithm: **SIMULATIONS**

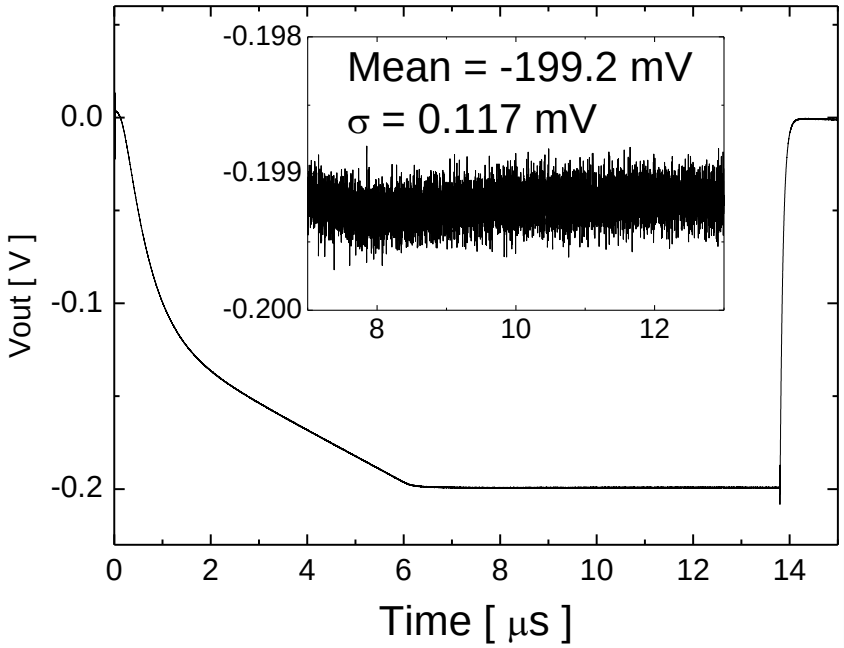
Energy = 74MeV

Flat-top RMS fluctuation 0.3%



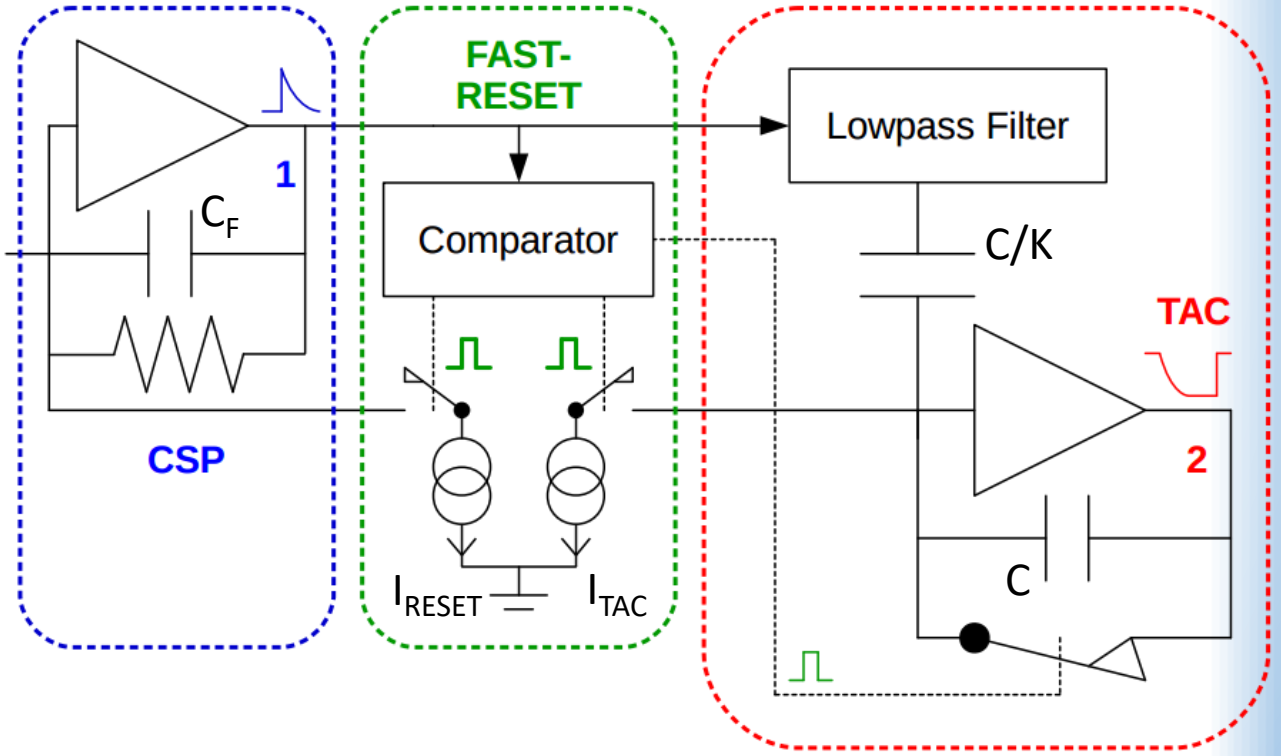

Energy = 74MeV

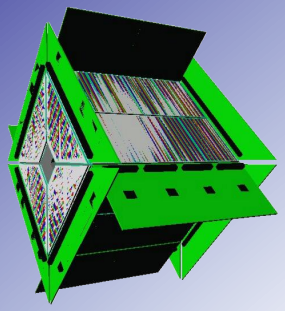
Flat-top rms NOISE fluctuation 0.1%



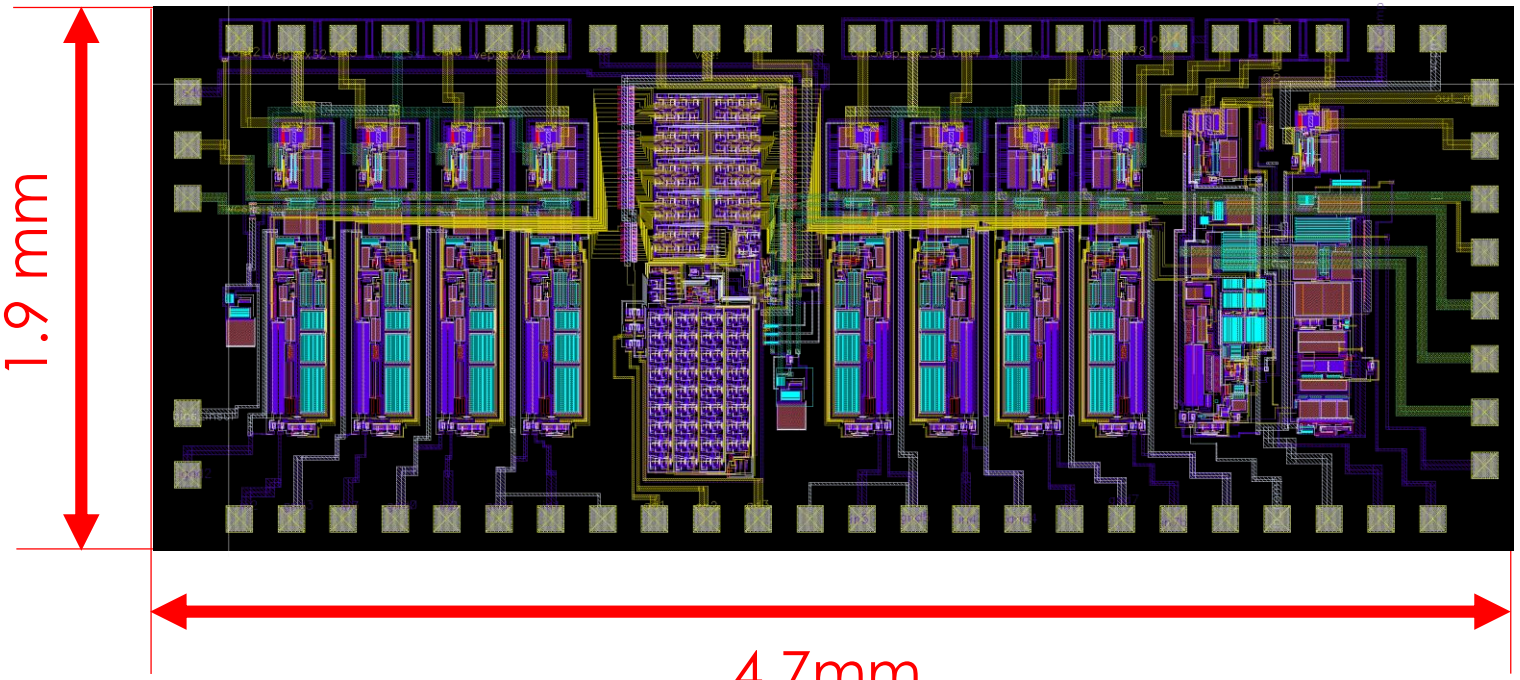
# Time-to-Amplitude Converter with correction algorithm: **CIRCUIT IMPLEMENTATION**

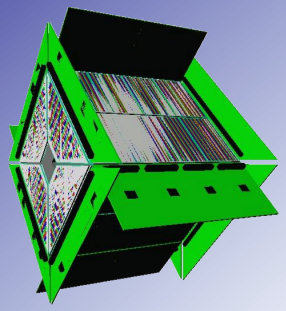
- TAC dynamic range: 400MeV
- Energy fluctuation due to electronic noise <0.1%
- Energy fluctuation due to non-ideal flat-top of the TAC signals: 0.3% @ 74MeV
- TAC Power consumption: 15mW



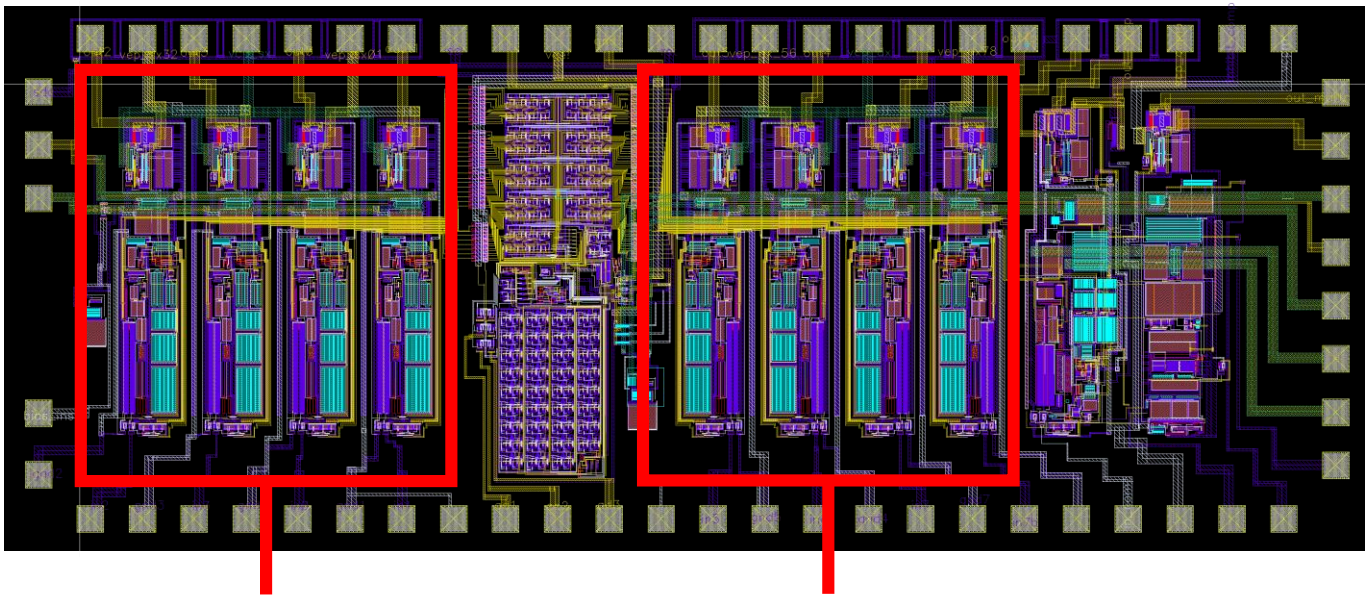


# 2016: The new TRACE ASIC preamplifier



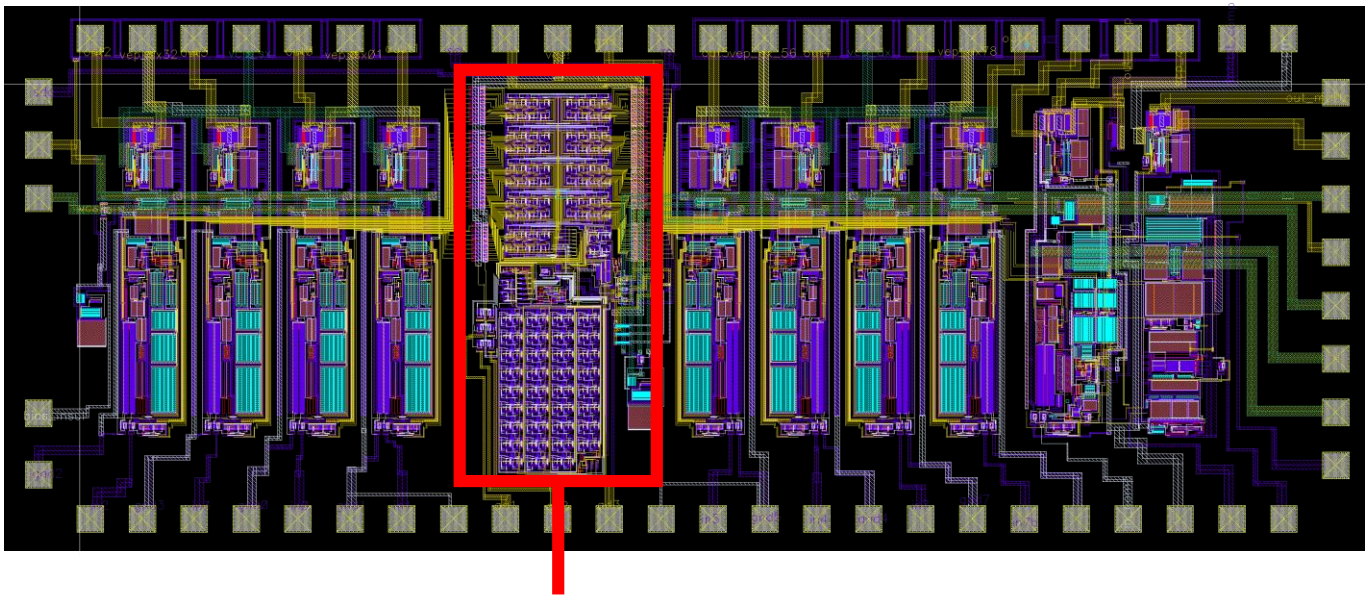


# 2016: The new TRACE ASIC preamplifier

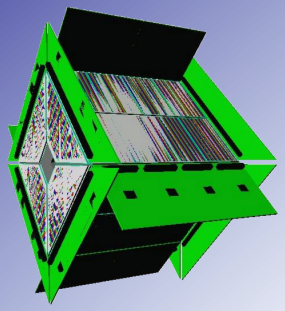


8 channels for hole signals (front pads), separately powered in groups of four

# 2016: The new TRACE ASIC preamplifier



I²C receiver



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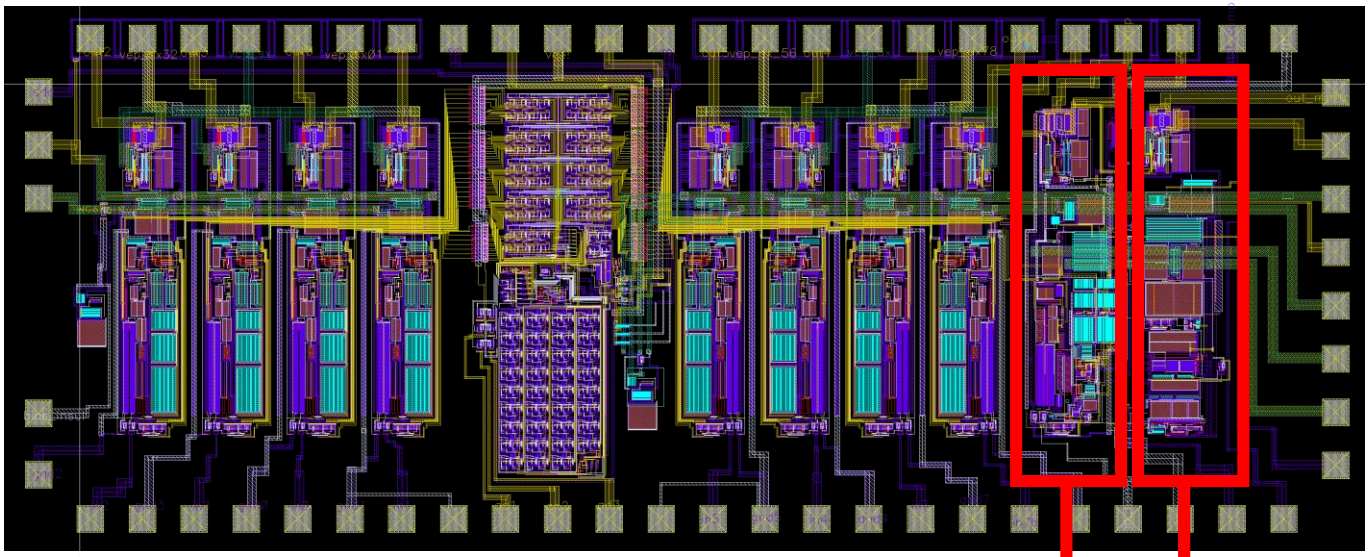
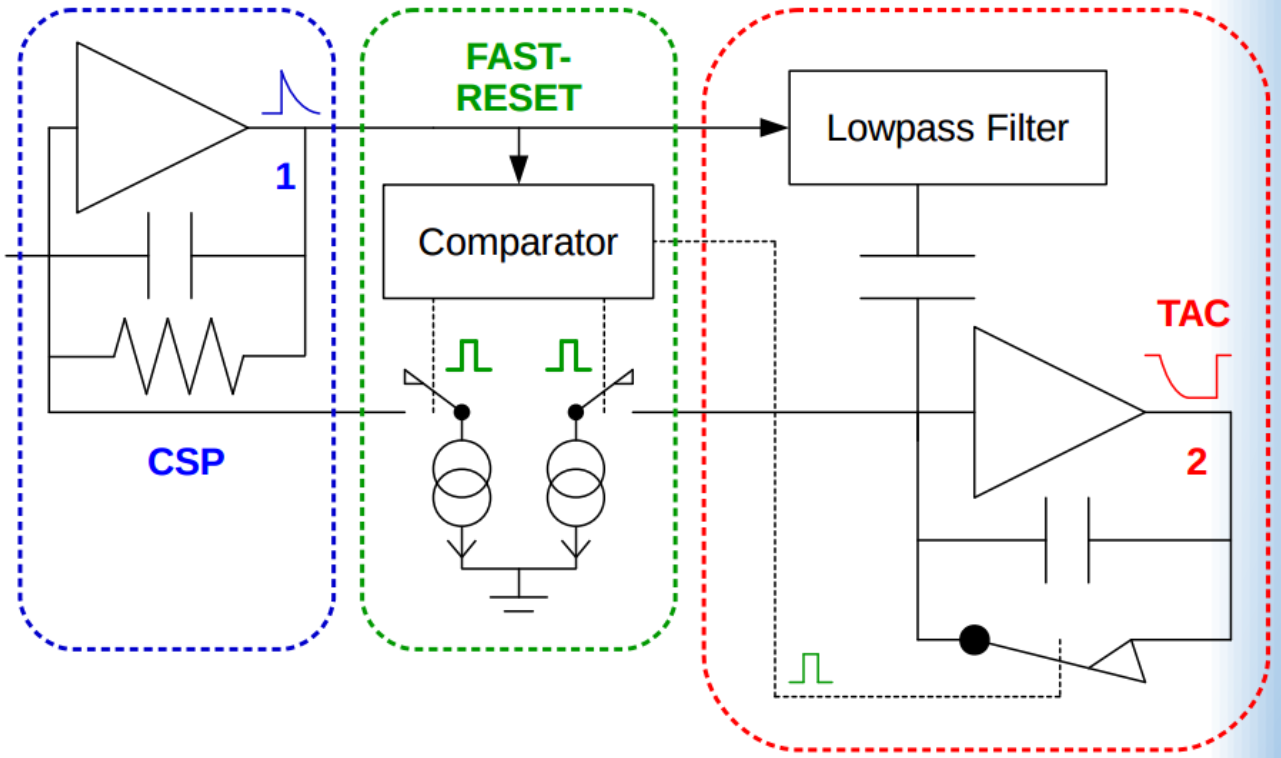


1 channel for electron signals (back)

TAC block with baseline correction circuit

# PERSPECTIVES:

- The baseline rejection algorithm suffers from a non-ideal sampling of the starting baseline in case of slow signals: the solution is to change the LPF with a S/C delay line
- The feedback resistance should be disconnected during the F/R process
- Selectable energy range for the TAC



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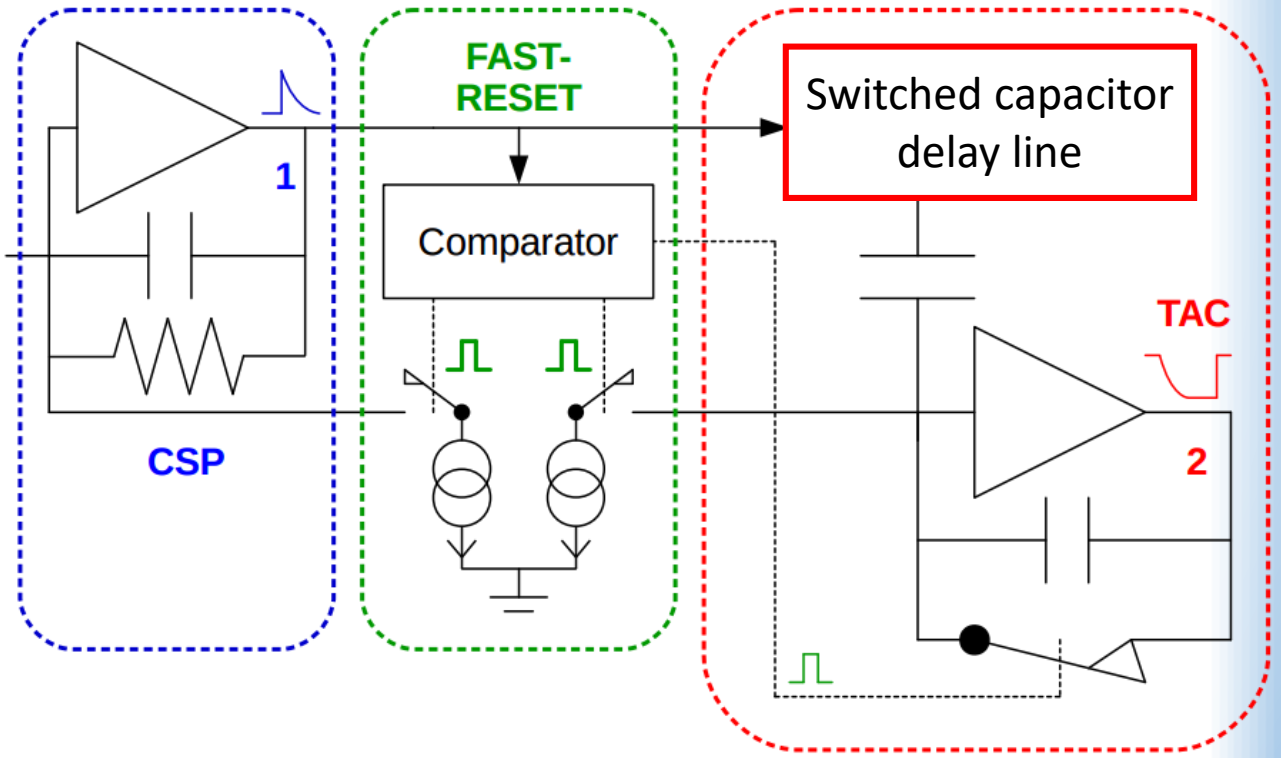

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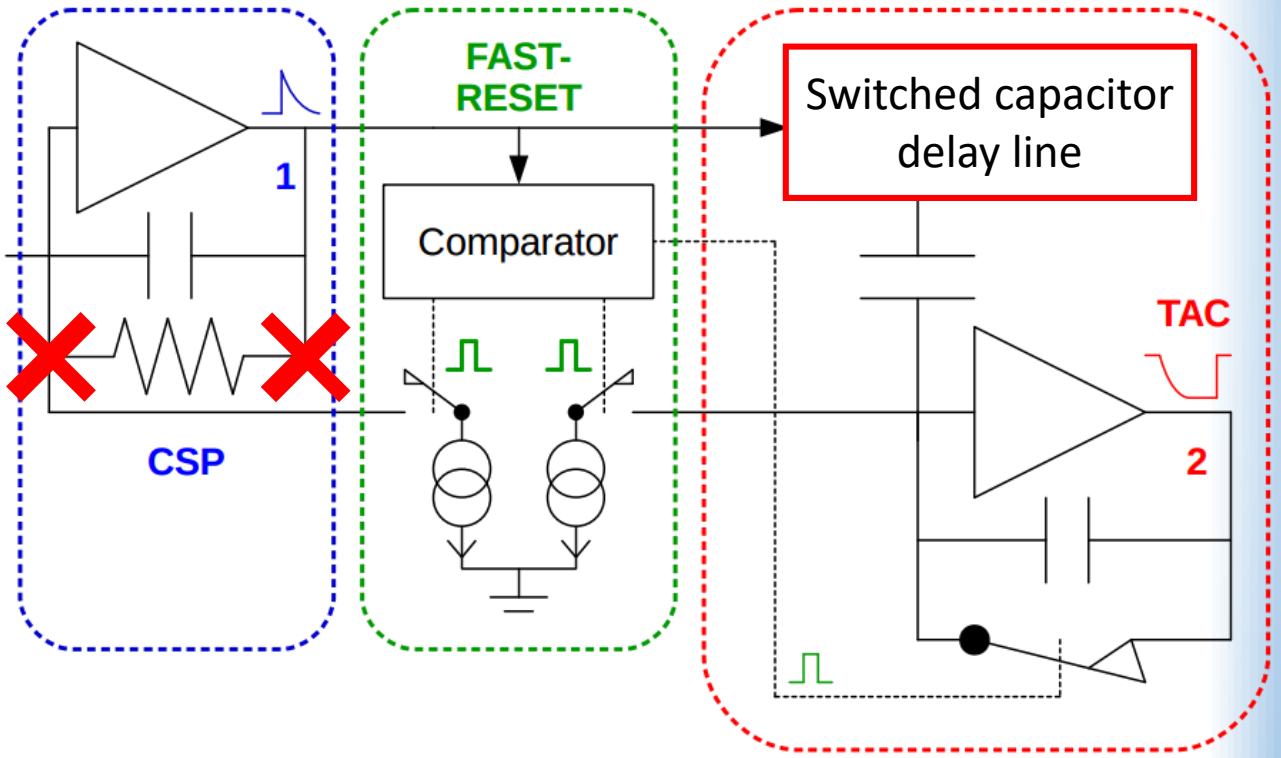

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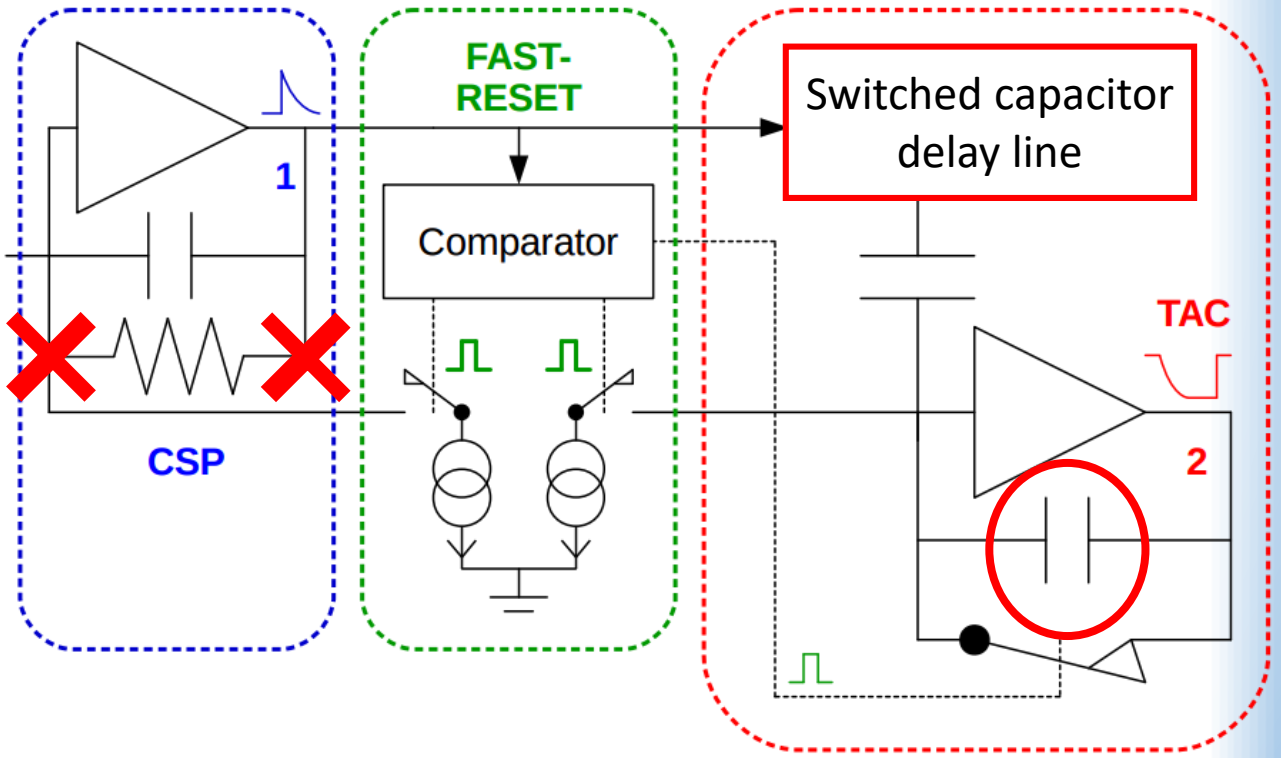
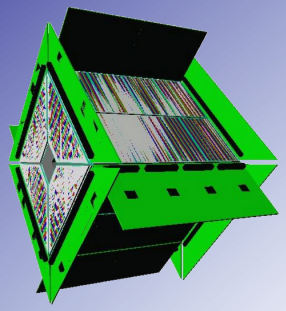
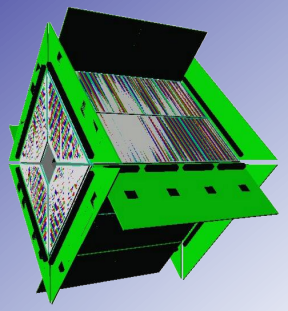




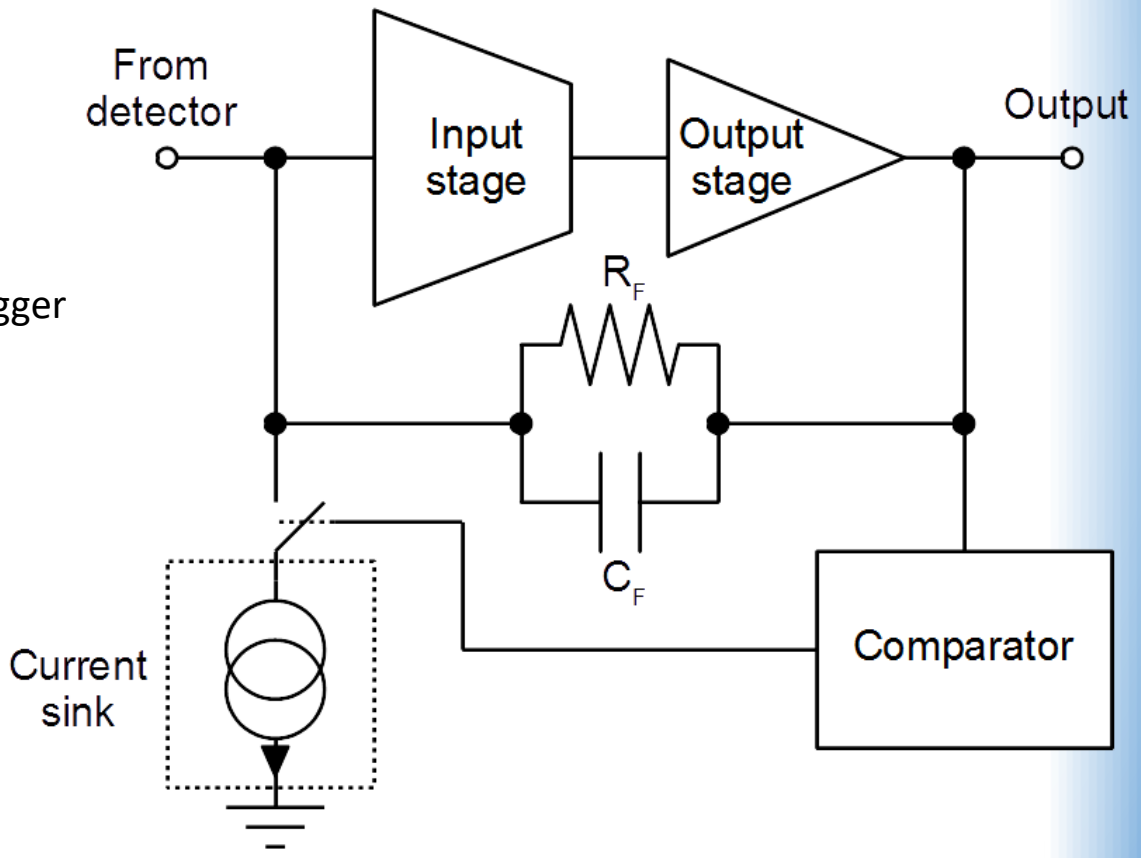


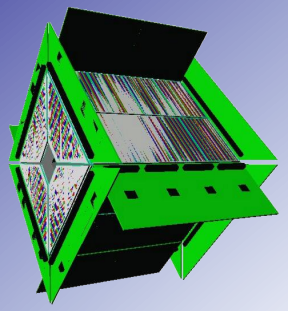
# Thank you



# Preamplifier channel block diagram

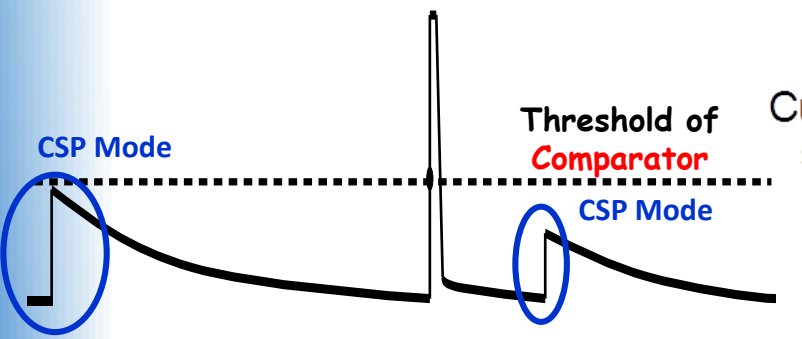
- Differential input stage with tunable bandwidth
- Low-impedance output stage
- Comparator configured as Schmitt-trigger
- Current sink to perform the fast-reset
- Discrete 0402 1GΩ feedback resistor
- Integrated, $I^2C$ adjustable feedback capacitor. It can assume the following values: 0.2pF, 0.5pF, 0.7pF and 1pF.

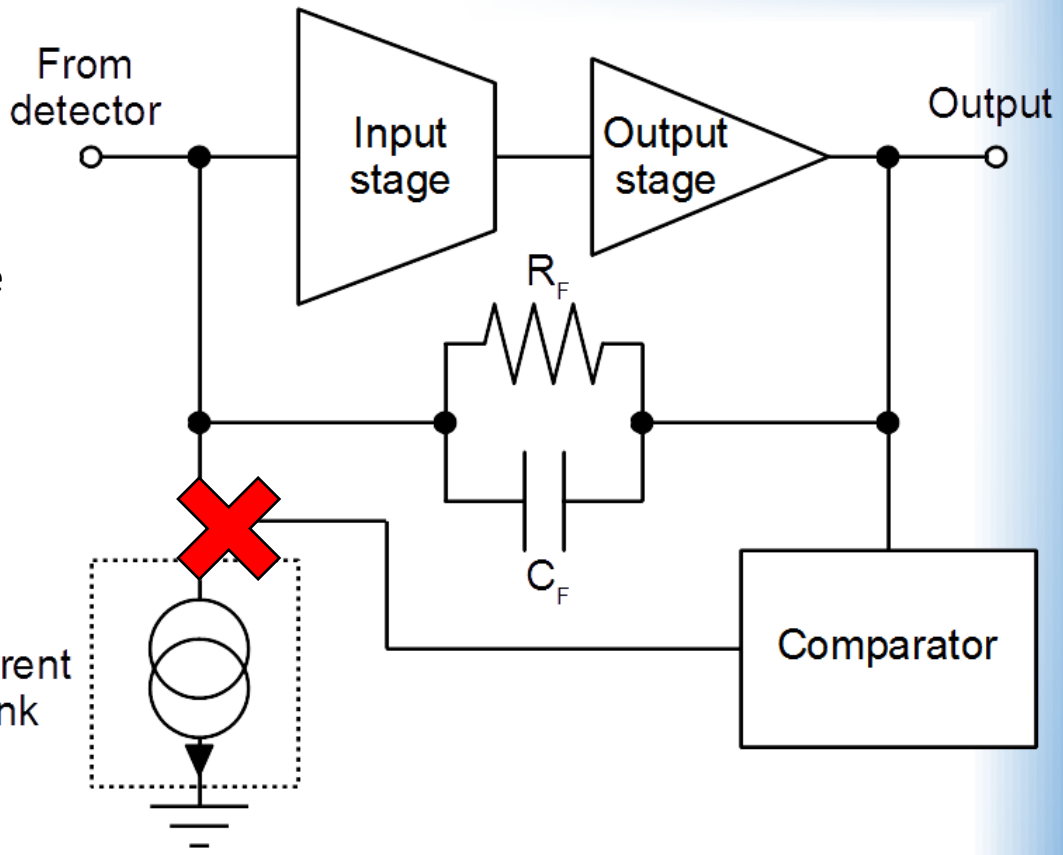


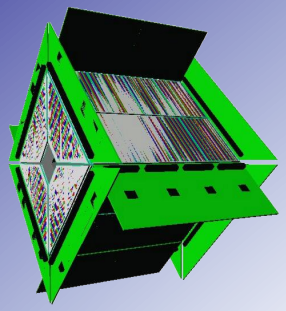


# The fast-reset technique: Charge-Sensitive Preamplifier (CSP) Mode

- For “normal” amplitude signals (up to a few MeV) the comparator keeps switch open
- The circuit is a Low-Noise Charge-sensitive preamplifier
- Allows for high-resolution energy measurements

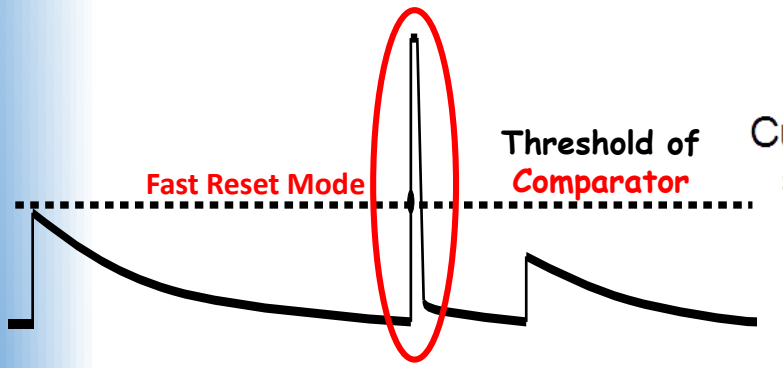


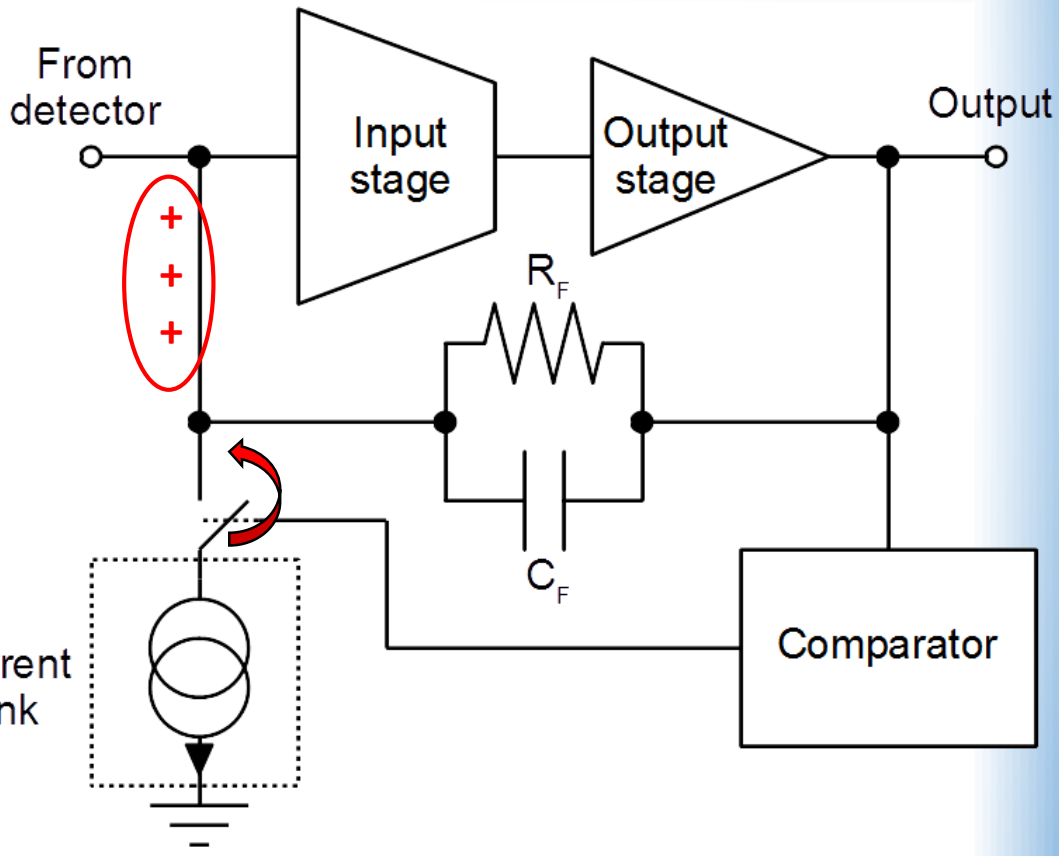



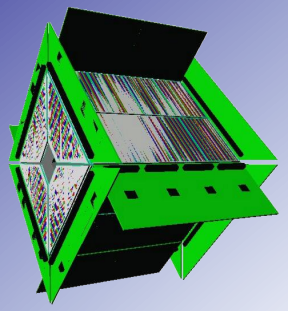


# The fast-reset technique: Fast-Reset mode

- Minimizes the preamplifier dead time and prevents from the paralysis of the acquisition system in the case of extremely high background counting rates
- Allows for charge information even in the saturation condition
- Allows for high-resolution energy measurements, extending the dynamic range of photons/particles spectroscopy

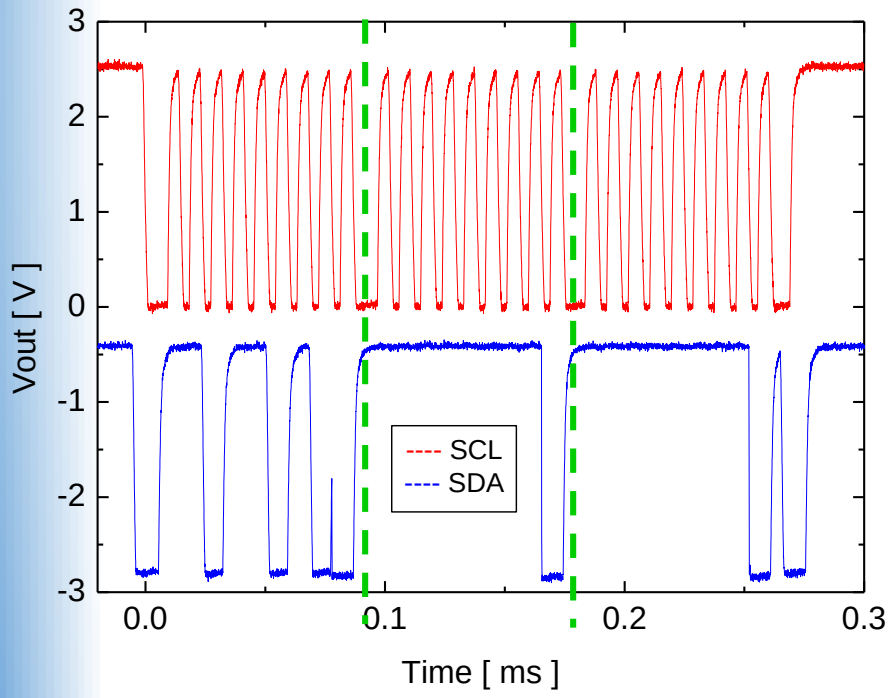


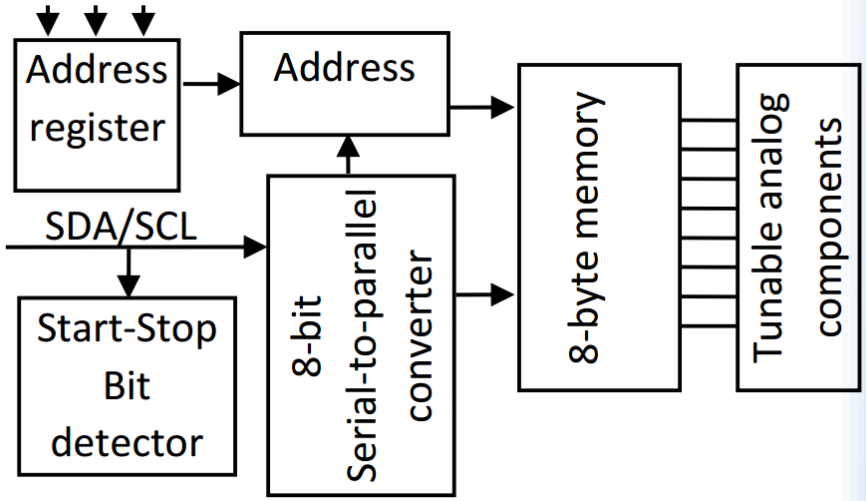


# I2C engine block diagram

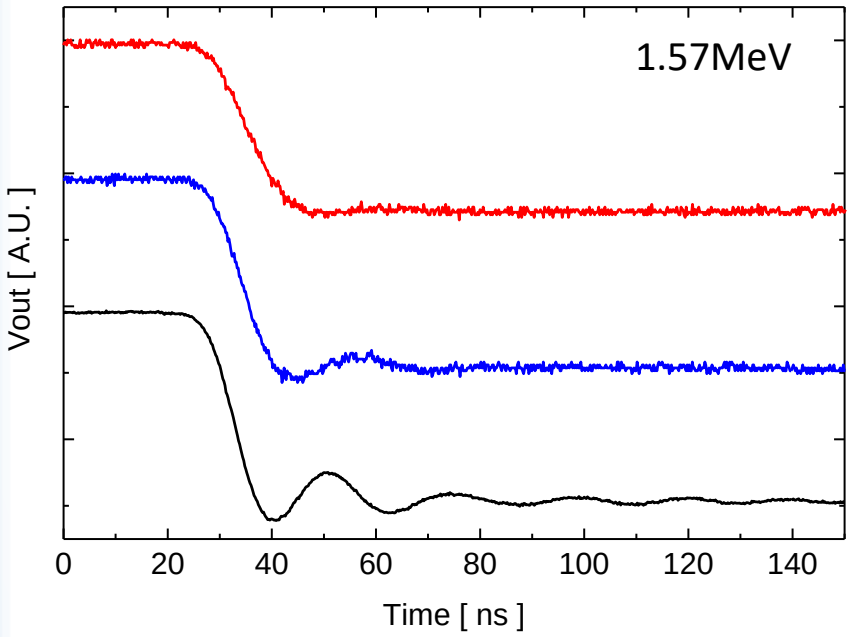
- Simple structure
- Designed to store the configuration of 8 channels on a SRAM




- Directly adjust the value of passive components through transmission gates
- Reset function to recover immediately a predefined configuration



# I2C functionality test




| $C_M$ | 3 pF | 4 pF | 5 pF |
|---|---|---|---|
| Risetime [ns] | 9.5 | 11.5 | 15.2 |