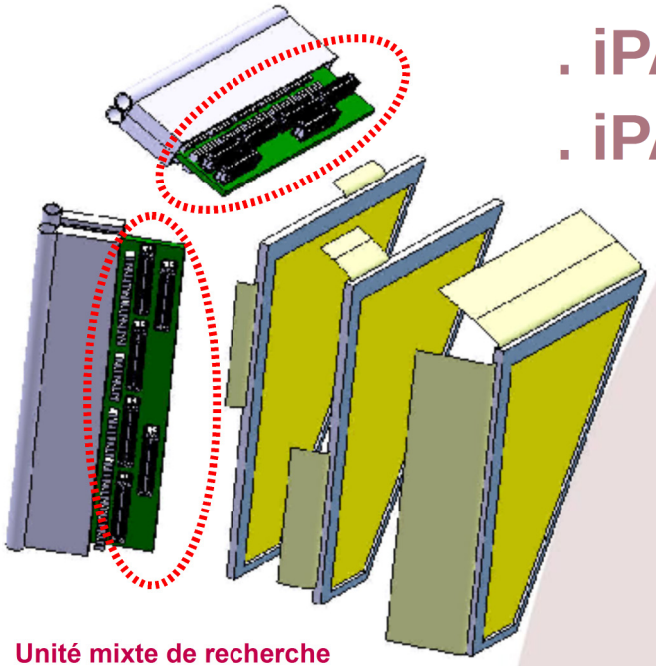
iPACI status

Tuesday 24th Jan 2017



. GASPARD and iPACI
. iPACI v1 measurement results
. iPACI v2 design progress

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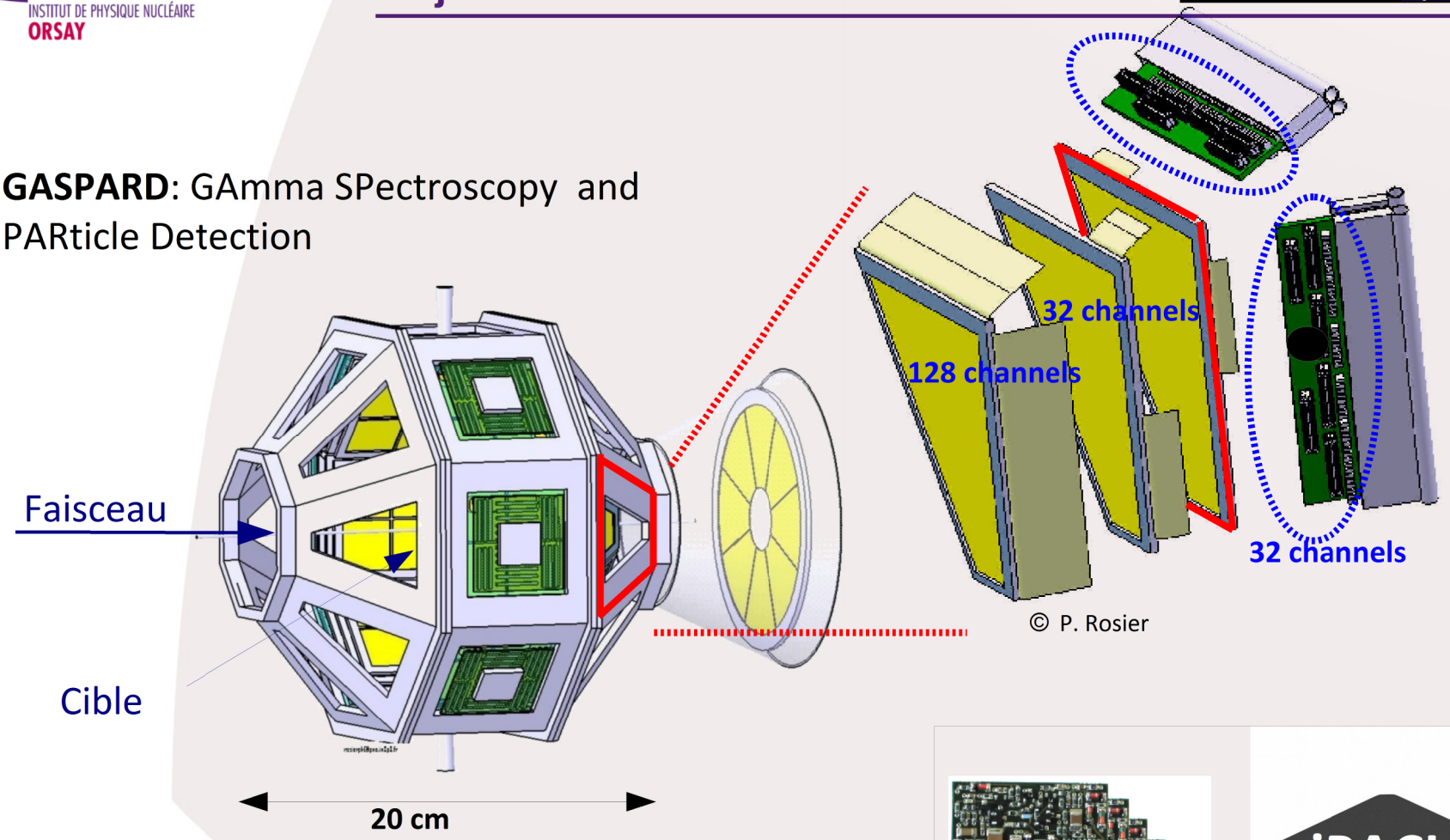
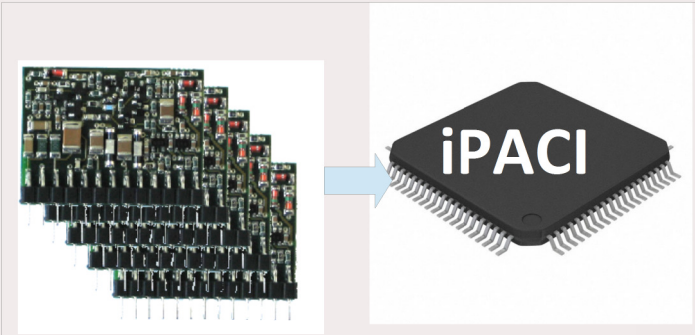
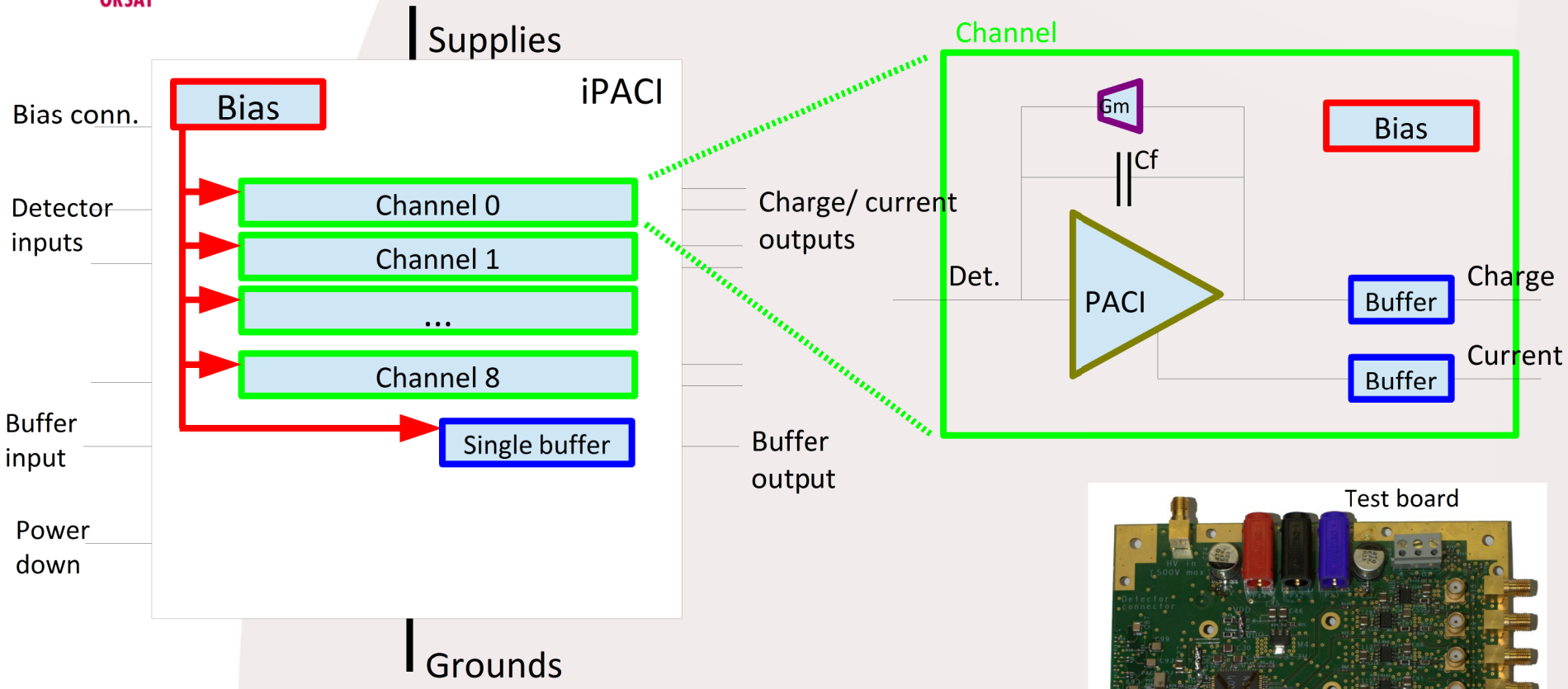
Project GASPARD

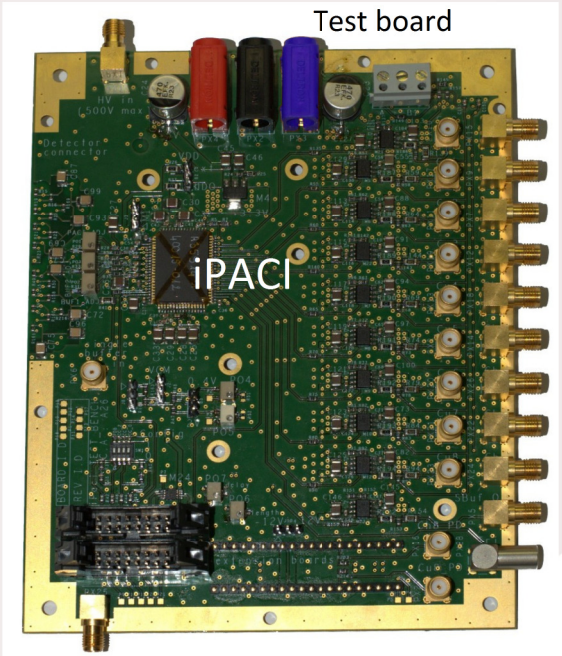
GASPARD: GAmma SPectroscopy and PARticle Detection





Architecture iPACI v1





Results and perspectives - iPACI v1

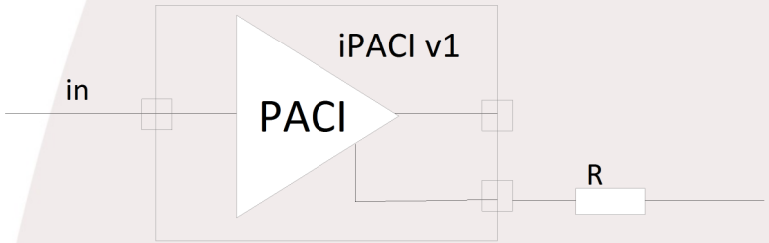
Measured with generator:
. 30mW/ch on 3.3V supply
. Charge Gain : 36.4 mV/MeV
. Current Gain : 8317 Ohm
. 50MeV linearity (< 1% INL)
. 12keV FWHM resolution (baseline) with detector
. 130MHz AC system BW with 20pF input load
. 83nA RMS on [1k, 10MHz] on Current output... (?)

Measured in alpha:
. 40keV FWHM with actual detector (still trying to improve the figure)
. 26keV FWHM with test detector

Measured on beam:
. Oscillations issues in May 2015. No useful data.
. Beam test to be done again with modified setup:
- Current output BW limitation
- Differentiation of the Charge output

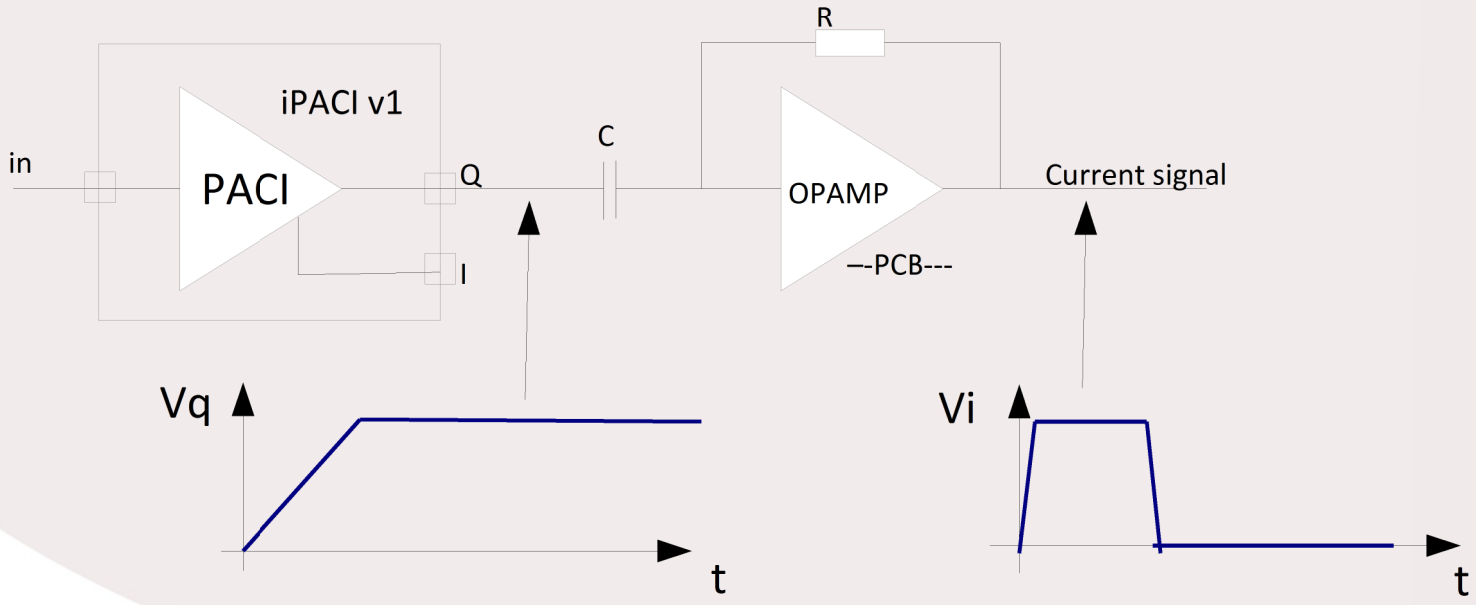
Results and perspectives - iPACI v1

1. BW limitation on the current output



Limits inrush current through the Current output and thus limits risk of oscillations

2. Differentiation enables generation of a current signal on PCB

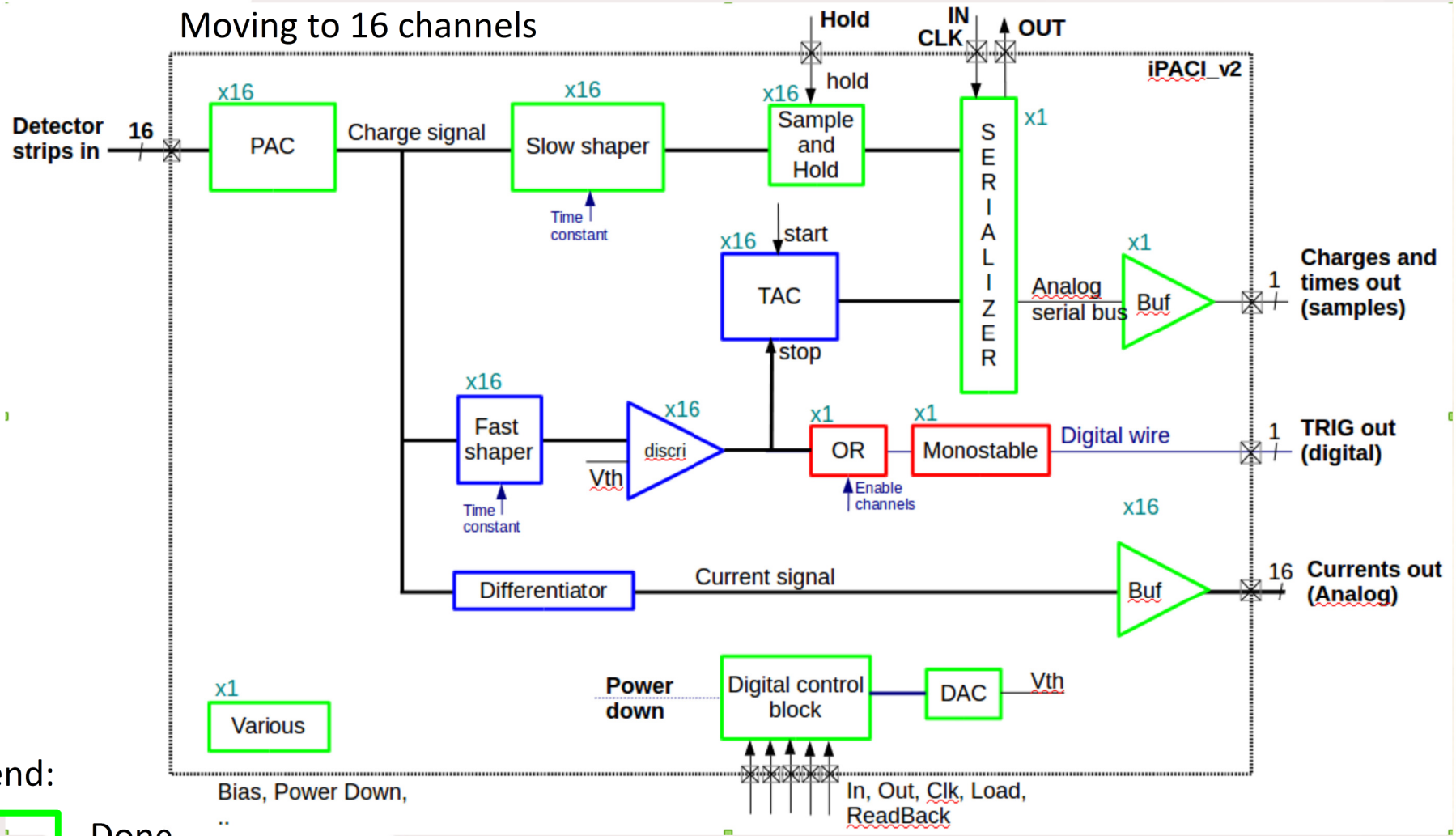


Preferred solution !

IPACI v2 architecture

Integrate: slow shaper, S/H, serializer, …

Moving to 16 channels



Legend:

- Done
- Started
- To be done

IPACI v2 status

Performance (simulated):

- 70meV / 200MeV modes

- About 15keV FWHM resolution on the charge path (after 400ns internal analog shaper)
- 150 MHz BW
- About 15 mW/ch consumption
- 17nA RMS on current output [1k, 10MHz]. PACI was 13.5nA

Stability issue:

- We'll get oscillations with 16 channels ON at the same time.
  – Need to plan for external differentiator option

Next runs:

- End of February 2017
- Beginning of June 2017

Questions ?

iPACI v1

GASPARD architecture

Differentiator circuit desigr

iPACI v2

iPACI v1 performance (Linearity, BW, Resolution)

Baseline noise vs Alpha resolution

Reliability issue

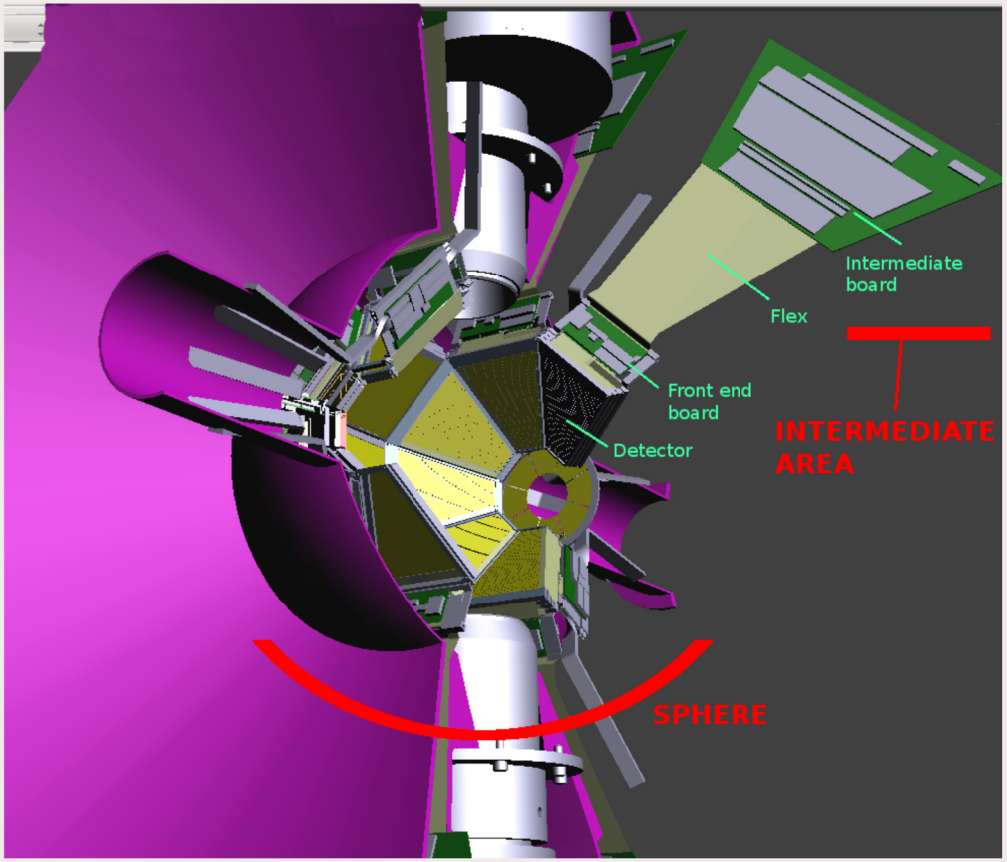
Oscillations

Architecture study – Option 1 - Reminder

Purpose of study was:
Propose architectural options for GASPARD electronics and derive:
- Functionality
- Performance
- Area requirements
- Consumption involved
- Planning & cost

Check feasibility vs Mechanics and Physics

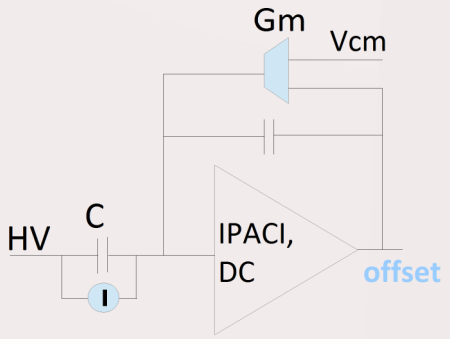
Proposed:
- System architecture
- ASIC architecture
- Consumption quote
- Area quote



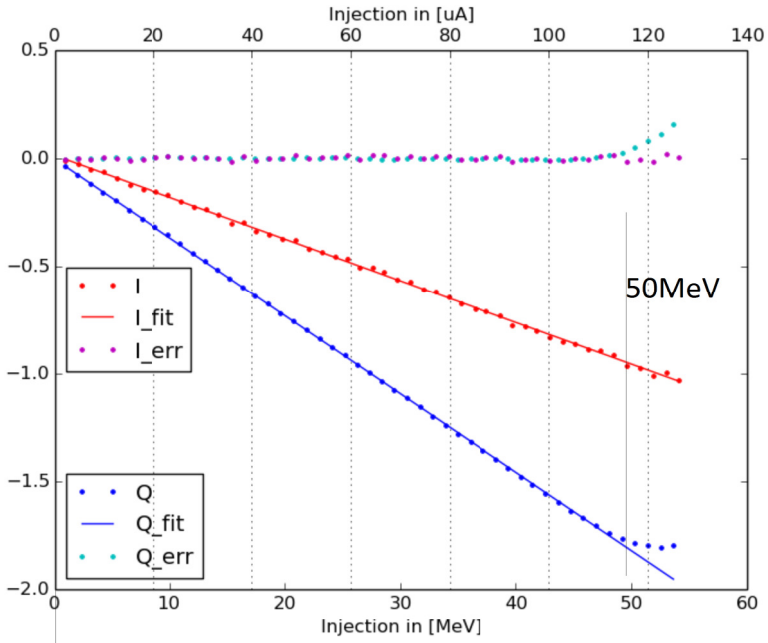
Status
-No progress. Data still available if requested

IPACI v1 / iPACI_TB – Tests results

Various Many blocks behave ok, including:
- Bias system (based on a external resistor and Bandgap)
- Power down (can keep only 1 channel ON for power saving)
- Slow control (home-made SPI link)
- HV behaviour (Board stands up to 500V)
- Leakage through DC-blocking caps (<< 10nA)



Performance : 50MeV ok, with less than 15 keV FWHM noise



Measured I/Q voltages (V)

Automated measurement on a test pulse (20ns rise time, sweeped amplitude)

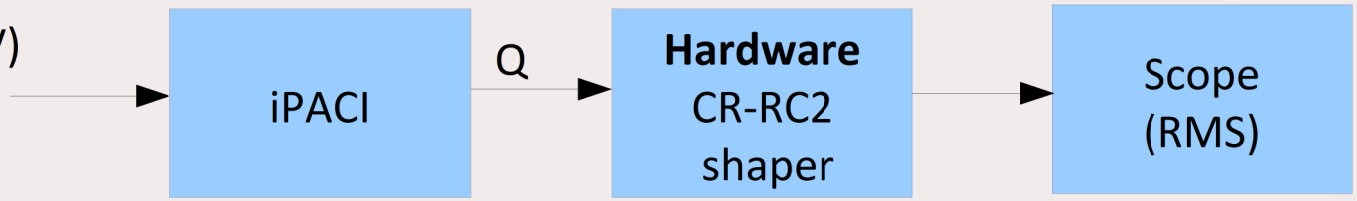
Charge Gain : 36.37 mV/MeV
Current Gain : 8317 kΩ

IPACI v1 / iPACI_TB – Tests results

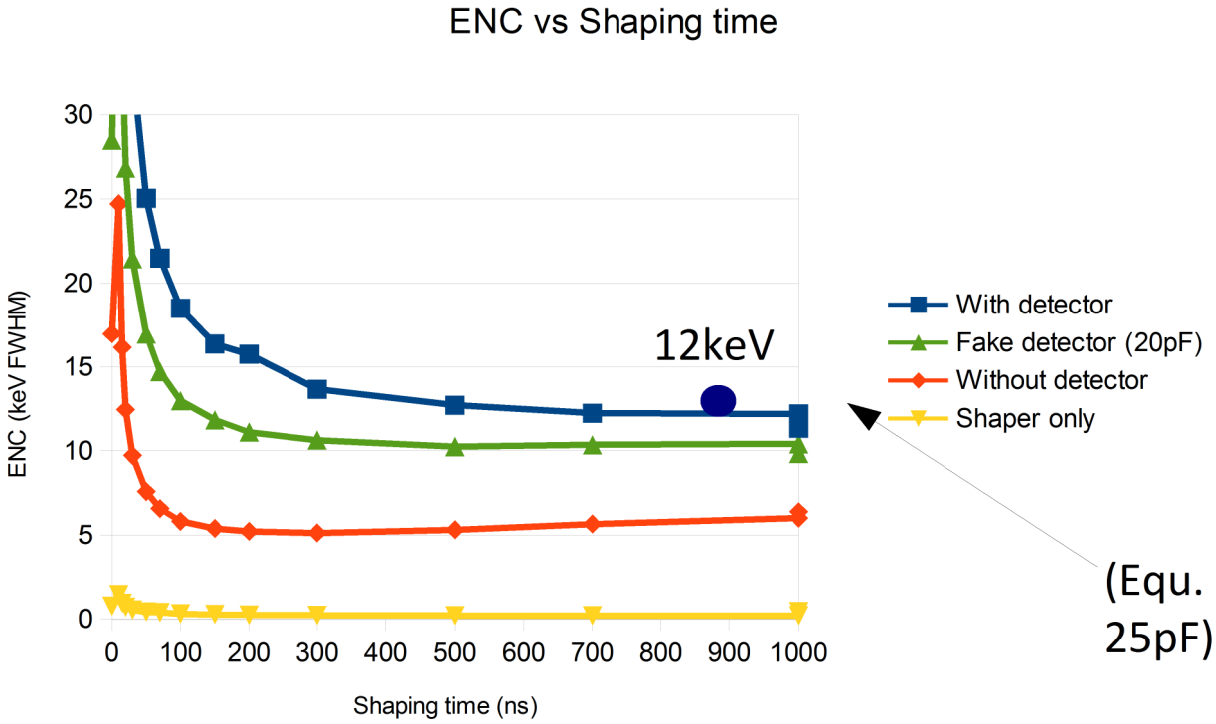
Schematic:

- Actual detector (200V)
- Fake detector
- Nothing

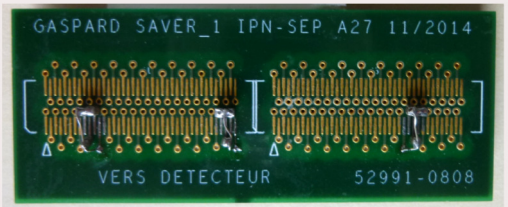
Measurements on **Noise only.** No signal !
Gain calibration done for each **Shaping time** step



BW: 1kHz – 250MHz
(1ms @ 500MSa/s)



Fake detector: PCB loading each preamp input with 20pF caps.

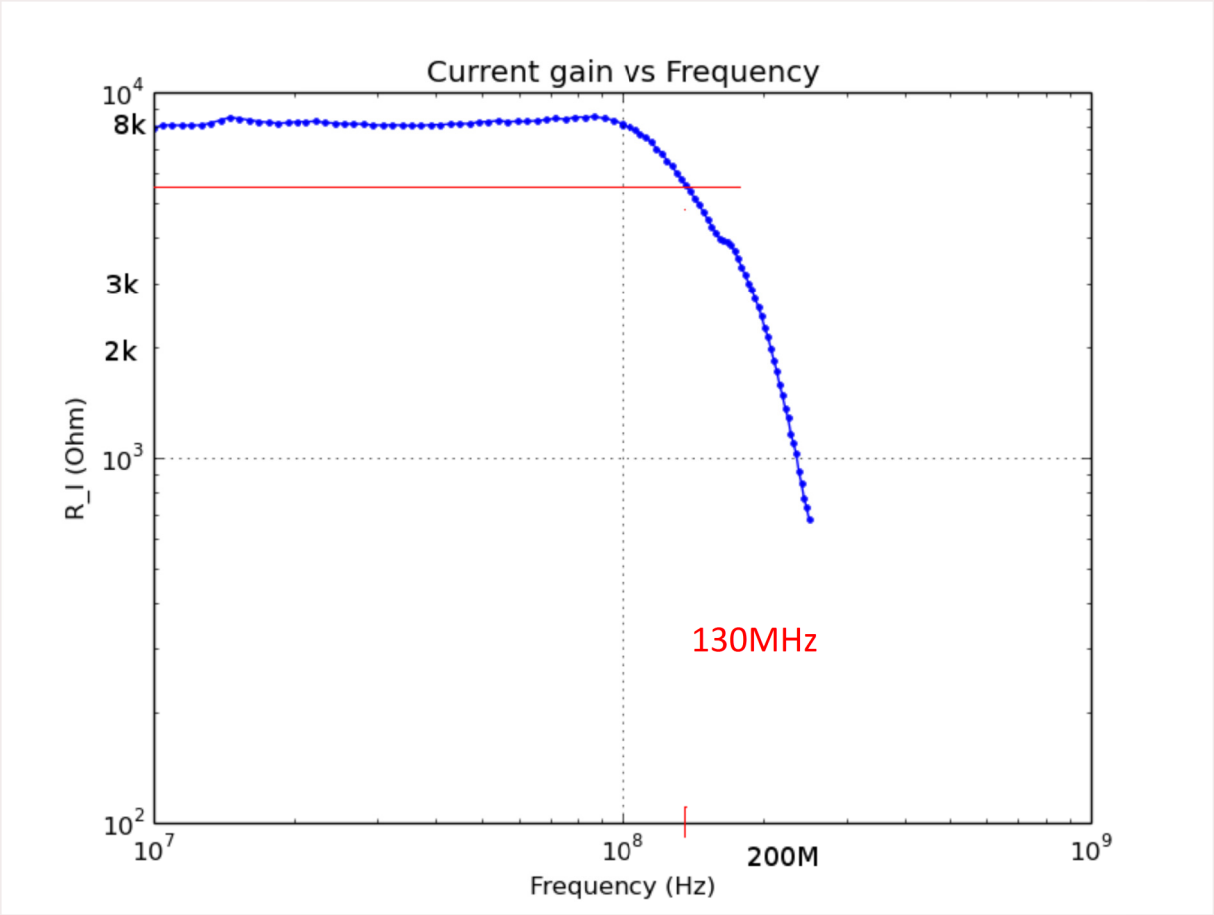


IPACI v1 - System BW

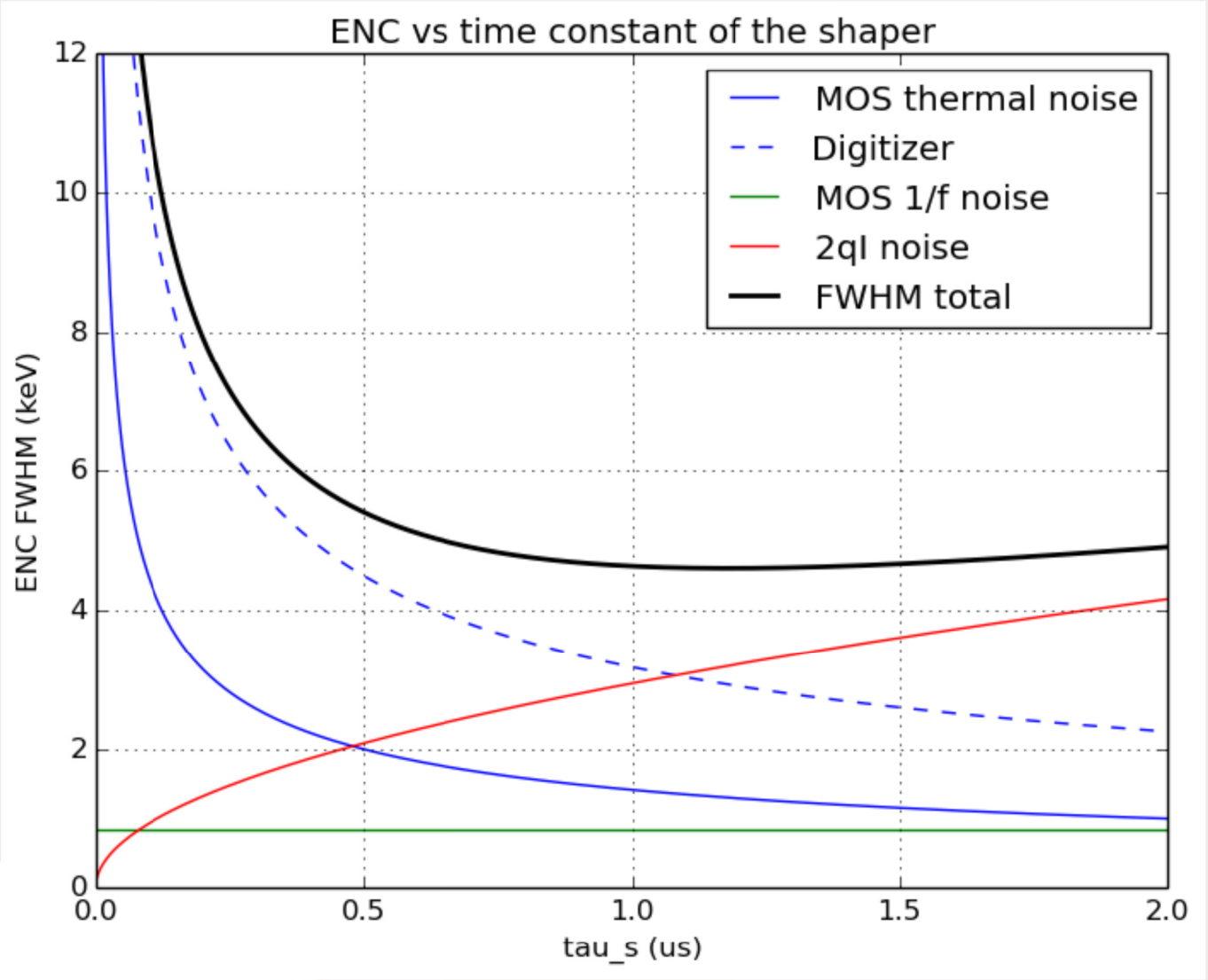
Large signal BW:

BW = 2.2 / (2*pi*tau)
= 81MHz (50MeV)
= 88MHz (5MeV)

Small signal BW:

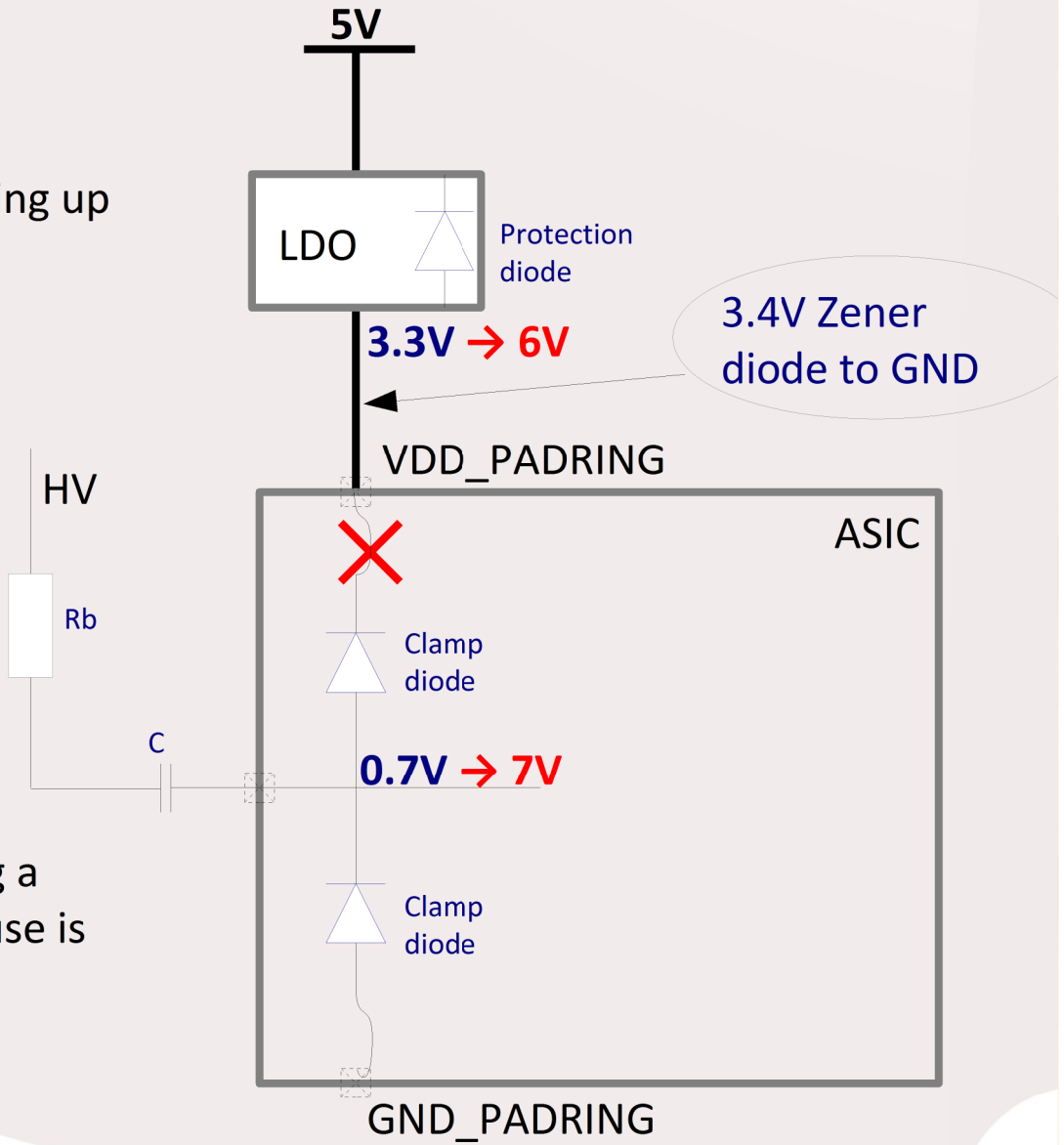


Backup – Shaper output noise vs Shaping time



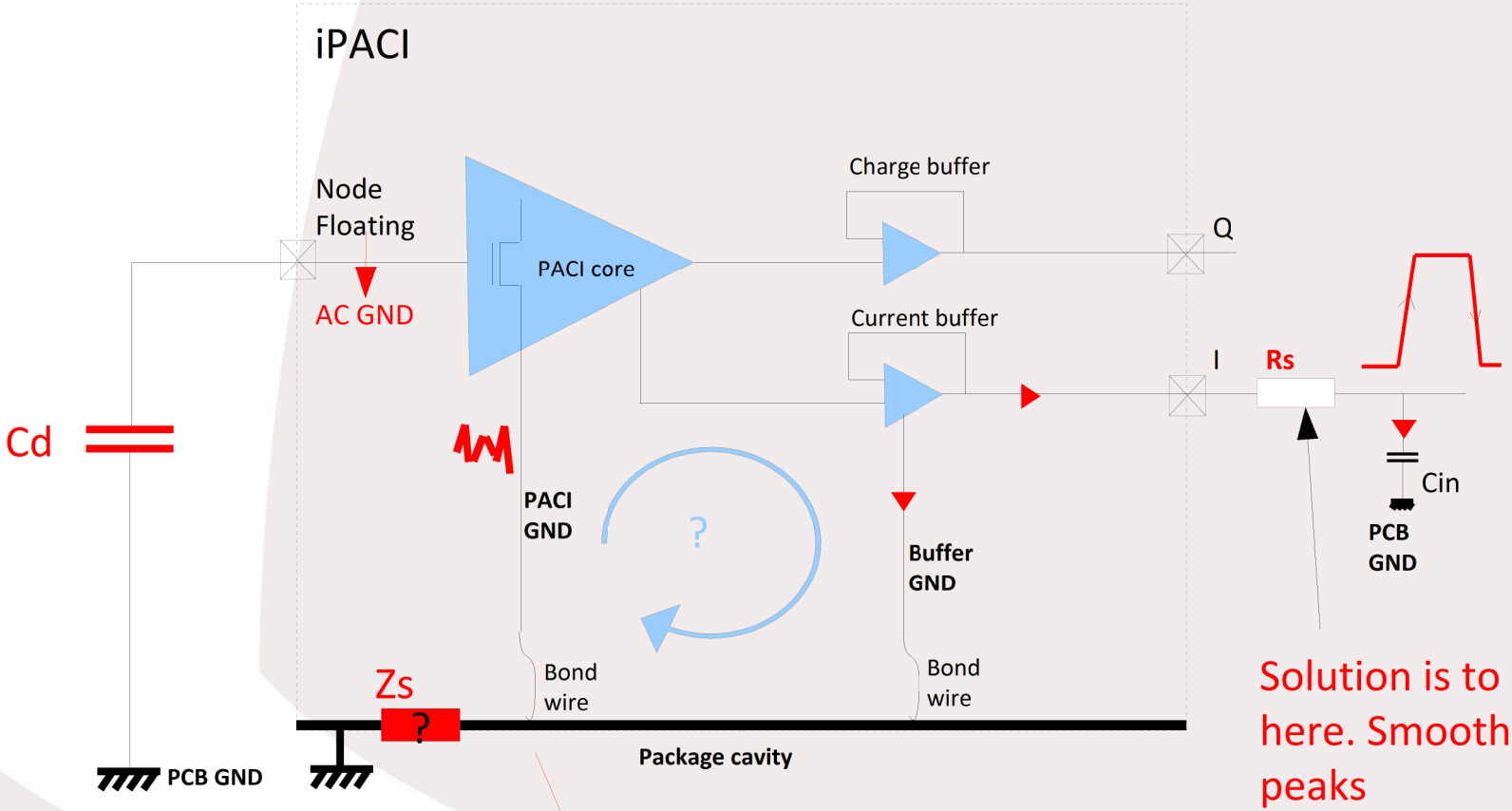
- Reliability

  Many chips damaged while ramping up (or down) the HV bias



- Issue seems solved after inserting a zener diode on VDD node but cause is not fully understood.

- Oscillations when detector present

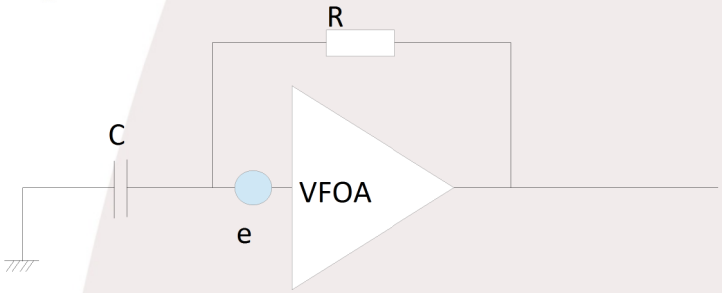


Solution is to add resistor here. Smoothens the current peaks

We should try to bond it directly to the pin
And utilize more bond wires

IPACI – Differentiator

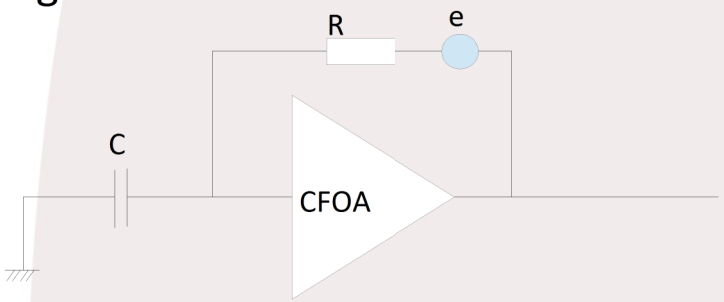
1. Using a VFOA



$$stb(\omega) = G(\omega) \cdot \frac{1}{1 + jRC\,\omega}$$

2kR, 1pF → pole at 80MHz, right in-band!
=> Always unstable!

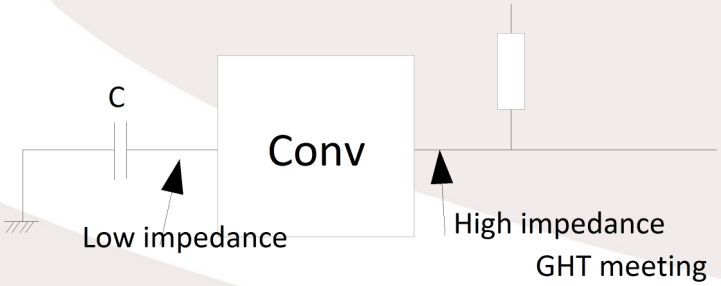
2. Using a CFOA



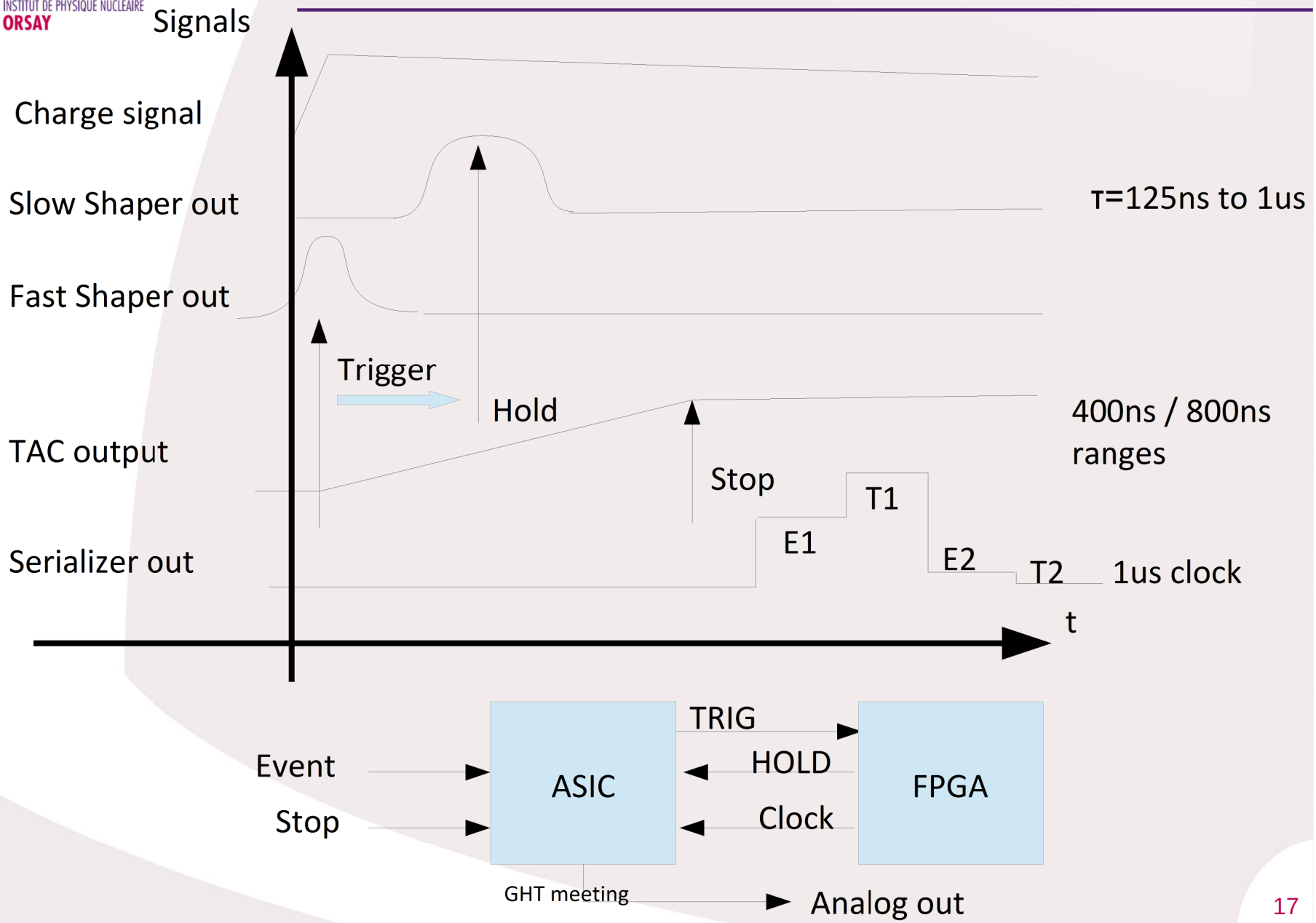
$$stb(\omega) = \frac{1}{1 + \frac{R}{Z_t(\omega)}}$$

Stability is independent of the R.C constant
(under the hypothesis that input impedance is low!)

3. Using a current conveyor



Open loop system, always stable


Signals
Charge signal
Slow Shaper out
Fast Shaper out
TAC output
Serializer out
τ=125ns to 1us
Trigger
Hold
Stop
400ns / 800ns ranges
T1
E1
E2
T2
1us clock
t
Event
Stop
ASIC
TRIG
HOLD
Clock
FPGA
GHT meeting
Analog out