PLAS: Analog memory ASIC

Status report

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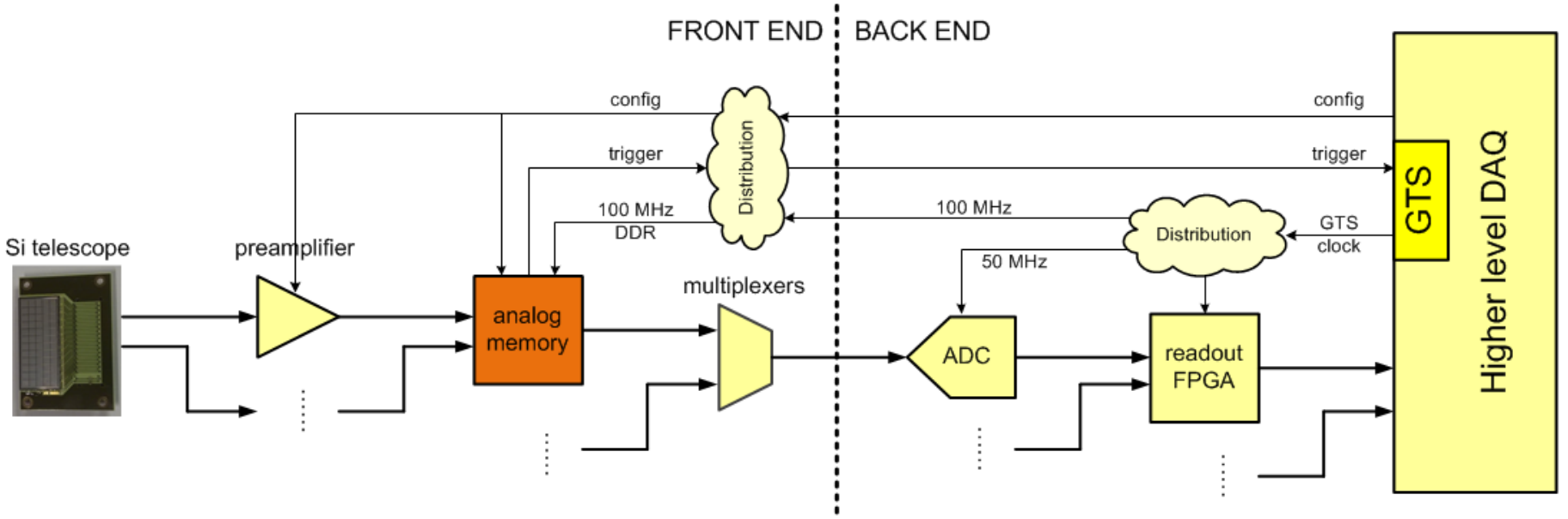
GHT Workshop – IPN Orsay

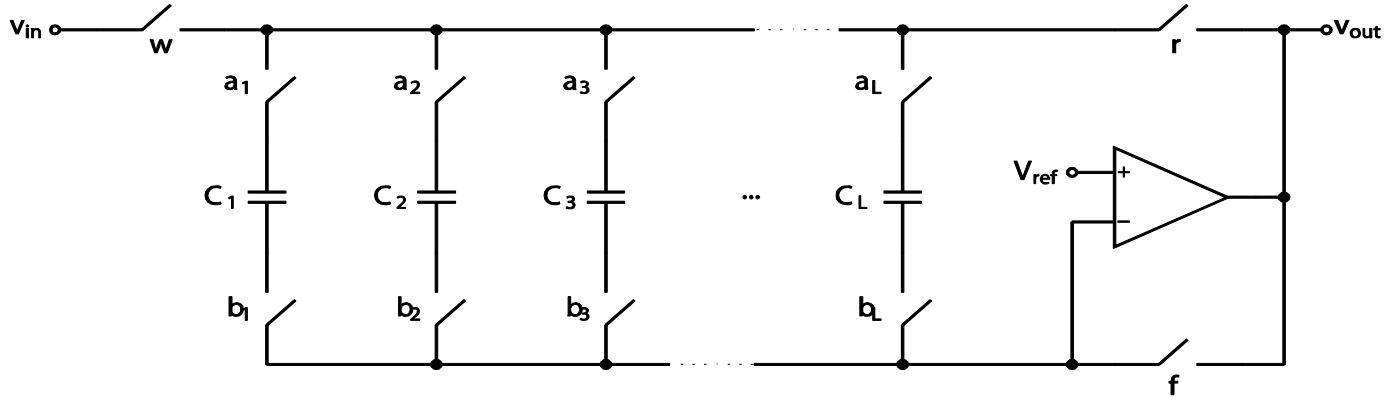
Purpose of PLAS



- Front-end circuit, receive preamp signals
- **Generate trigger** request
- **Sample** valid pulses, **zero suppression**
- **Serialize** output
- Minimize deadtime
- Minimize power consumption

⇨ **Analog memory**

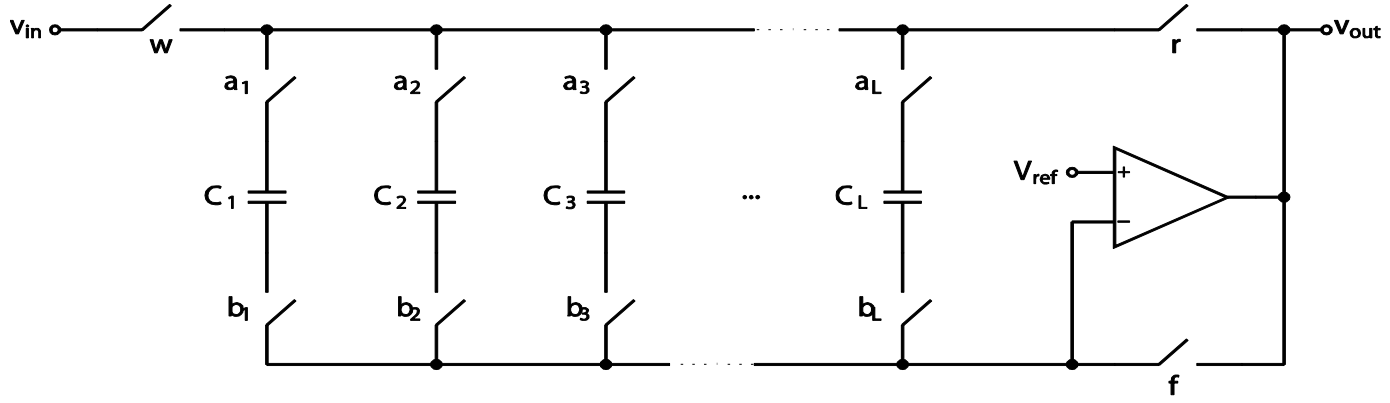
Classic analog memory structure



Switched Capacitor Array (SCA)

- Capacitors charged consecutively, **high write frequency**
- On trigger, SCA is stopped and contents are held
- **Slow read frequency**, voltage digitized externally
- SCA is replicated for each input channel

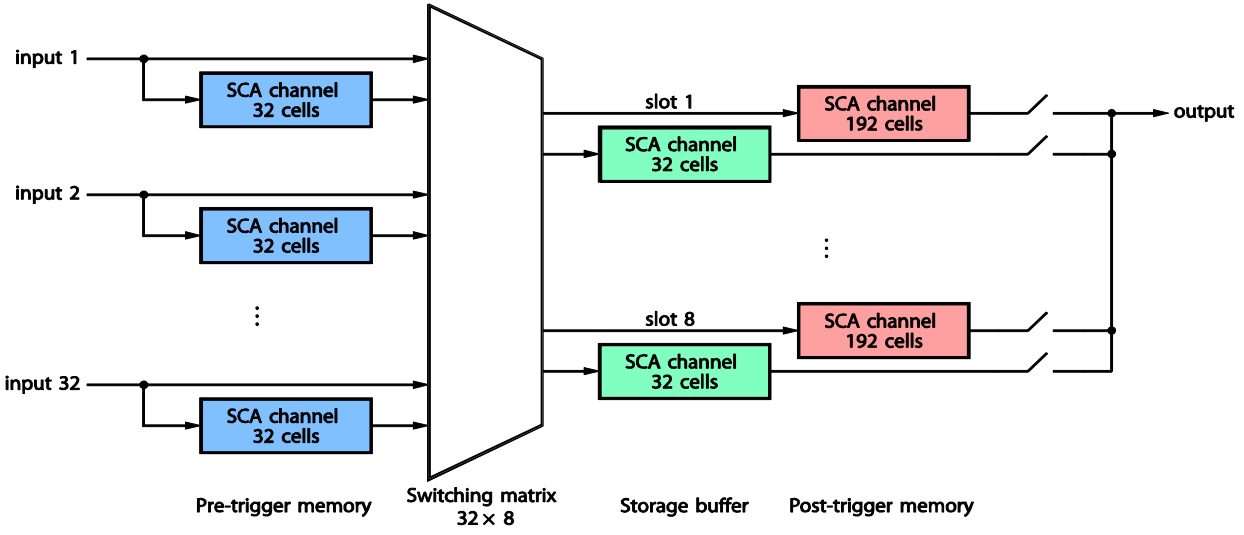
Classic analog memory structure



Switched Capacitor Array (SCA)

- **Problem:** SCA cannot be rewritten until read out
- Low read frequency implies **very long dead time**
- Existing solutions:
  - Partial readout
  - Replication

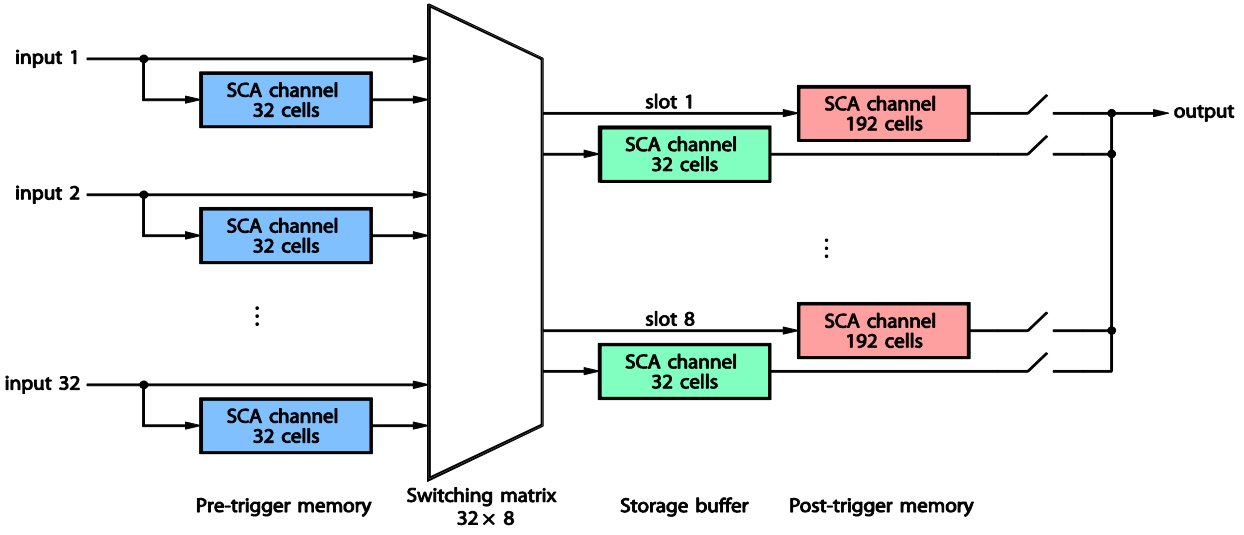
New analog memory structure



PipeLined Asymmetric SCA (PLAS)

- Split the memory into two sequential SCA stages
- Stage 1: Many **short SCAs** for **pre-trigger** samples, one per input
- Stage 2: A few **long SCAs** for **post-trigger** samples, **shared**
  - Include **buffer SCAs** where contents of stage 1 are transferred

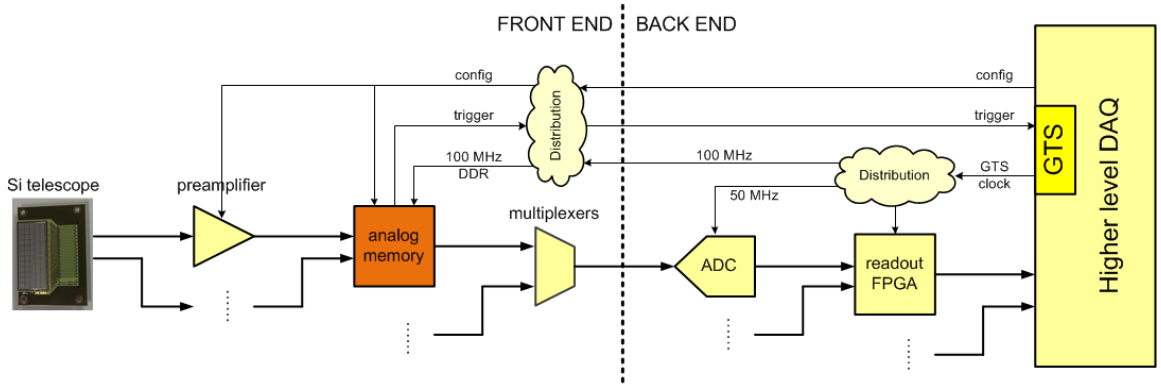
New analog memory structure

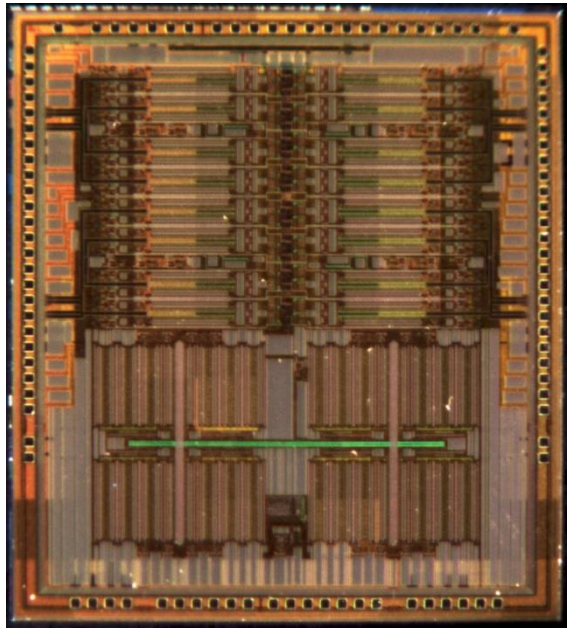


PipeLined Asymmetric SCA (PLAS)

- Advantages:
  - **No deadtime**
  - Smaller circuit (less capacitor cells)
- Disadvantages:
  - Calibration more complex (needs path through both stages)

PLAS 1.0 specifications

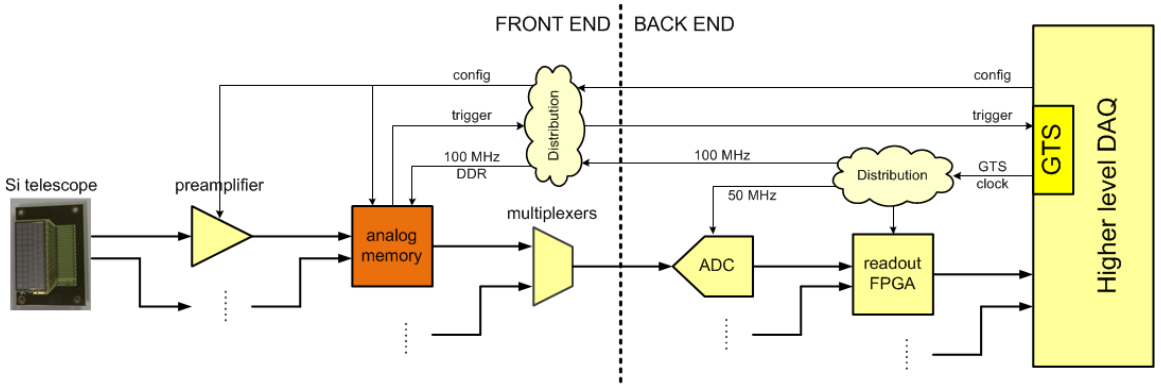




General information:

- 0.18 µm CMOS technology
- Die size 3.5 mm × 3.9 mm (32 channels)
- 1.8 V power supply
- I2C configuration interface
- Low power (12 mW/channel, measured)
- Low noise (11.9 ENOB, simulated)

PLAS 1.0 specifications



Pulse capture:

- **32 inputs** with independent trigger
- Generates common Trigger Request
- Samples at **200 MHz**
  - Both edges of 100 MHz clock
- **224 samples** captured per pulse
  - **32** before trigger, **192** after trigger
- **No deadtime**

Memory readout:

- **8** output queue slots
- **Single analog output** (differential)
- Serial readout at **50 MHz**
- Needs external ADC
- Designed for **triggerless** readout
- **Generates timestamp** for pulses
  - Synchronizable with each other and/or GTS

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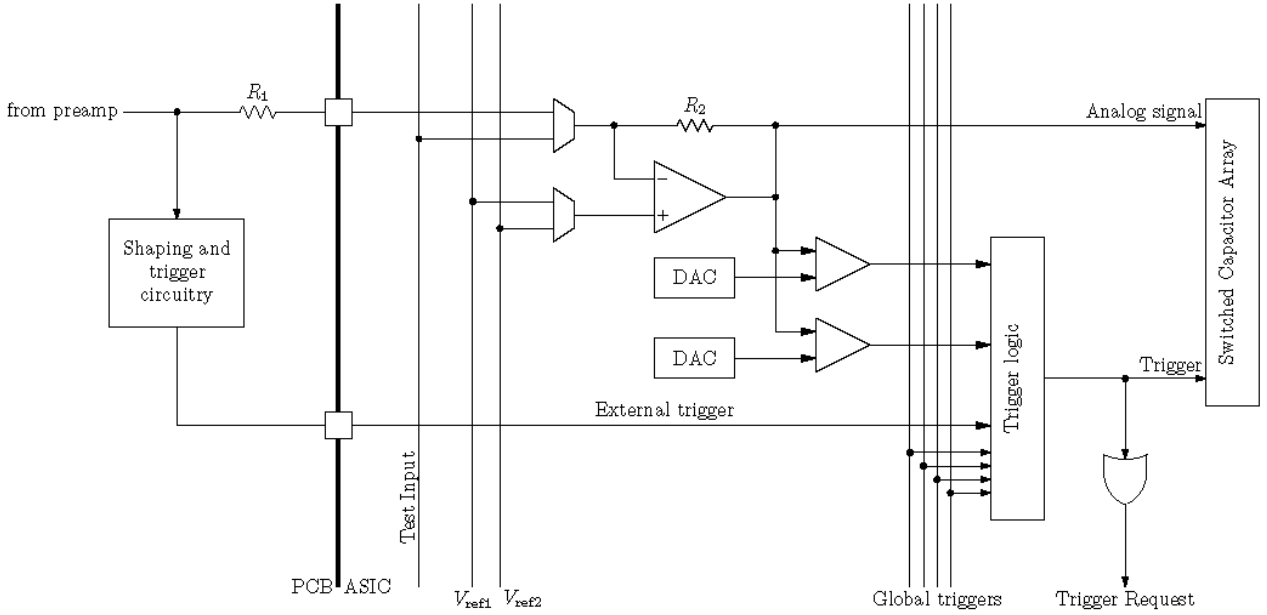
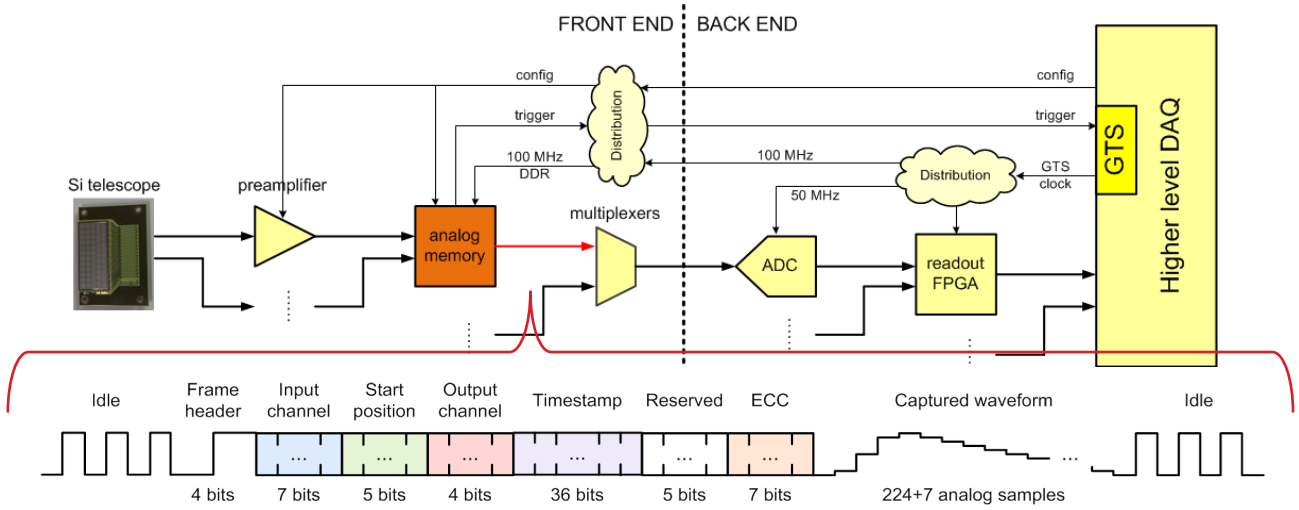
Input stage



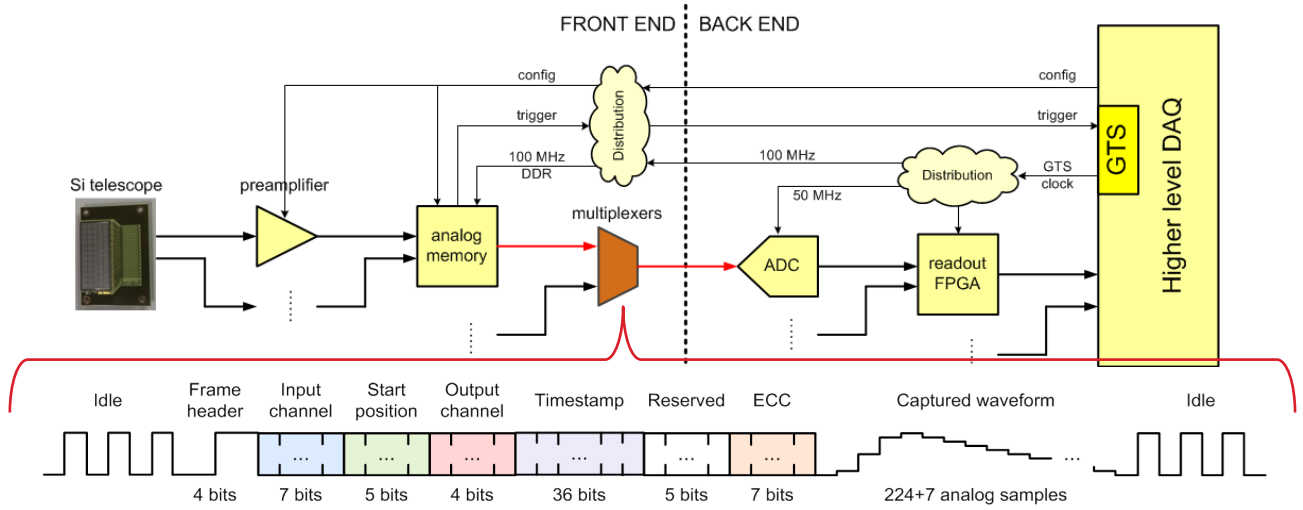
- Input signals
  - Configurable input range and polarity for each channel
  - External resistor R_1
  - Programmable V_{ref} (2 per block of 8 channels)
- Channel trigger
  - Leading edge, programmable threshold (2 per channel)
  - Programmable mode (edge polarity, global trigger, hysteresis…)

Output format



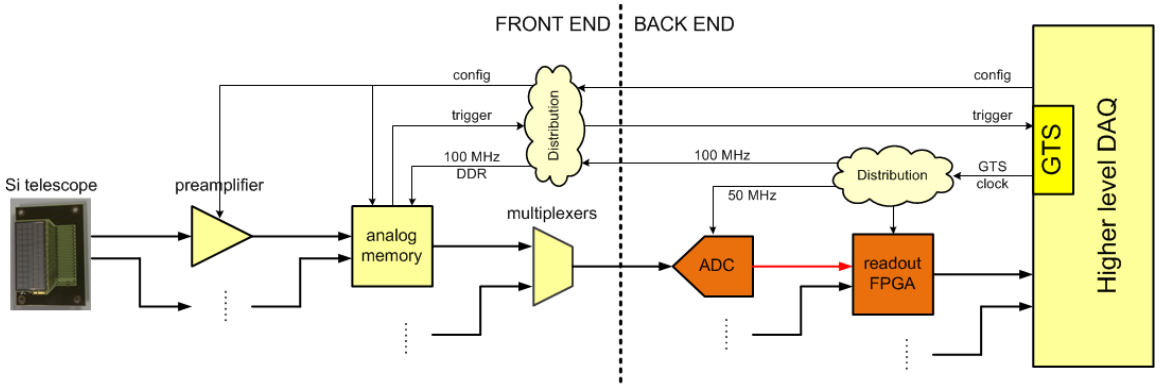
- All data serialized into one differential link at 50 MBaud
- Output frames contain analog and digital data for single pulses
- Frame contents:
  - Training pattern when idle (010101…)
  - Frame header
  - ID of triggering channel
  - Circular buffer position on trigger
  - Tracking info through PLAS
  - Trigger timestamp (Grey encoded)
  - Error correcting code (SECDED)
  - 32(+1) pre-trigger samples
  - 192(+6) post-trigger samples
- Total duration: **5.98 µs** (up to 165 kEvent/s)

Multiplexing PLAS outputs



- Merge output from several PLAS with external multiplexer
- Less physical links, increased latency, event rate reduced (or not)
- Requires external arbitration controller
- PLAS 2.0 will include:
  - Chip ID field in frame (4 bits)
  - Multi-PLAS arbitration support

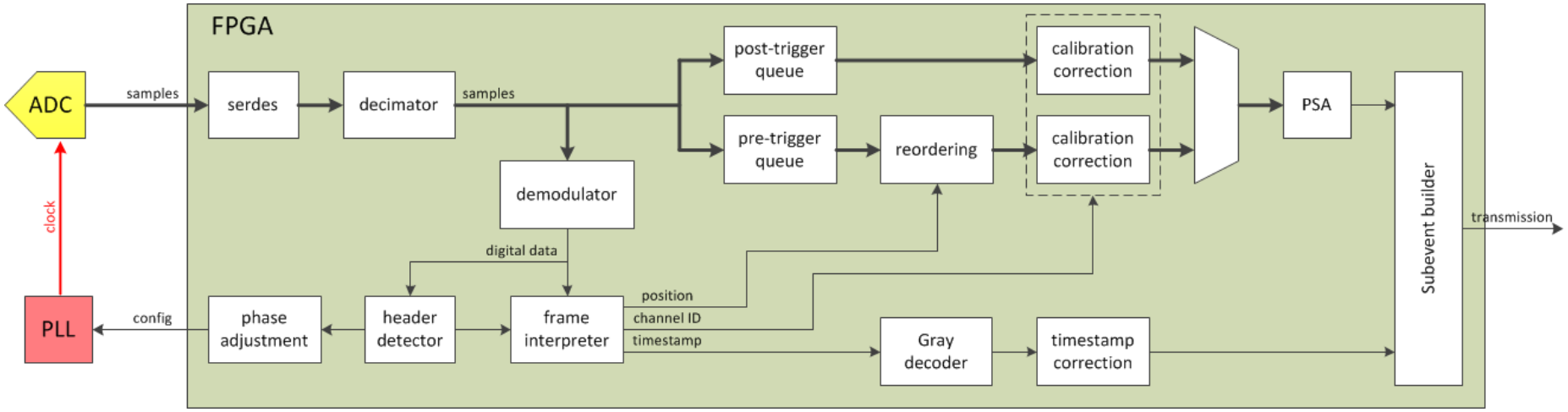
Readout



- Frames are digitized by free running ADC
  (digital: “0”= –1.8V, “1” = +1.8V)
- FPGA mandatory for decoding ADC output
  - Detect start of frame
  - Decode frame contents
  - Adjust sampling phase automatically

- Firmware needs to include:
  - Sampling phase control
  - PLAS frame decoding
  - Sample reordering
  - Calibration correction
  - Timestamp synchronization
  - PLAS configuration
  - TRACE-specific PSA

Processing in FPGA

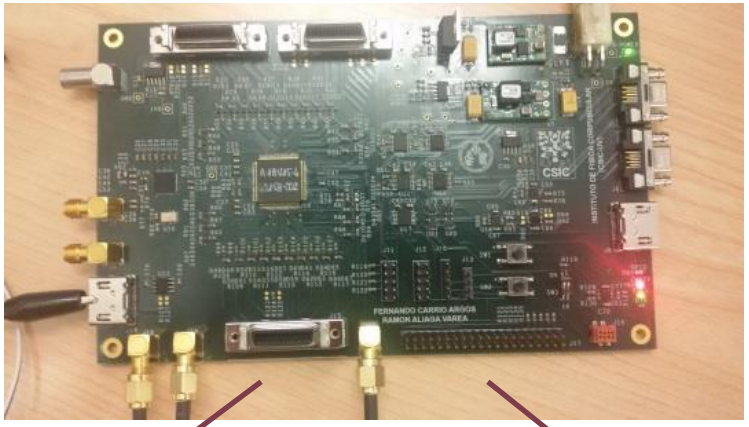


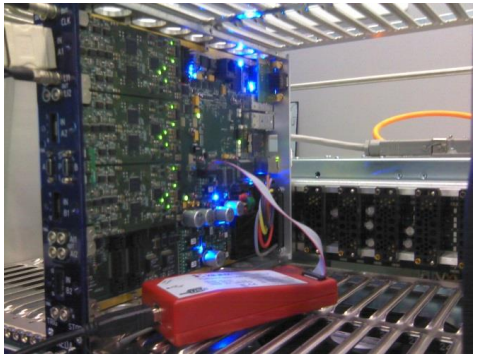
Continuous processing steps:

- Extracting analog and digital data
- Header detection
- Bit error correction
- Recovering data fields in frame
- Reordering samples and removing dummies
- Calibration correction
- Timestamp correction
- Pulse Shape Analysis (TBD)

Current options for readout

PLAS 1.0 test board



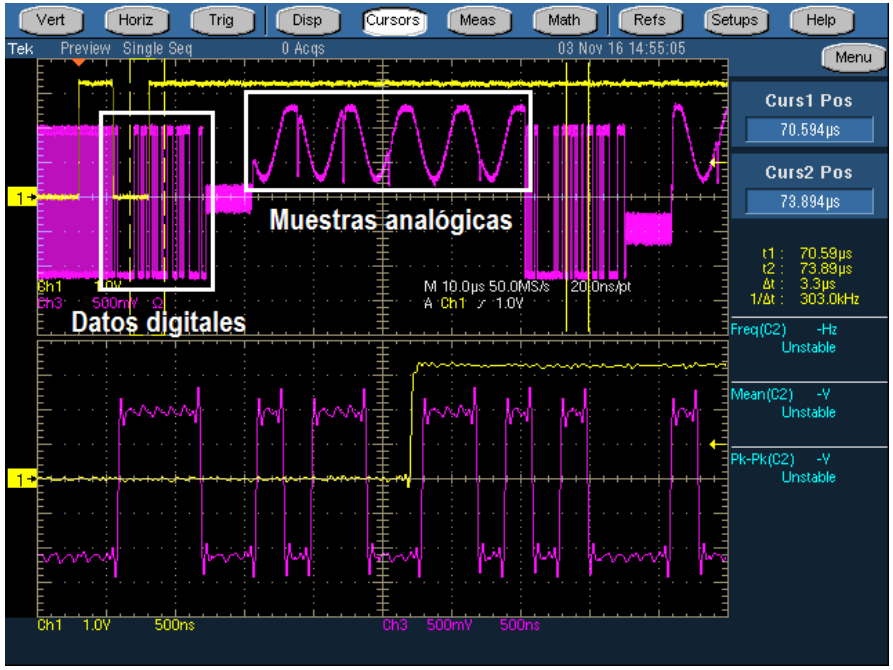


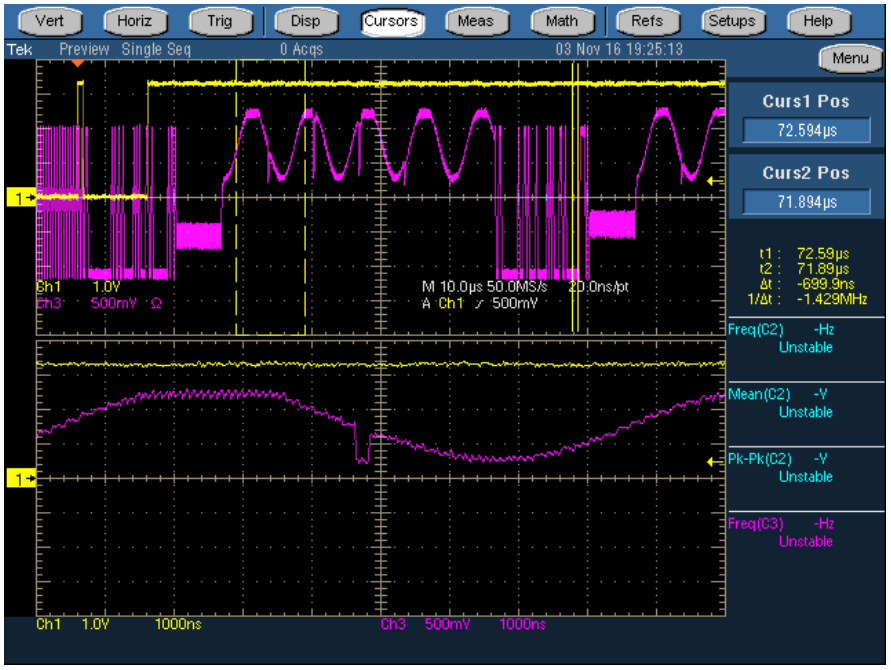
NUMEXO2 + FADC Mezzanine

Custom DAQ from older project

First tests

- Tests with oscilloscope capture, not FPGA

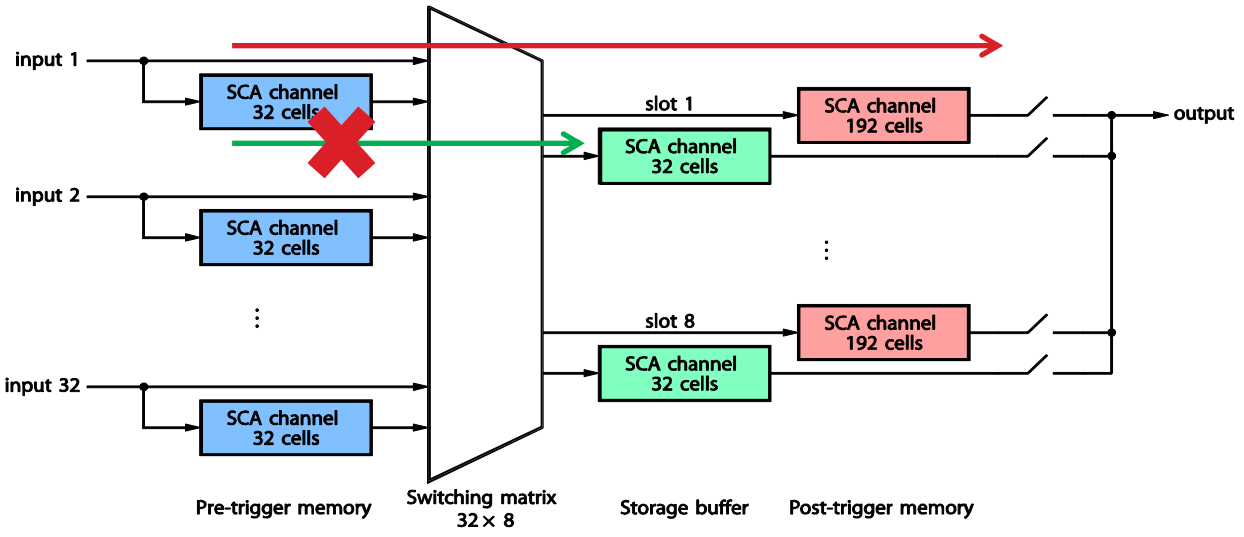




Results of first tests

- Summary: **PLAS 1.0 works partially, redesign mandatory**
- Some event data is lost
  - Pre-trigger samples
  - Triggering channel ID
  - Circular buffer position
- Max frequency below 100 MHz
  - Works properly at 90 MHz
  - Using 80 MHz or 78.125 MHz for tests
- Configuration interface fully operational
- Trigger request signals working
- Around **12 mW/channel** (in test conditions)

Bugs in trigger logic



- (Almost) confirmed in simulations
- Sensitivity to clock skew between 1st and 2nd stage
  - Stage 2 knows there is a trigger
  - Stage 1 does not realize there is a trigger
  - Data is not transferred (channel ID, pretrigger samples…)
- Trigger logic needs redesign

Current plan and status

- PLAS 1.0 test
  - FPGA-based readout
    - NUMEXO2: Having some troubles with setup…
    - Custom DAQ: Ongoing
  - Full PLAS characterization & calibration
  - Completion expected by **15th March** (with custom DAQ)

- PLAS 2.0 redesign
  - Fix/redesign trigger logic
  - Fix operating frequency
  - Clarify specifications
    - Internal vs external shaper
    - Pre-trigger window
    - Other changes depend on test results. **Proposals?**
  - Foundry deadline: **15th May** or **14th August**

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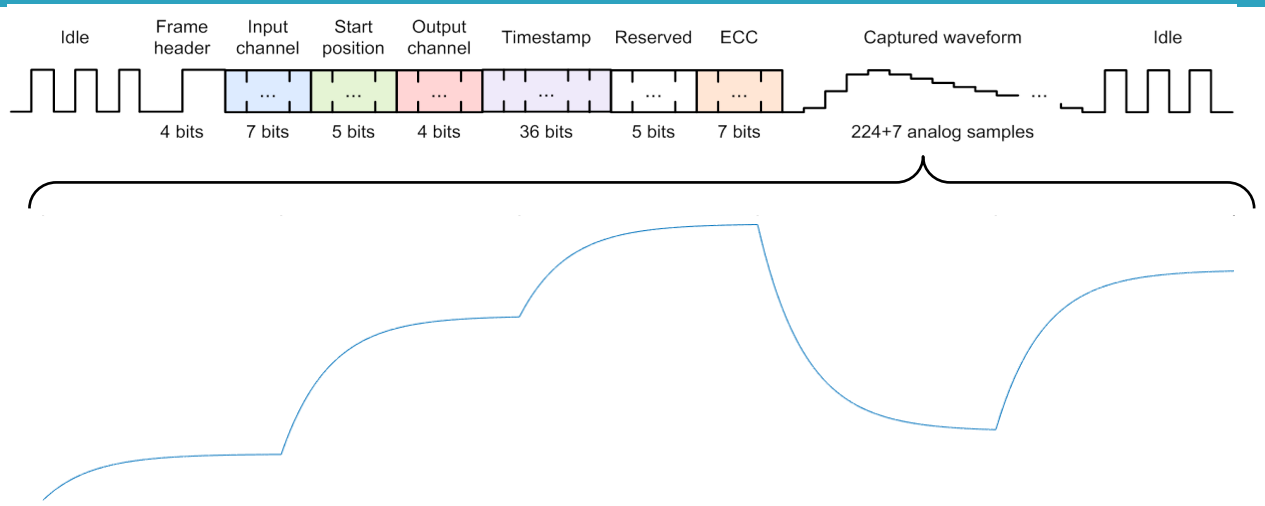
- European Commission FEDER funds

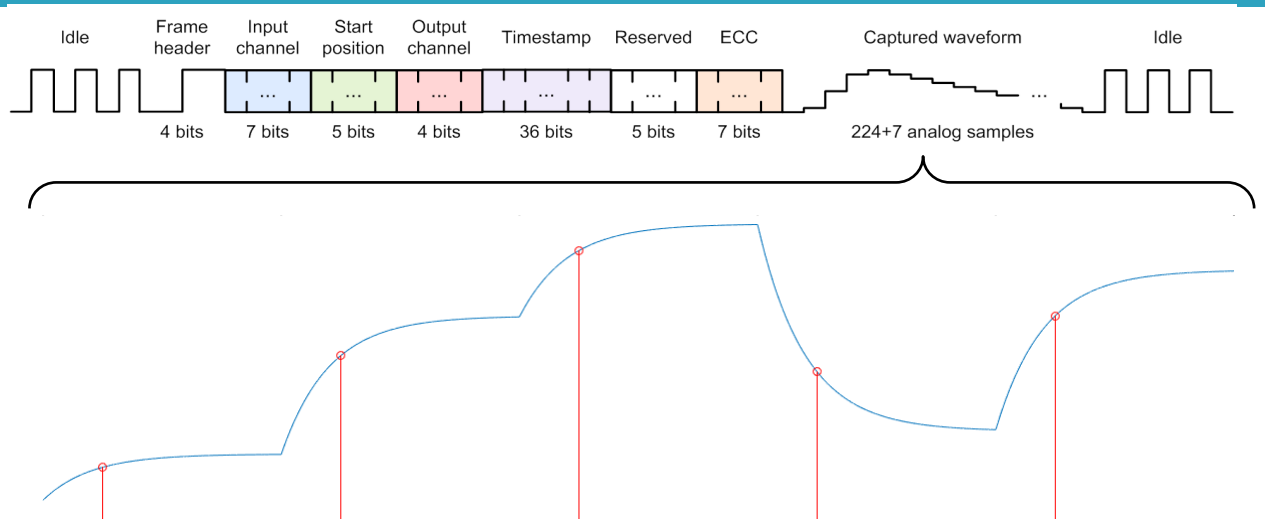
Extra slides

Sampling phase adjustment



- PLAS analog output does not have sharp edges
  - Exponential waveform, **sampling error**
  - Error $\propto \Delta v$, not systematic
  - Error decreases exponentially with sampling phase φ
- **Sampling phase control at the readout digitizer**

Sampling phase adjustment



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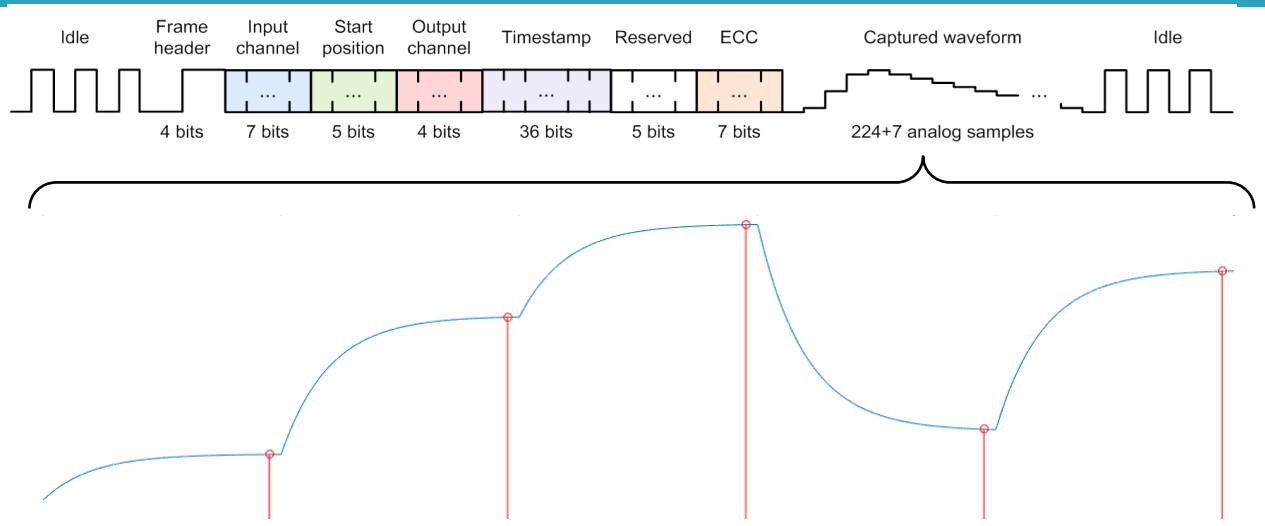

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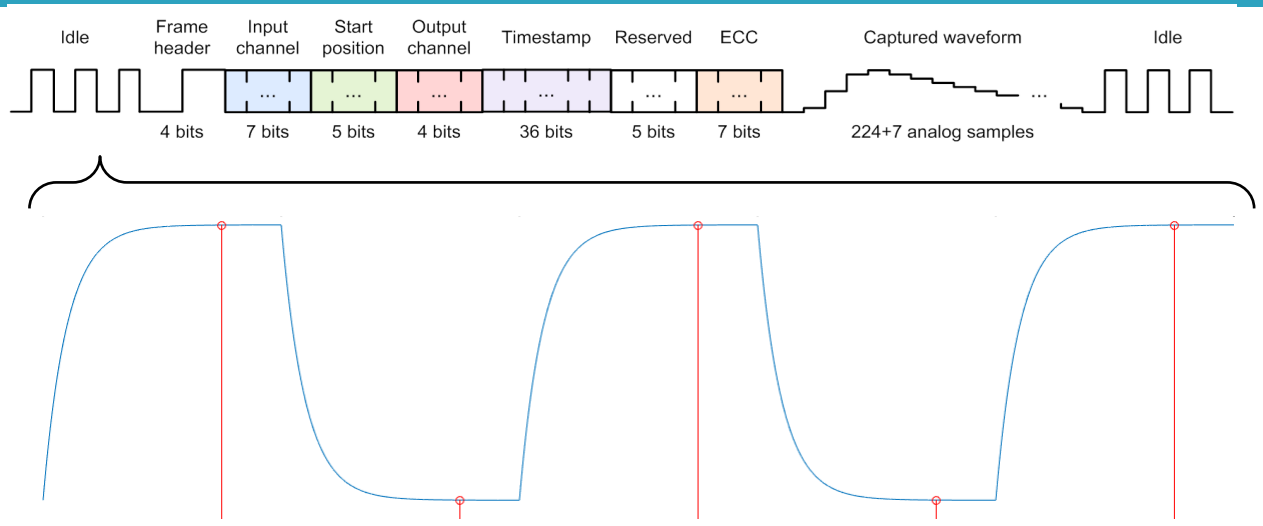
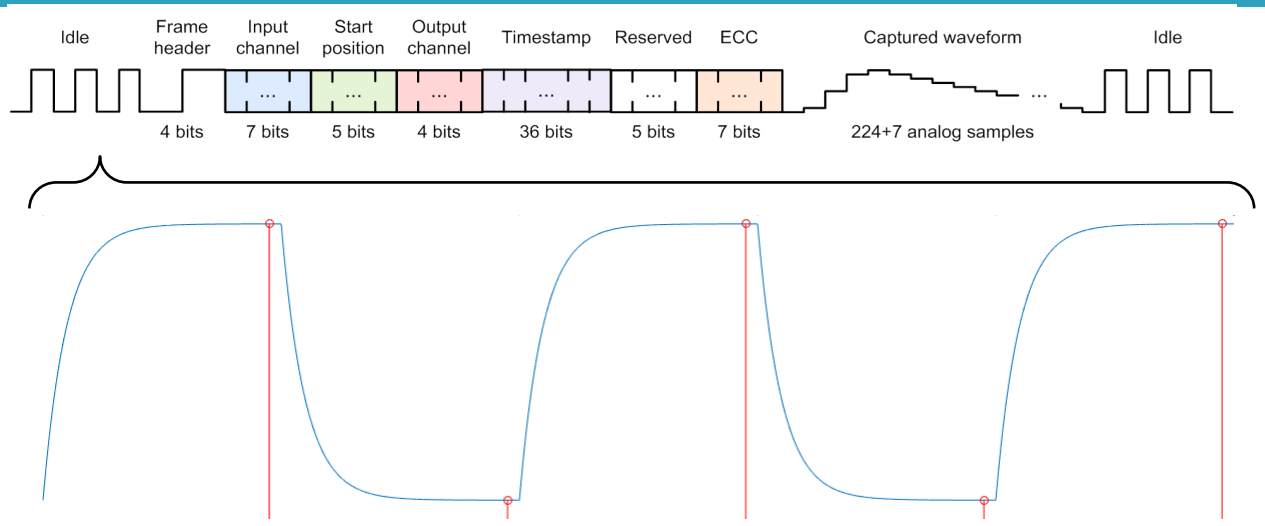


Adjustment method:

- Capture the idle training pattern (010101…)
- Shift φ until bit slip detected
- Set φ at value just before the bit slip
- Shift over the whole period recommended for optimal SNR

Sampling phase adjustment



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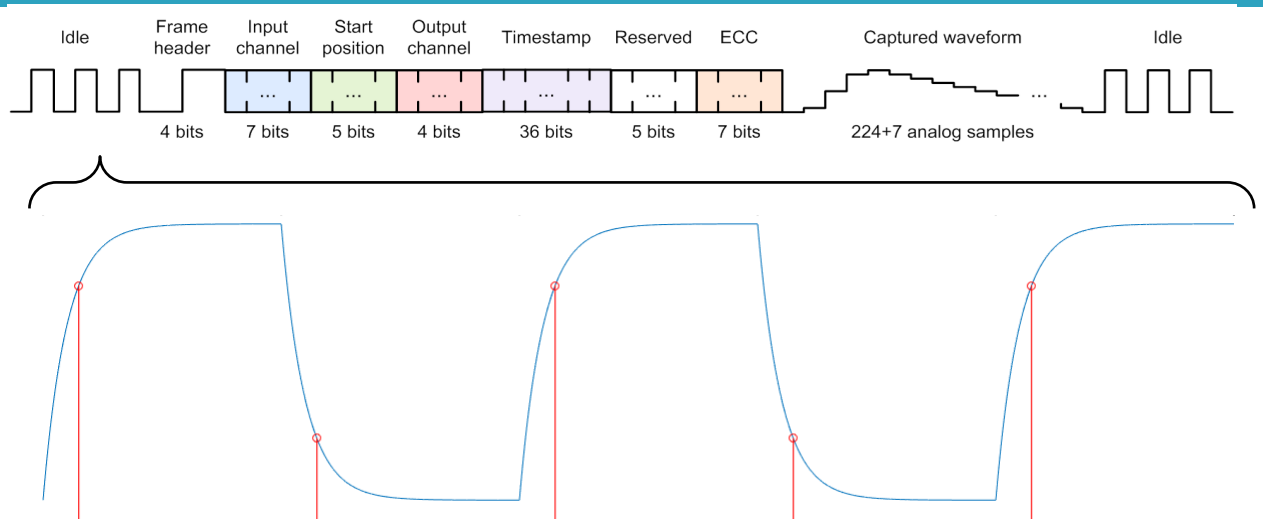

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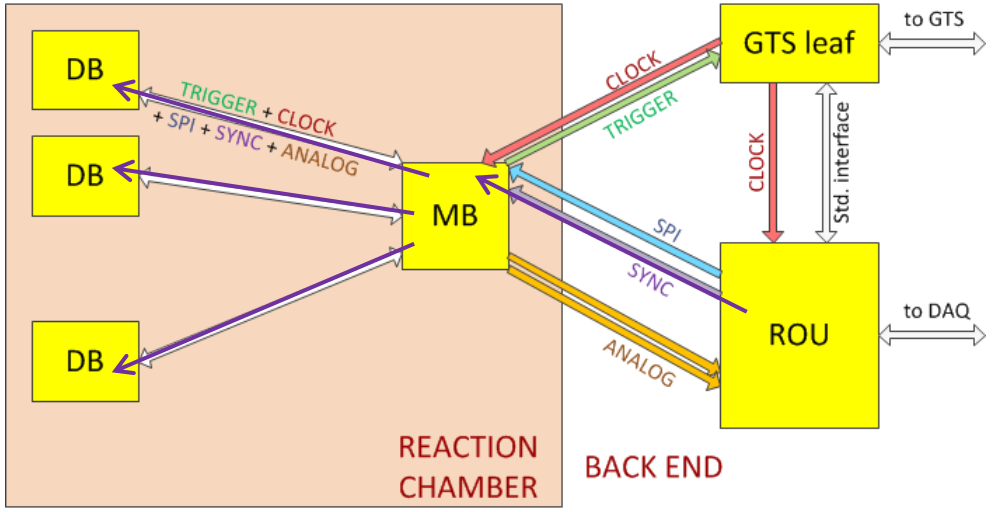
Synchronization scheme

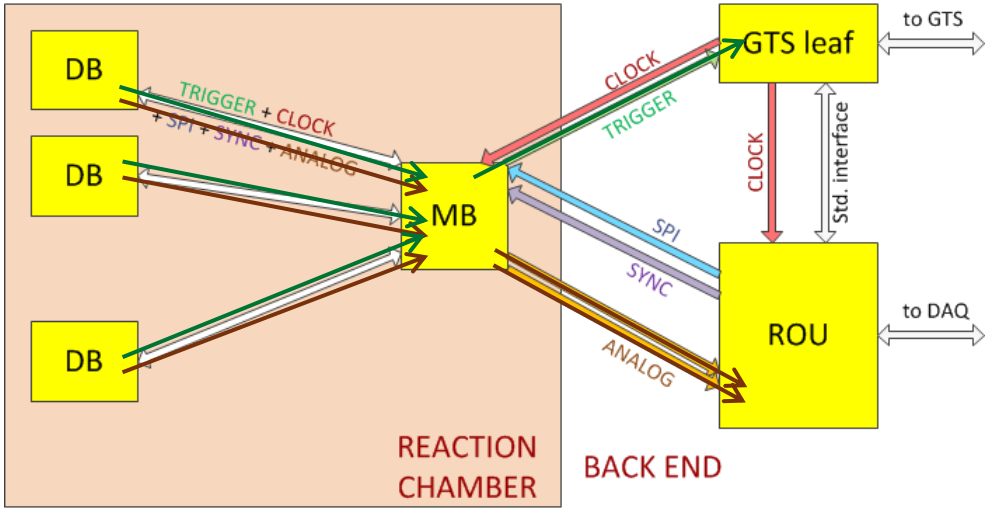


- PLAS timestamp (TS_{PLAS}) ≠ GTS timestamp (TS_{GTS})
- PLAS clock = GTS clock $\Rightarrow$ $TS_{PLAS} - TS_{GTS}$ = constant offset

Alignment method: Compute offset, subtract from TS_{PLAS}

- **SYNC signal** distributed to all PLAS in all DBs at the same time (clock cycle)
- Use **SYNC** as PLAS External Trigger on a dummy channel in each PLAS
- Triggers controlled sync event on all PLAS

Synchronization scheme



- Causes Trigger signal to reach the GTS
  ⇒ **Obtain TS_{GTS}(sync)**
- Places sync event in PLAS queue with TS_{PLAS}(sync)
- Sync frame reaches ROU, identify by channel ID
  ⇒ **Obtain TS_{PLAS}(sync)**
- Compute **offset = TS_{PLAS}(sync) – TS_{GTS}(sync)**
- For all future events, correct TS_{GTS}(event) = TS_{PLAS}(event) – offset