INFN Istituto Nazionale di Fisica Nucleare

CERN European Organization for Nuclear Research

Radiation tolerant electronics for high energy physics experiments

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Outline

- Radiation definition and units
- Radiation effects on CMOS electronics
  - **ASICs**
    - min channel size: 250 nm, 130 nm & 65 nm
    - examples: CARLOS, FeI4, GBTx, RD53
  - **FPGAs**: rad-tol vs COTS
    - antifuse, Flash, SRAM
- Mitigation techniques
- Irradiation test facilities
- Our experience:
    - ALICE SDD
    - CMS Muon Barrel @Louvain la Neuve
    - ALICE TOF @Trento

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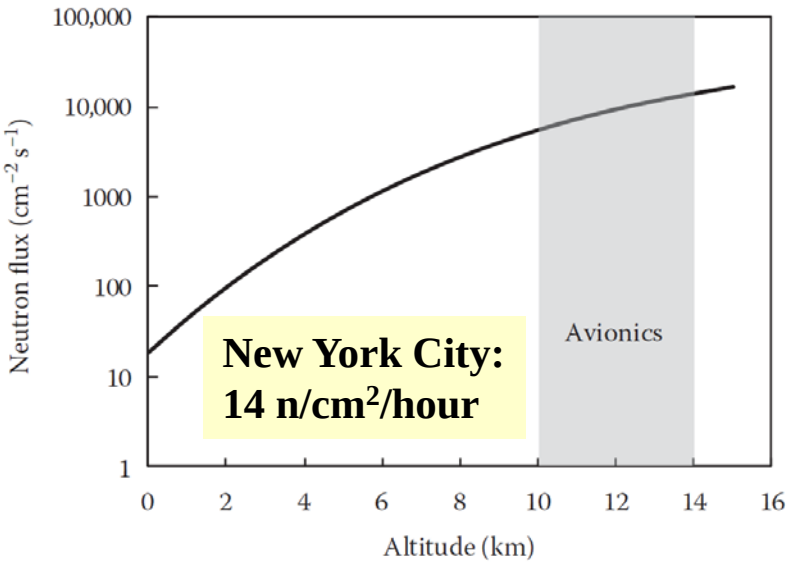
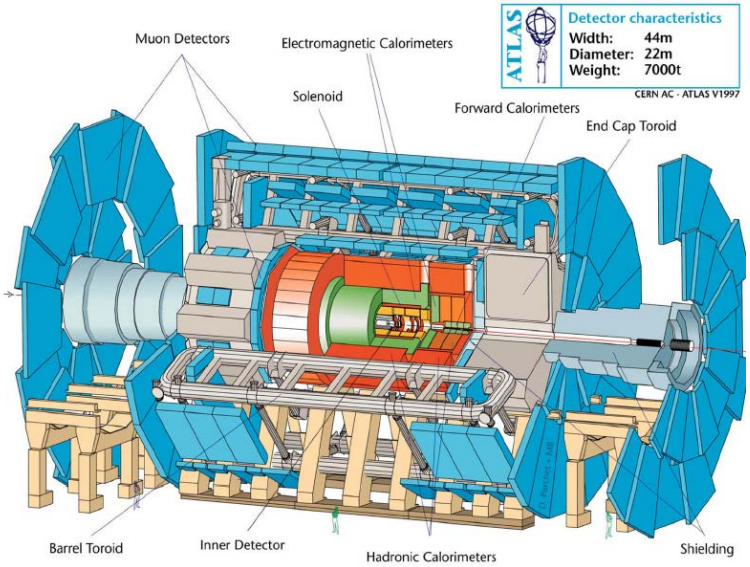
Need for rad-tolerant electronics

- Space applications
- Avionics
- Nuclear power plants instrumentation
- Military application
- High Energy Physics experiments



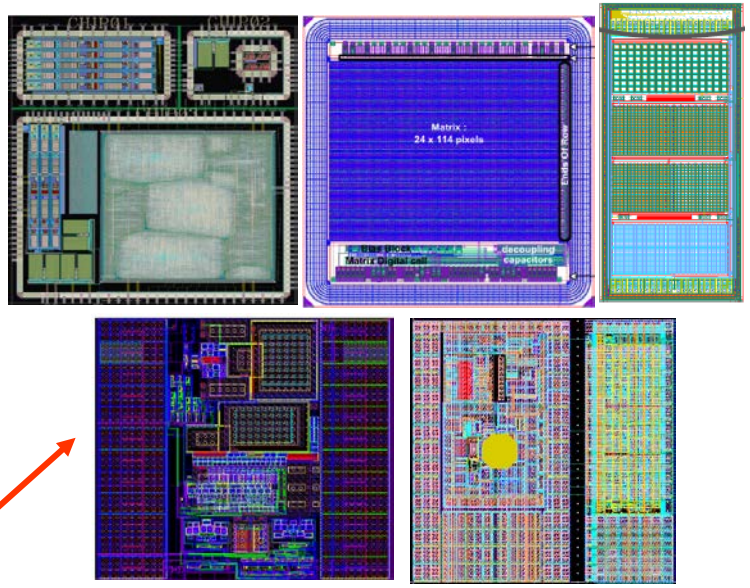
ATLAS Pixels: 2 10^{15} n/cm^2/10 years



Need for rad-tolerant electronics

ESA Sentinel-2

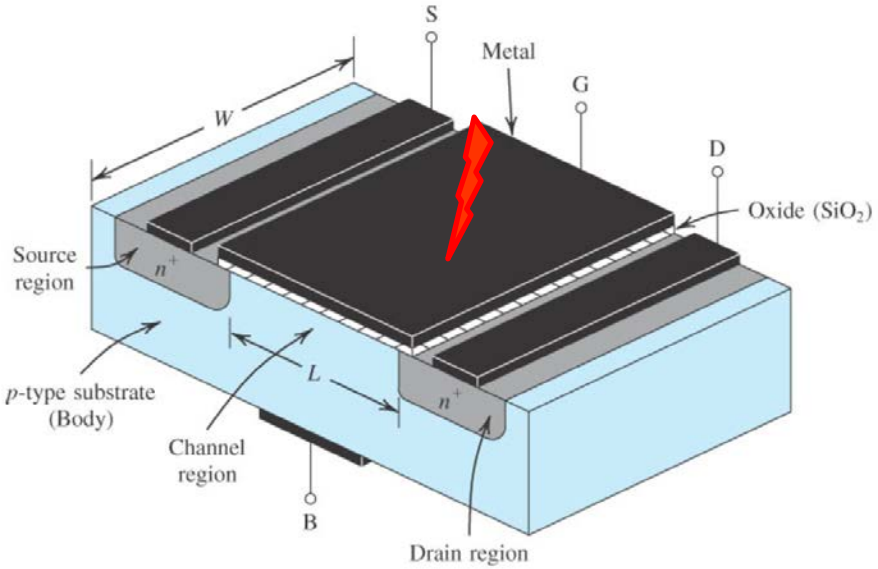
ASICs



IC type	where	quantity
ASIC	P/F	59
ASIC	P/L	0
FPGA	P/F	112
FPGA	P/L	37
uP	P/F	21
uP	P/L	0
Std ASIC	P/F	10
Std ASIC	P/L	0

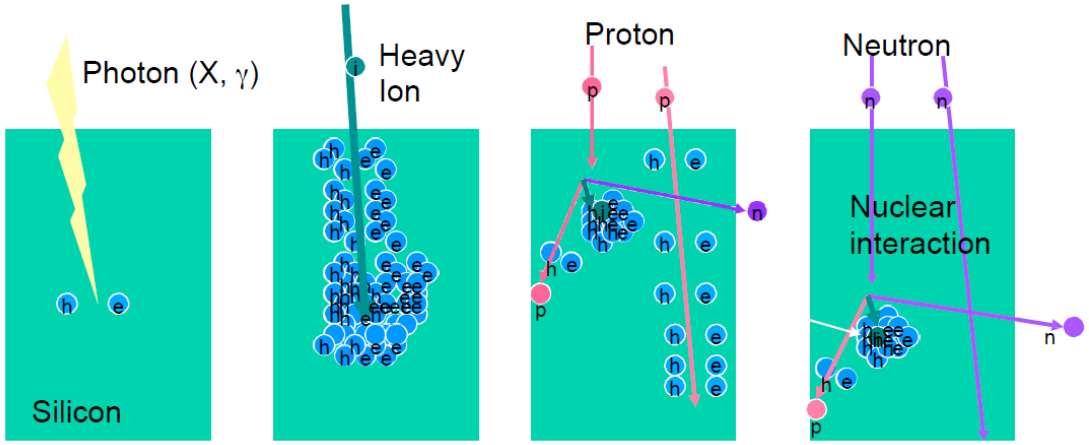
FPGAs

Interaction radiation - Si



radiation @ LHC:

- protons
- neutrons
- pions
- heavy ions
- photons



Radiation effects on electronics

cumulative effects

no dependence on particle type, just on dose

Total **I**onizing **D**ose (**TID**)

ionizing radiation

all components

Displacement **D**amage (**DD**)

non ionizing radiation

bipolar technologies, opto-electronics

single event effects (**SEE**)

depends on type and energy of the radiation

soft

SEU

SET

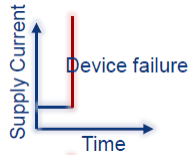
SEFI

digital ICs

hard

SEL

CMOS



SEBO

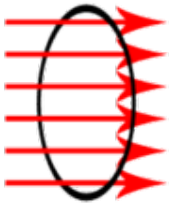
power MOSFET, BJT, diodes

SEGR

power MOSFET

TID + **SEE** are the major concerns in CMOS electronics

Radiation definitions and units



fluence: $\Phi = \frac{dN}{da}$ number of impinging particles per area (cm^{-2})

flux: $\phi = \frac{d\Phi}{dt} = \frac{d^2 N}{dtda}$ fluence rate ($cm^{-2}s^{-1}$)

energy from radiation: $\varepsilon = R_{in} - R_{out} + \Sigma Q$

R_{in}: energy in
R_{out}: energy out
ΣQ: energy changes in V

absorbed dose: $D = \frac{d\bar{\varepsilon}}{dm}$

absorbed energy per volume unit
gray = 1 J/Kg = 100 rad
rad = 100 erg/g

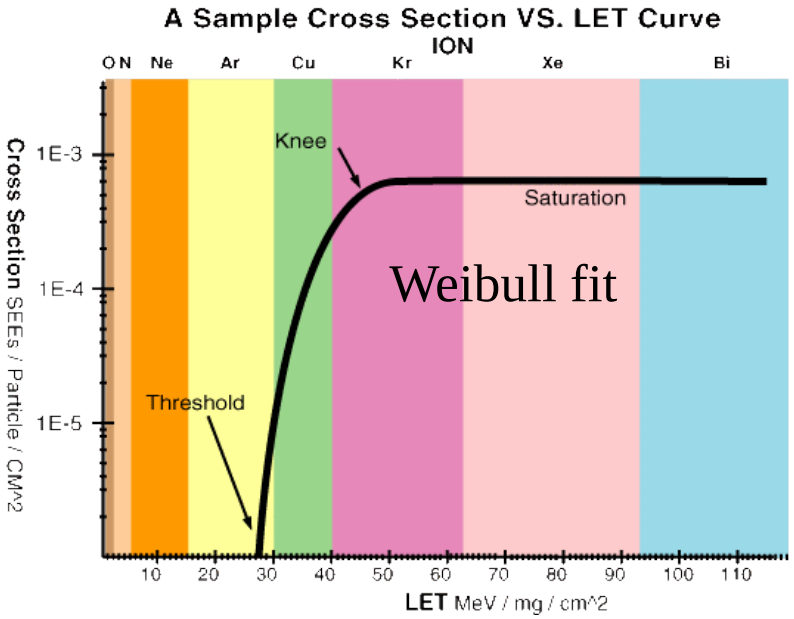
dose rate: $\dot{D} = \frac{dD}{dt}$ gray/s, rad/s

Radiation definitions and units

LET: linear energy transfer ($1/\rho\ dE/dx$)
MeV cm^2 /mg

Ion Species	Energy (MeV)	Range in Si (μm)	Surface LET in Si (MeV×cm^2/mg)
^{1}H	28	4390	0.02
^{7}Li	56	378	0.37
^{11}B	80	195	1.01
^{12}C	94	171	1.49
^{16}O	108	109	2.85
^{19}F	122	99.3	3.67
^{28}Si	157	61.5	8.59
^{32}S	171	54.4	10.1
^{35}Cl	171	49.1	12.5
^{48}Ti	196	39.3	19.8
^{51}V	196	37.1	21.4
^{58}Ni	220	33.7	28.4
^{63}Cu	220	33.0	30.5
^{74}Ge	231	31.8	35.1
^{79}Br	241	31.3	38.6
^{107}Ag	266	27.6	54.7
^{127}I	276	27.9	61.8
^{197}Au	275	23.4	81.7

ρ_{Si}=2330 mg/cm^3



cross-section (σ): the probability that the particle produces a SEE, given in cm^2/bit, or cm^2/device

$$\sigma = N_{SEU} / \Phi$$

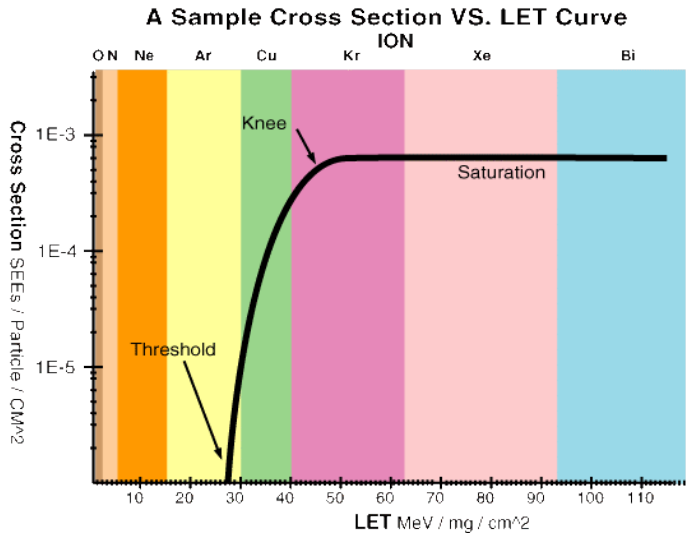
Failure In Time rate (in 1 billion hours):

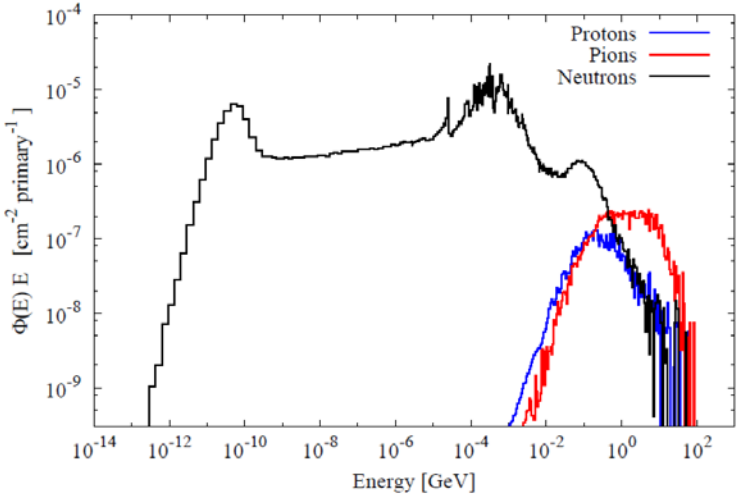
FIT/Mbit = $\sigma * \phi * 10^6 * 10^9$

Mean Time Between Failures:

MTBF = $1/(bits * \sigma * \phi)$

SEU rate (R) estimate





$$\mathbf{N_{SEU}} \quad R = \int_{E0}^{\infty} \sigma(E) \frac{d\phi}{dE} dE$$

$$\mathbf{R = N_{device}\ \sigma\ \Phi}$$ **SEU rate**

Huhtinen and Faccio, "*Computational methods to estimate Single Event Upset rates in an accelerator environment*"

This work shows that **an irradiation with protons directly gives an estimate of the SEU rate in LHC: the measured σ at an energy of about 60MeV or more, multiplied by the total hadron ϕ (above 20MeV) foreseen in the position of interest in LHC, gives the expected upset rate.**

Particles and damages

Dose (rad(Si)) = LET *Fluence*1.610^{-5}

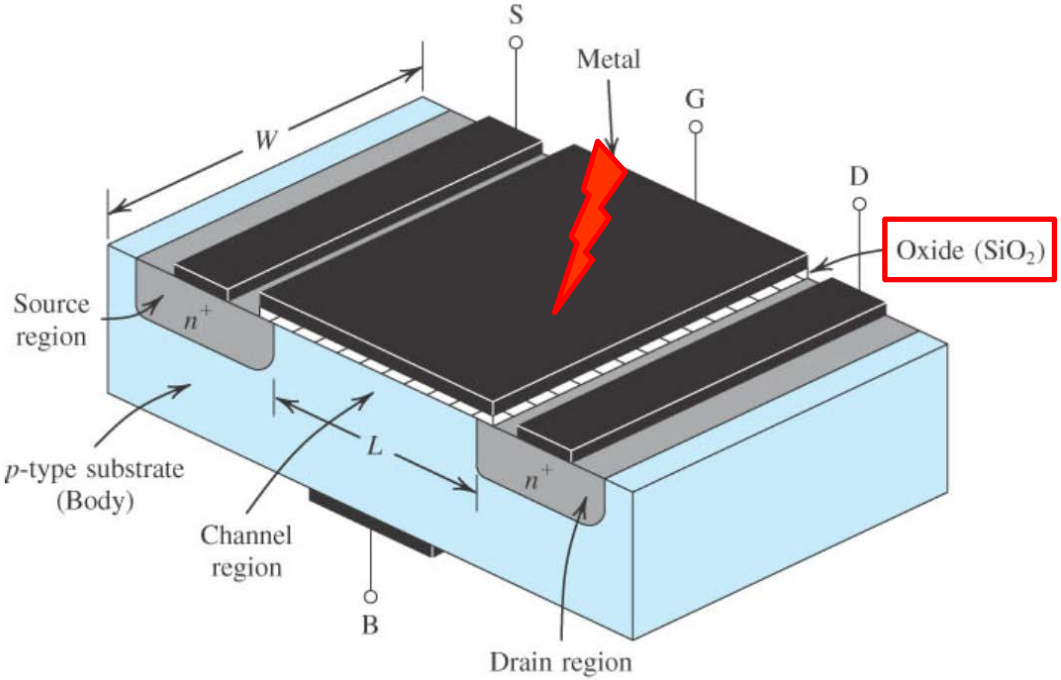
Radiation	TID	Displacement (NIEL)	SEE
X-rays ^{60}Co γ	Expressed in SiO_2 Almost identical in Si or SiO_2	No	No
p	Equivalences in Si[$] @60MeV 10^{11}p/cm^2=13.8krd @100MeV 10^{11}p/cm^2=9.4krd @150MeV 10^{11}p/cm^2=7.0krd @200MeV 10^{11}p/cm^2=5.8krd @250MeV 10^{11}p/cm^2=5.1krd @300MeV 10^{11}p/cm^2=4.6krd @23GeV 10^{11}p/cm^2=3.2krd	Equivalences in Si[$,*] @53MeV 1 p/cm^2 = 1.25 n/cm^2 @98MeV 1 p/cm^2 = 0.92 n/cm^2 @154MeV 1 p/cm^2 = 0.74 n/cm^2 @197MeV 1 p/cm^2 = 0.66 n/cm^2 @244MeV 1 p/cm^2 = 0.63 n/cm^2 @294MeV 1 p/cm^2 = 0.61 n/cm^2 @23GeV 1 p/cm^2 = 0.50 n/cm^2	Only via nuclear interaction. Max LET of recoil in Silicon = 15MeVcm^{2}mg^{-1}
n	Negligible	Equivalences in Si[$,*] @1MeV 1 n/cm^2 = 0.81 n/cm^2 @2MeV 1 n/cm^2 = 0.74 n/cm^2 @14MeV 1 n/cm^2 = 1.50 n/cm^2	As for protons, actually above 20MeV p and n can roughly be considered to have the same effect for SEEs
Heavy Ions	Negligible for practical purposes (example: 10^6 HI with LET=50MeVcm^{2}mg^{-1} deposit about 800 rd)	Negligible	Yes

[$] Energy here is only kinetic (for total particle energy, add the rest energy mc^2)

[*]The equivalence is referred to "equivalent 1Mev neutrons", where the NIEL of "1MeV neutrons" is DEFINED to be 95 MeVmb. This explains why for 1MeV neutrons the equivalence is different than 1

SEU rates in LHC is dominated by hadrons with E > 20 MeV

Radiation effects on CMOS electronics

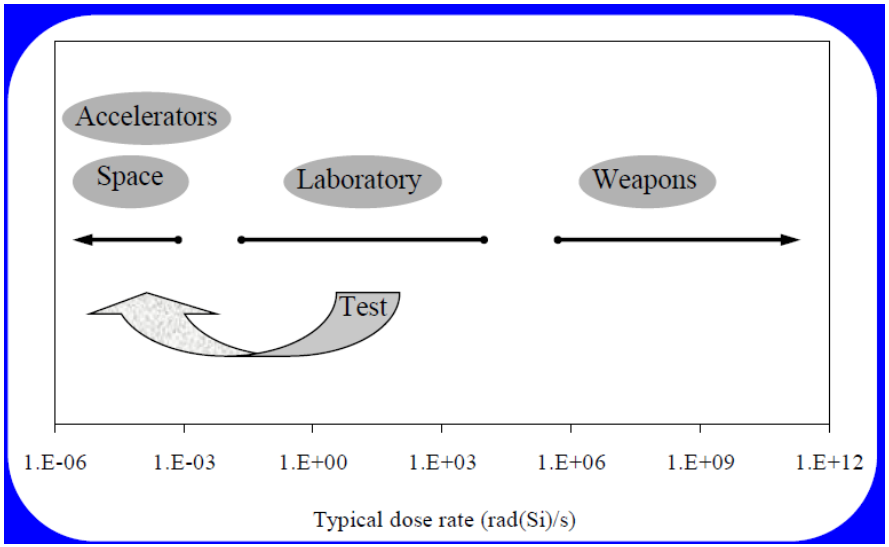


Radiation effects depend on:

- type of radiation
- W/L geometry
- temperature

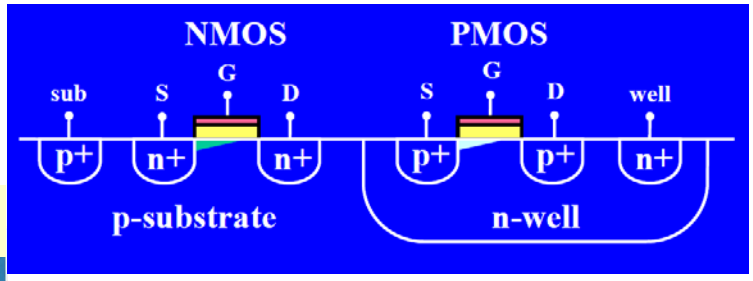
They do **NOT** depend on:

- dose rate



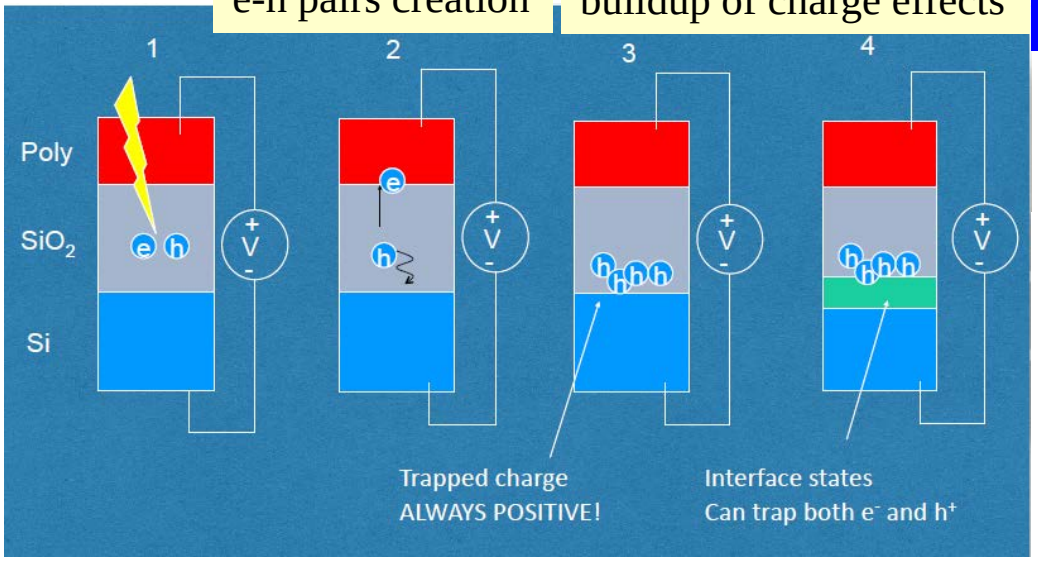
This allows to test at high dose rates systems that will have to face low dose rates!

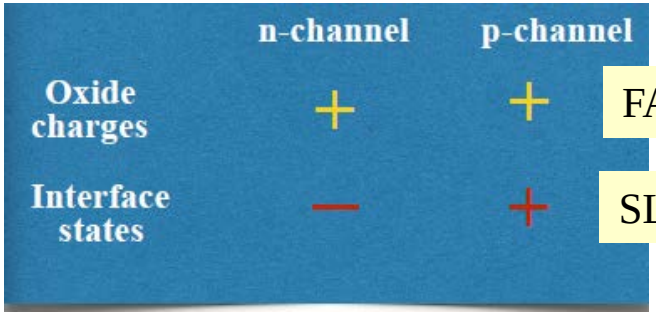
TID



e-h pairs creation

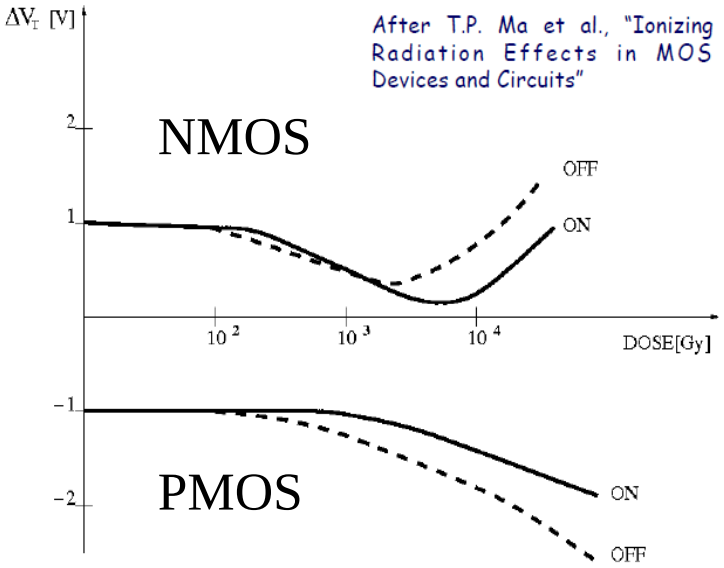
buildup of charge effects





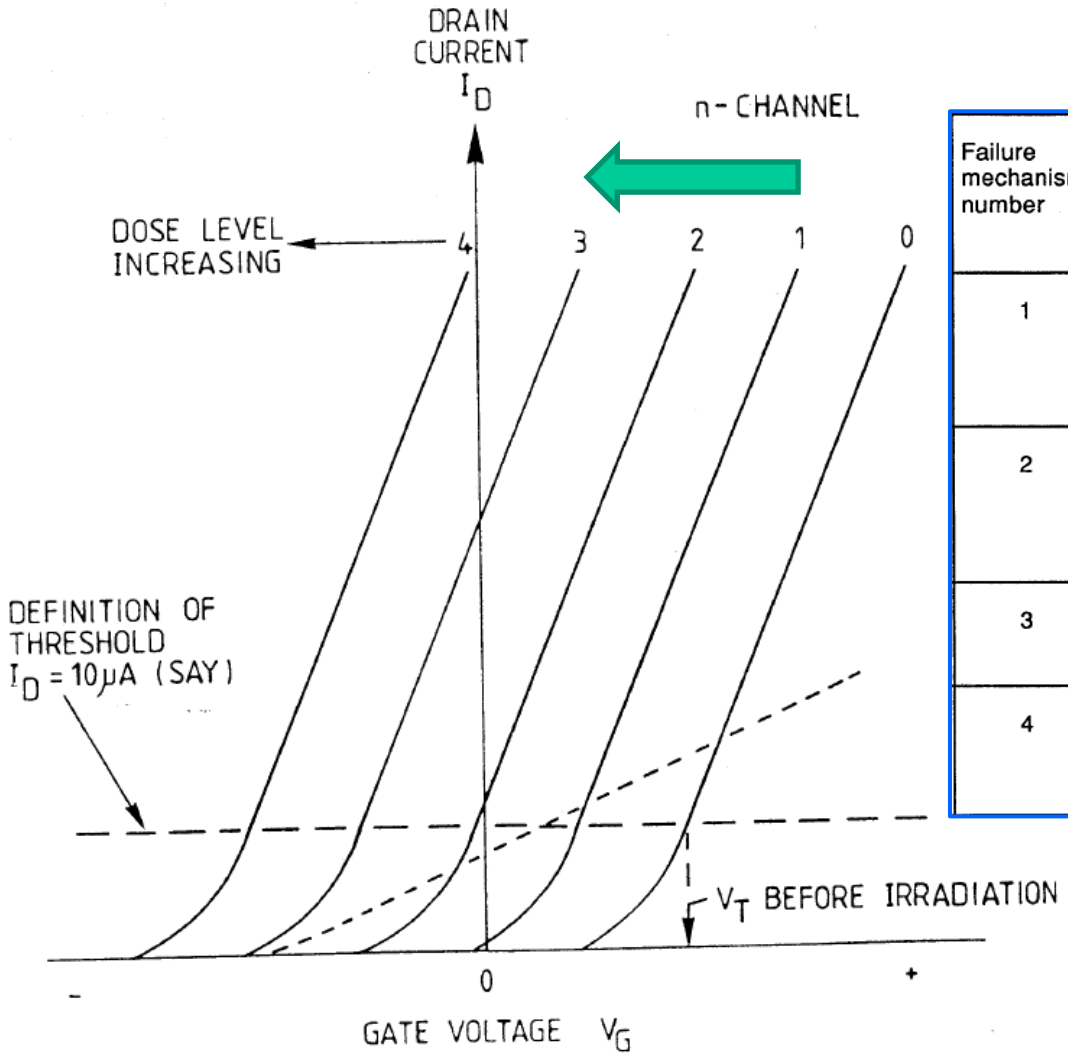
FAST process

SLOW process



TID ➔ how much the device parameters drift ?
(device degradation)

TID effects



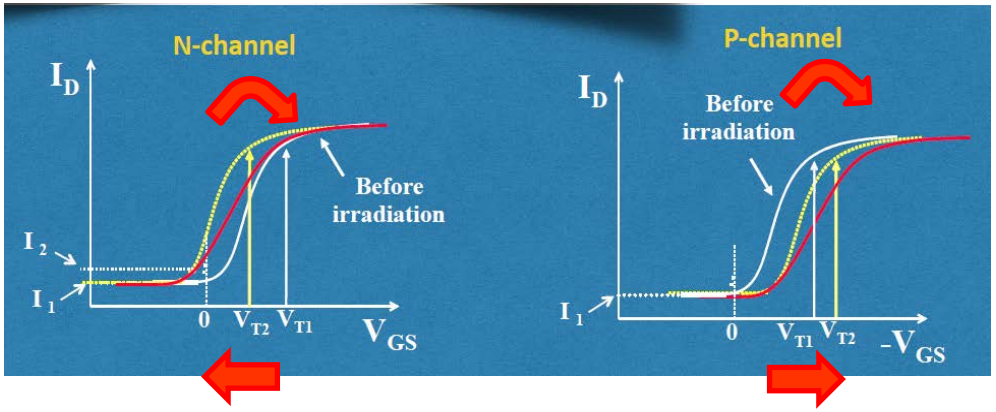
Failure mechanism number	Main degradation effect	Symbol	Typical values for CMOS LSI	
			Dose rad (Si)	$-\Delta V_T$ volts
1	Minor 'noise immunity reduction'; possibly minor loss in switching speed	NIR	8×10^2	0.2
2	Sharp quiescent current increase due to 'V_T of N-channel crossing zero	VTNZ	5×10^3	1
3	Switching speed reduction	SSR	1×10^4	2
4	Change of logic state impossible: 'Logic failure'	LF	3×10^4	4

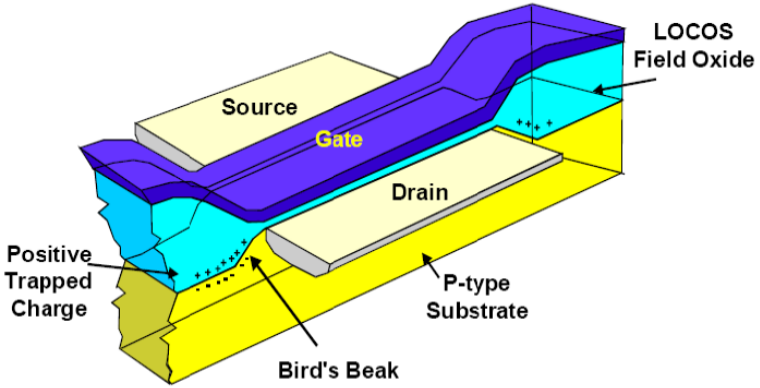
from ESA PSS-01-609 Issue 1 (May 1993)

TID effects

leakage current increase

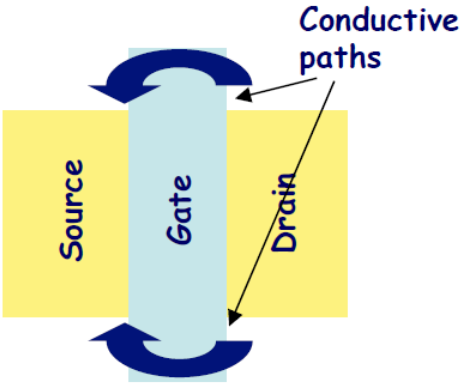
threshold voltage shift $\Delta V_T = -\frac{Q_{OX}}{C_{OX}} \propto t_{ox}^2$





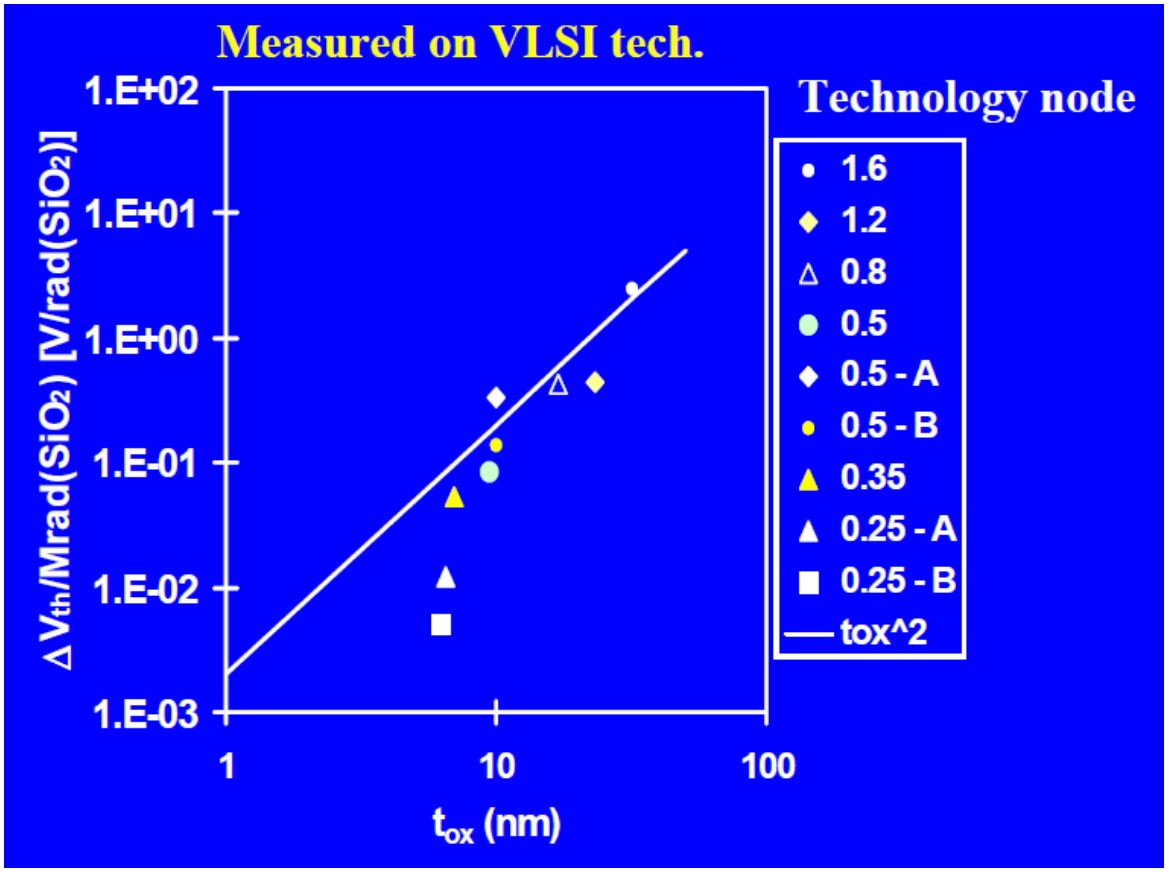
transconductance ⇩⇩

the MOS gets slower



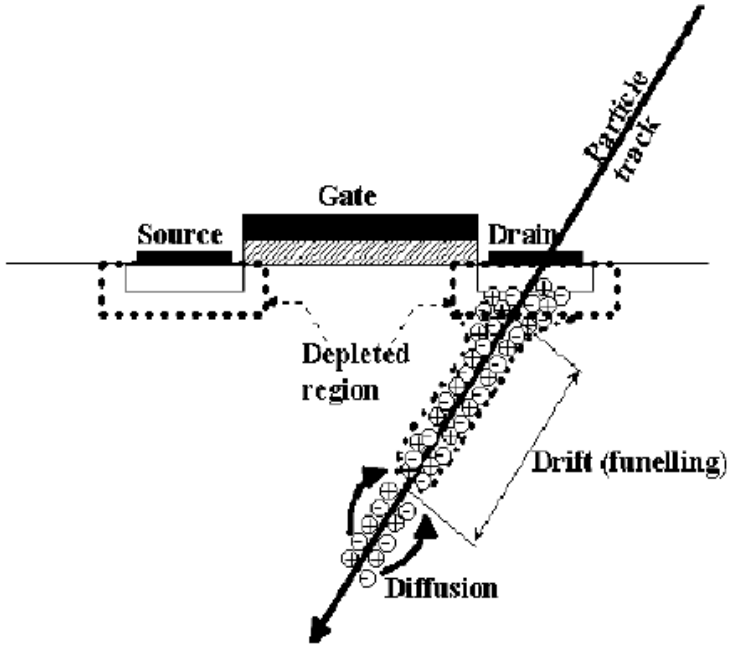
TID effects

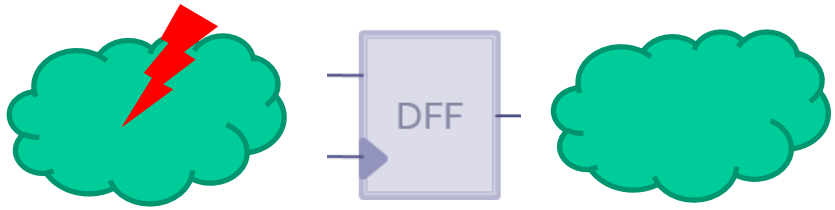
$$\Delta V_T = -\frac{Q_{OX}}{C_{OX}} \propto t_{ox}^2$$

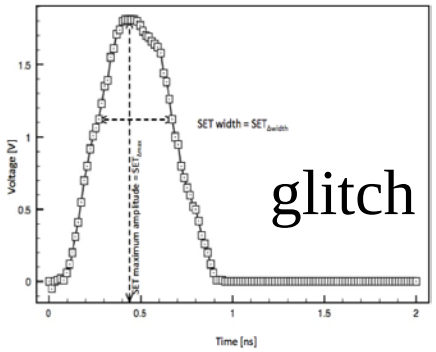


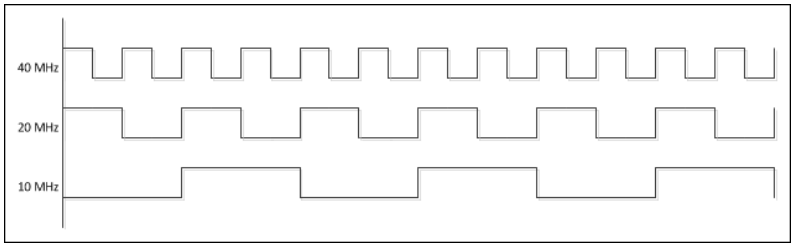
Good news: Shrinking the technology, the oxide thickness is reduced and also the threshold voltage variation

Soft SEU effects

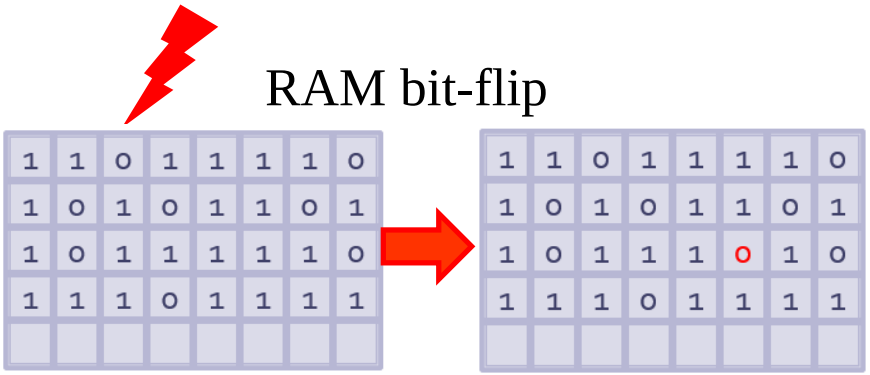






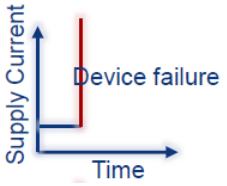


RAM bit-flip



SET: the higher the clock frequency, the higher the probability of an error being propagated

Hard SEU effects



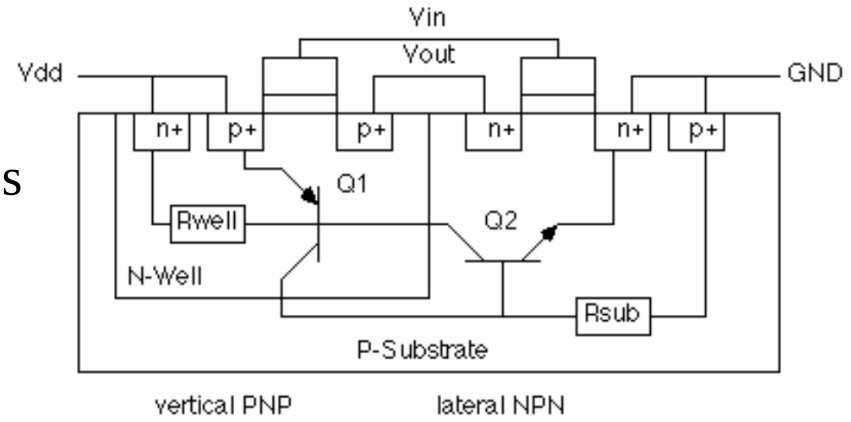
Electrical latchup can be fired by:

- electrical transients on I/O lines,
- high T
- bad sequencing of power bias

Latchup can be fired by ionizing particles

⇩

SEL



What to do with SEL:

SEL needs to be faced by monitoring the supplied current and shutting off power and I/Os when a current bump is found

Mitigating TID & SEE effects: radiation hardening

Hardening:

by layout:

modifying the device geometrical layout

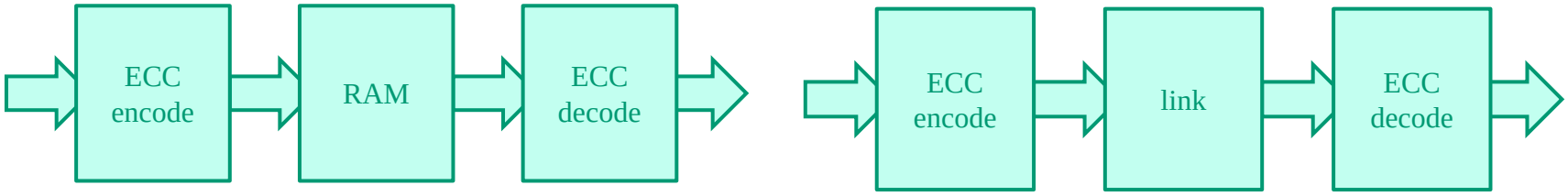
by process:

modifying one or more steps of the fabrication process

by design:

improve the design to be rad-tolerant

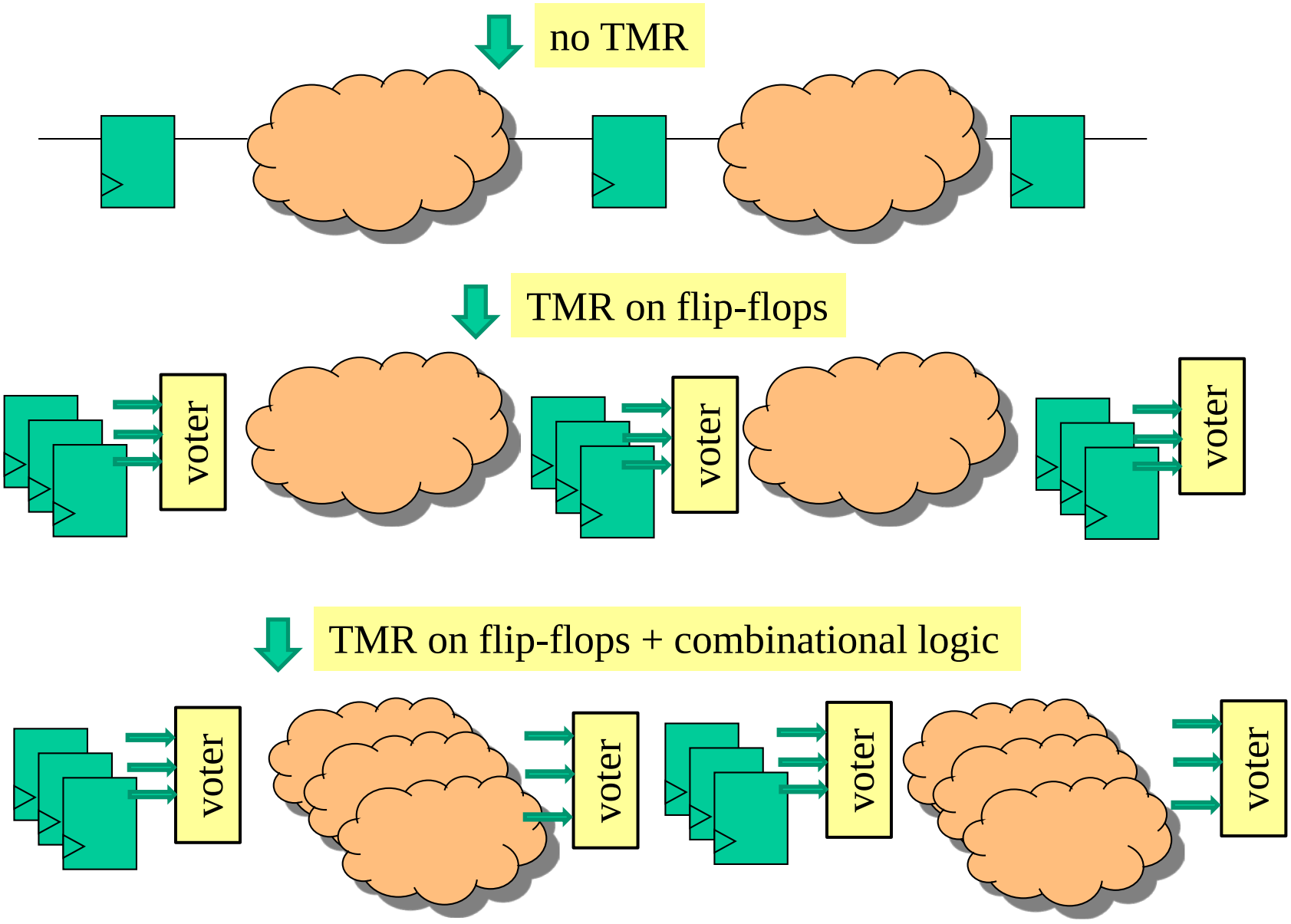
EDAC : Error Detection And Correction



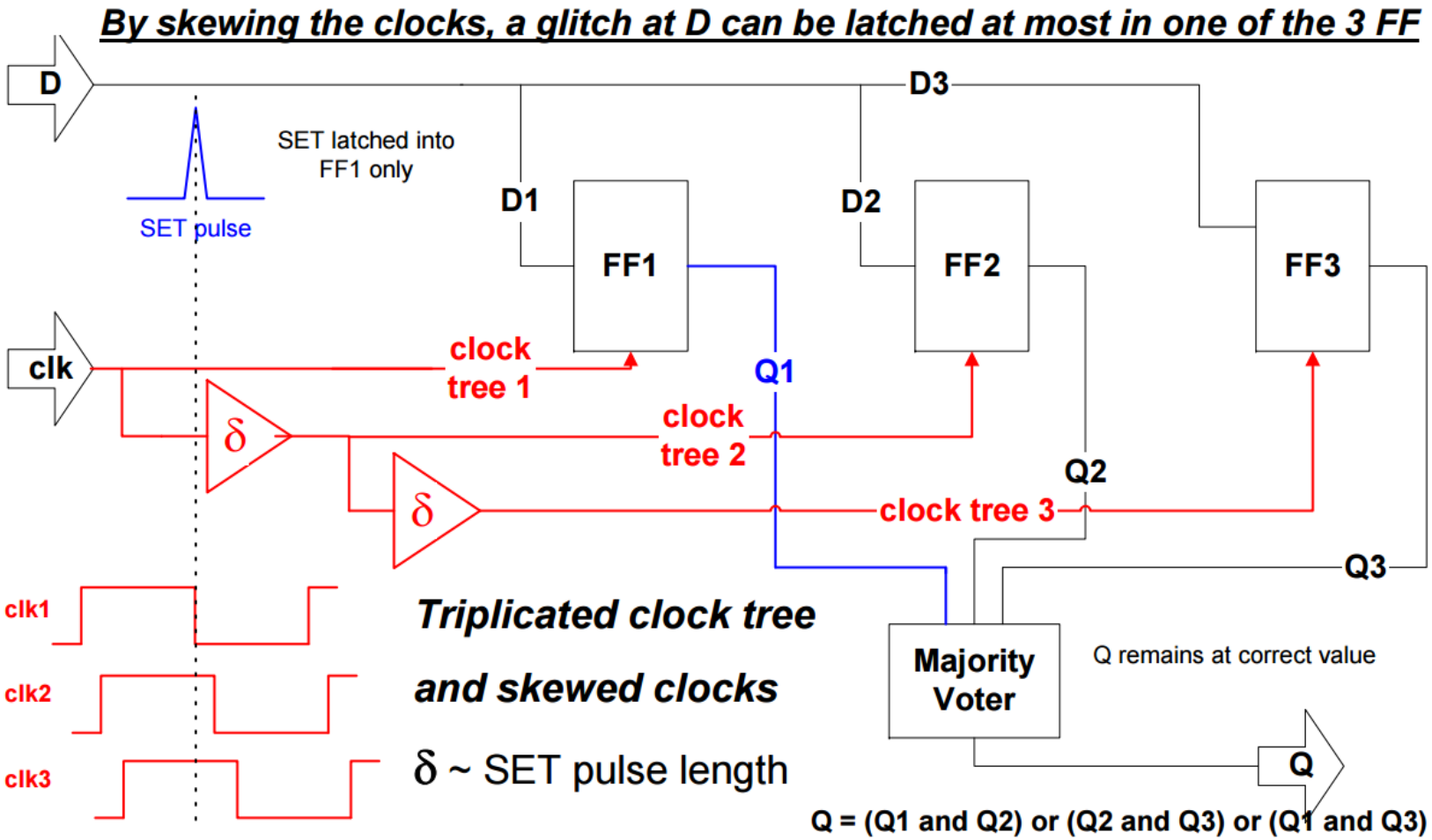
An error-correcting code (**ECC**) or forward error correction (**FEC**) code is a process of adding redundant data, or *parity data*, to a message, such that it can be recovered by a receiver even when a number of errors (up to the capability of the code being used) are introduced

hardening ➔ risk reduction comes at some cost!

Triple Modular Redundancy



SET mitigation with skewed clocks



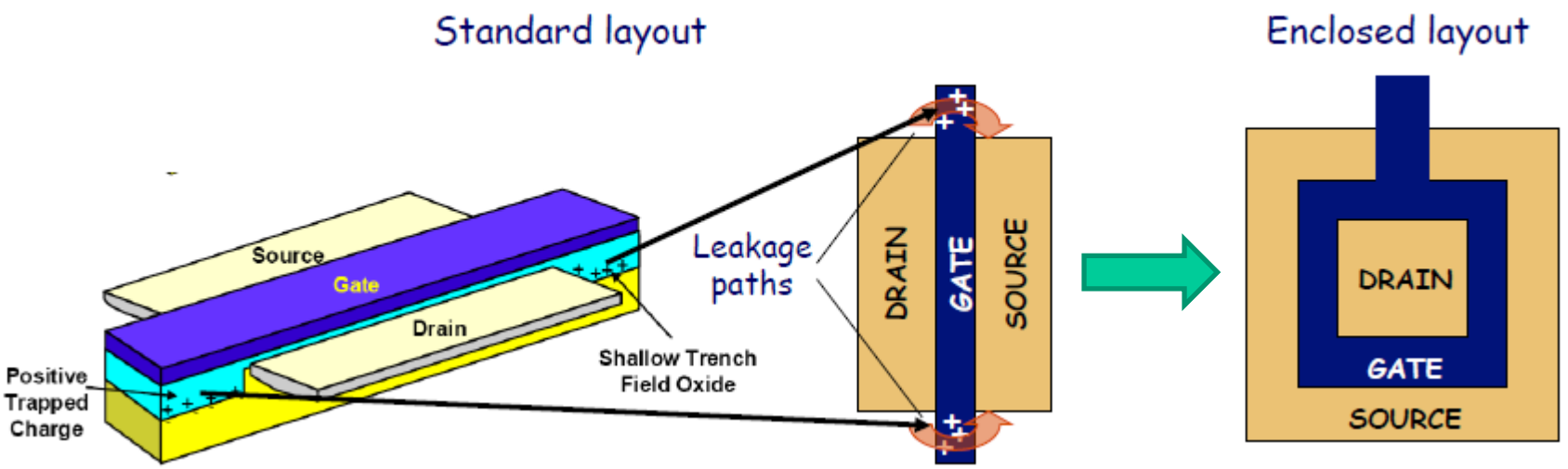
Beware!!

- **TMR voting and clock skewing reduce maximum spee**
- **increased area leads to higher interconnect delay**

250 nm CMOS technology node (t_{ox} = 5 nm)

TID has been addressed by redesigning the digital library of standard cells with Enclosed Layout Transistors (ELTs)

linear transistor EL Transistor

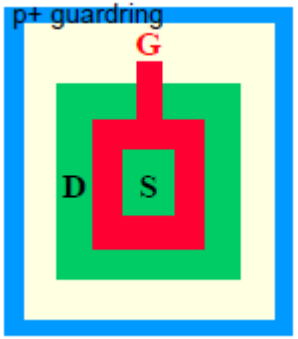


net positive charge trapped into the Si-SiO_2 interface

→ no TID effect up to 140 Mrad (Si-SiO_2 interface removed by design)

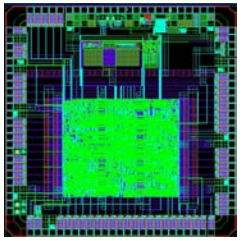
SEU

redundant logic, like TMR, Hamming codes …

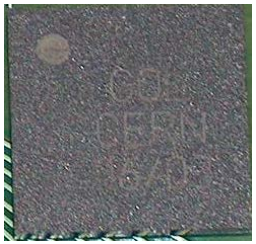


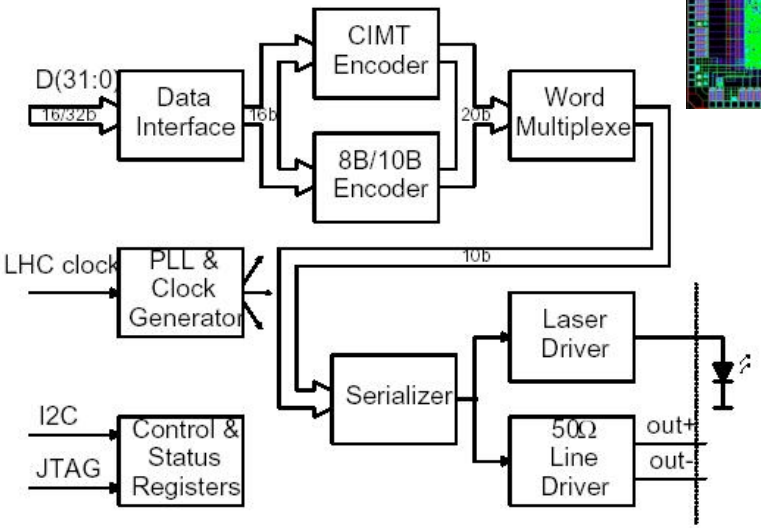
hardening by layout

250 nm CMOS chips



GOL

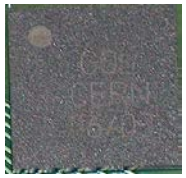




rad requirements:

- **TID**: 10 to 100 Mrads
- **Φ**: 10^{15} to 10^{16} p/cm^2

p @ 230 MeV



mitigation techniques adopted:

- use of ELT modified standard cells against **TID**
- hardwired config data
- Hamming protected config
- 8B/10B encoding/decoding

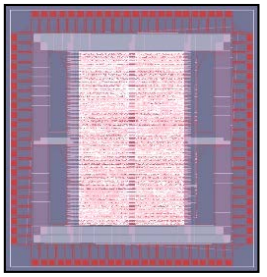
TID No effects up to 100 Mrad (Si) = 1.9 10^{13} p/cm^2

SEU No SEE up to 10^{11} p/cm^2

200 LoL events ➔ $\sigma = 2.5\ 10^{-13}$ cm^2

20 bit corruption events ➔ $\sigma = 5.3\ 10^{-14}$ cm^2

CARLOS: 250 nm ASIC



ALICE SDD compression chip:

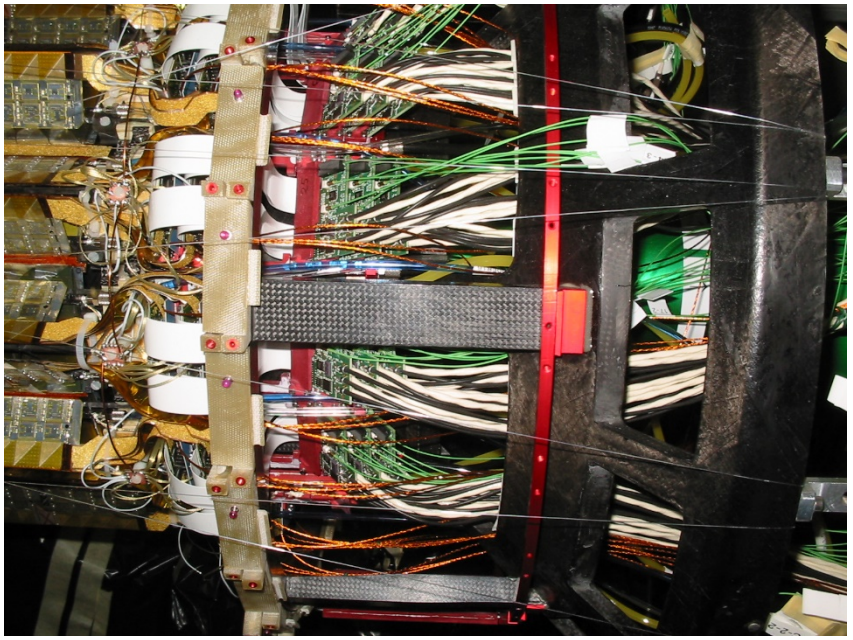
- 15 kgates
- 4 256-word RAMs
- die area: 4x4 mm^2

radiation environment:

- **TID:** 14 krad
- Φ = 3.5 10^{11} n/cm^2 in 10 years

mitigation techniques adopted:

- use of ELT modified standard cells against **TID**
- no redundancy against SEUs

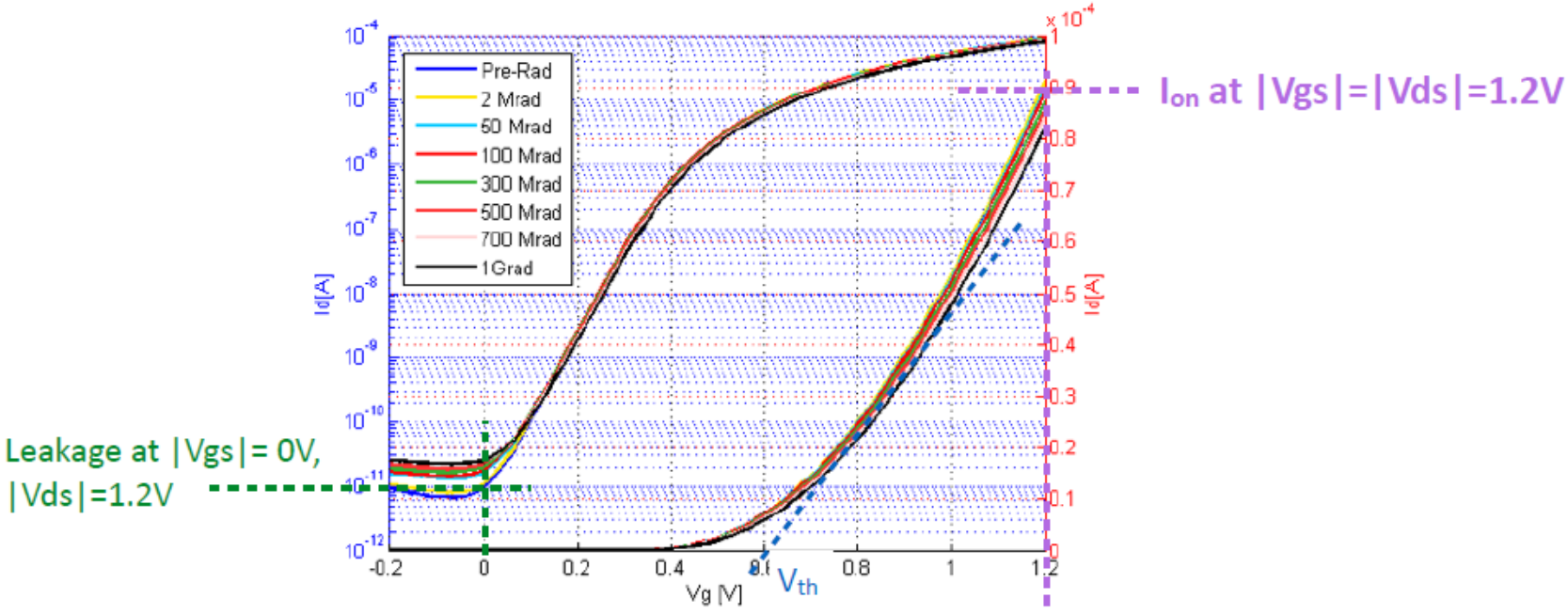


130 nm CMOS technology node (t_{ox} = 2.2 nm)

TID

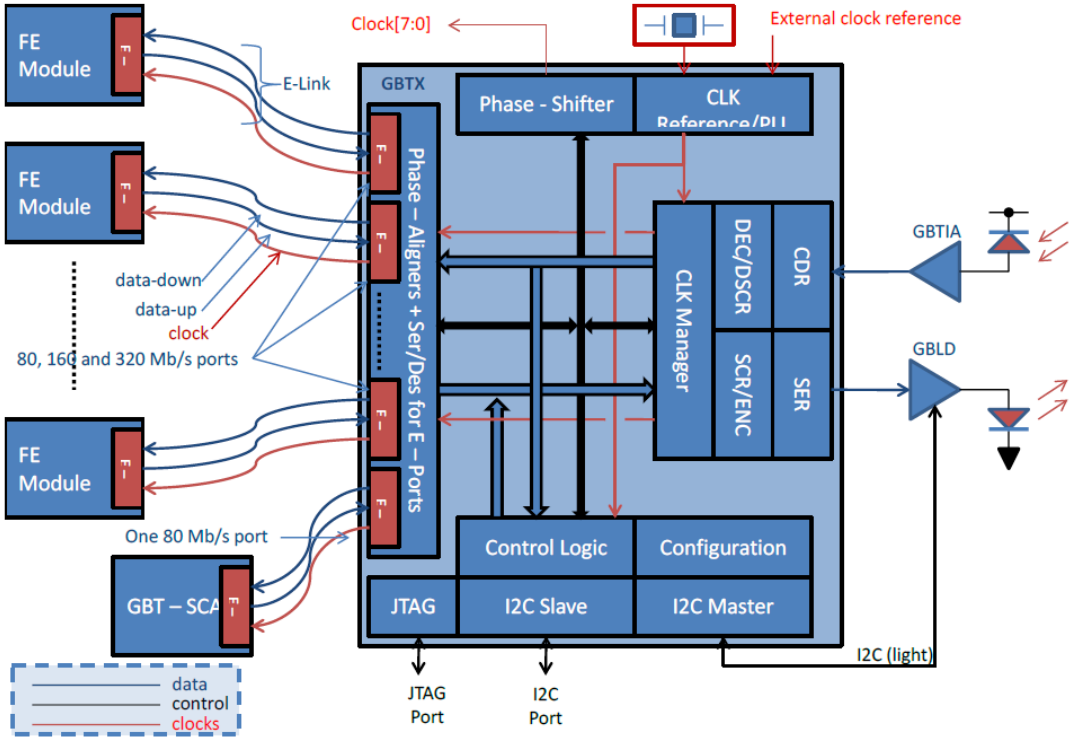
The 130 nm feature size process enjoys an inherently high total dose radiation tolerance of the core transistors

→ **no need for ELTs**



SEU to be proven on each project

GBTx: 130 nm ASIC

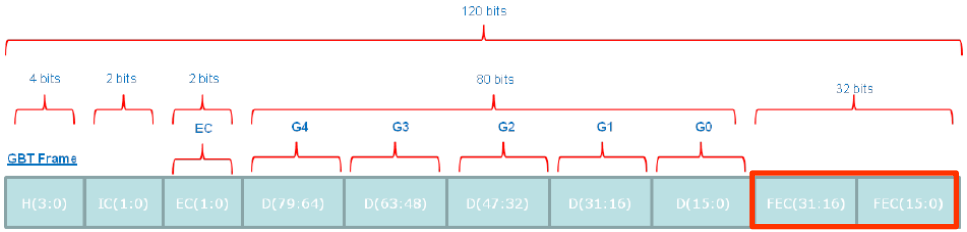


radiation environment:

- **TID:** 100 Mrad
- $\Phi = 10^{16}$ n/cm^2 in 10 years

Mitigation techniques adopted:

- TMR for all 366 configuration registers
- Forward error correction code (**FEC**)
- Watchdog
- 2 SEU-related registers:
  - SEU counter
  - FEC-RX correction counter

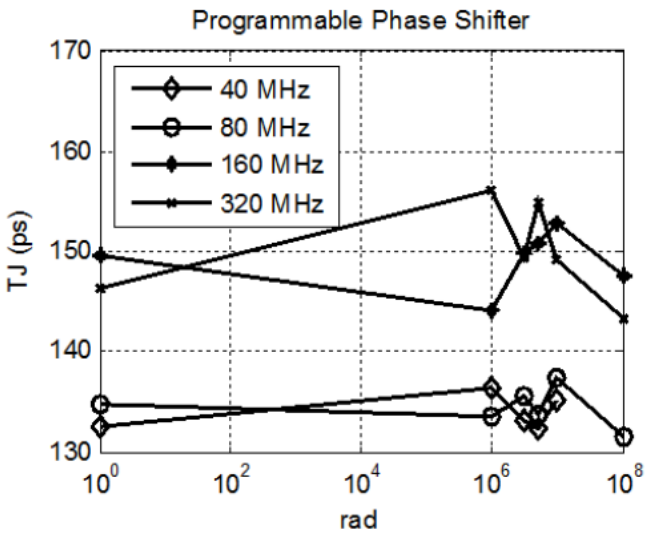


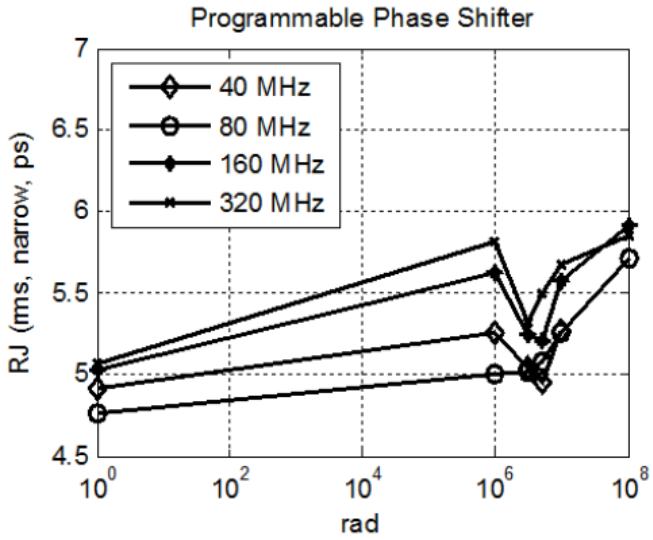
The user bandwidth is 80bits per BC, that is 3.2 Gbps

hardening by design

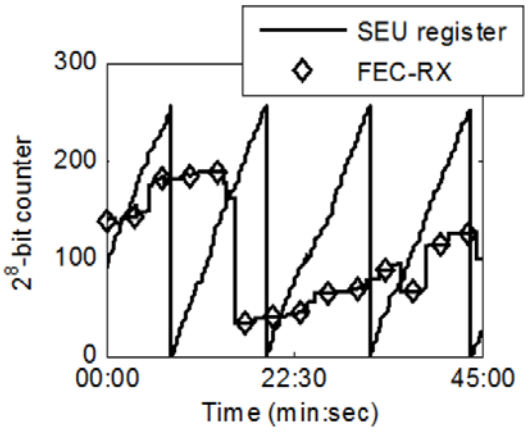
GBTx: 130 nm ASIC

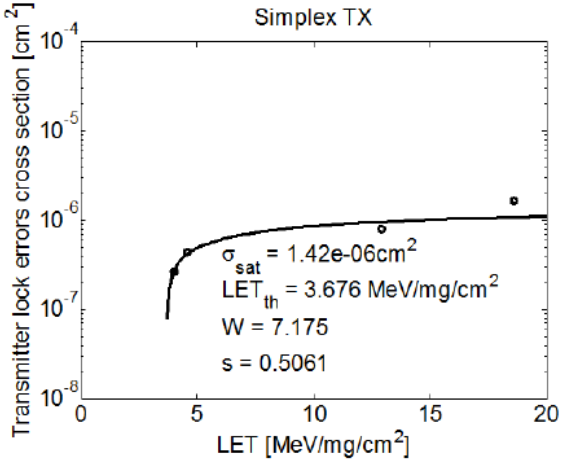
TID (40 KeV X-ray up to 100 Mrad @ 100 krad/min)

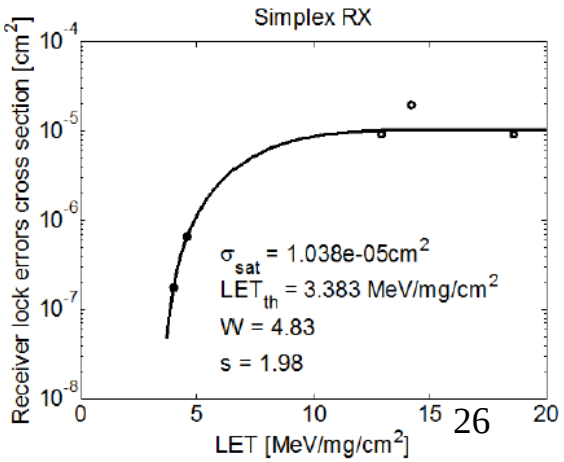




SEU (Heavy Ion Irradiation Facility, Louvain la Neuve)







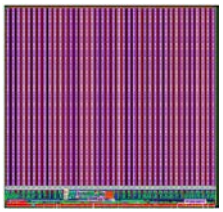
GBTx: 130 nm ASIC

SEU

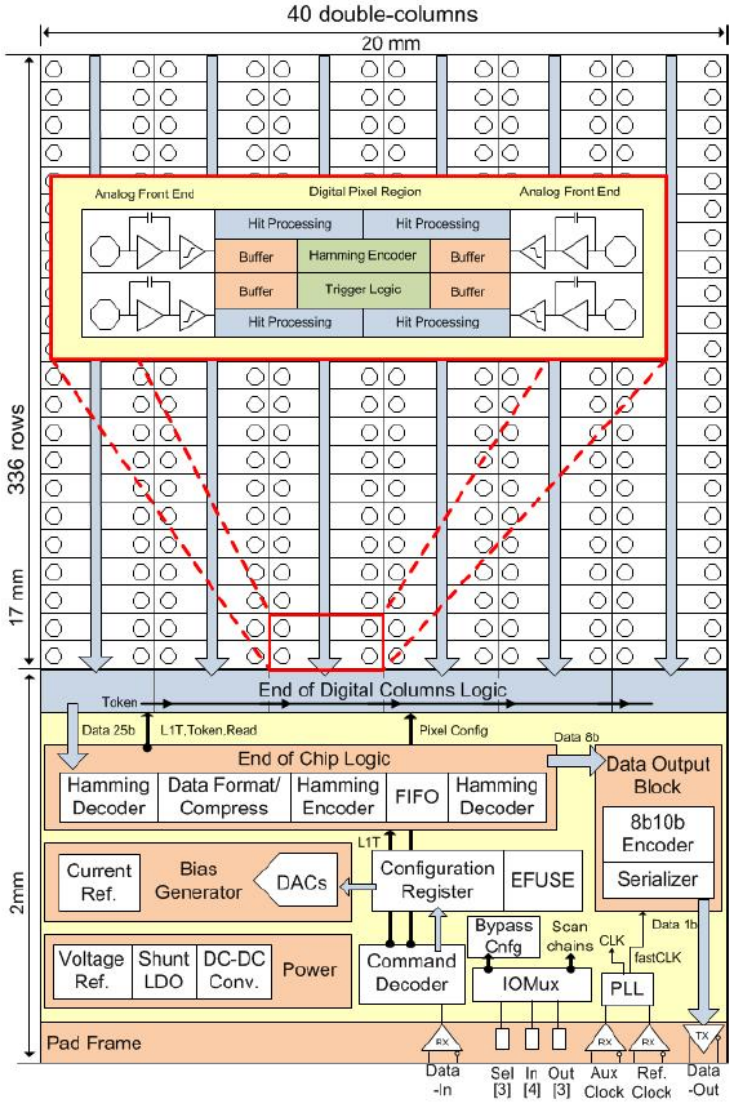
Detector position	Flux (p/cm^2·s)	Lock errors (errors/(device·day))		Frame errors (errors/(device·day))	
		RX	TX	RX	TX
Exp. Hall	8.50E+01	2.5E-05	4.9E-06	-	3.6E-05
Outer Tracker	1.50E+05	5.5E-02	1.0E-02	-	7.0E-02
Endcap ECAL	2.98E+05	0.1	2.2E-02	-	0.2
Pixel	1.40E+07	7.8	1.4	-	10.0

lock & frame errors $\mathbf{R = \sigma\ \Phi}$ expected errors per device per day

FeI4: 130 nm ASIC



80M transistors
matrix of 336x80 pixels
(50x250 μm each)

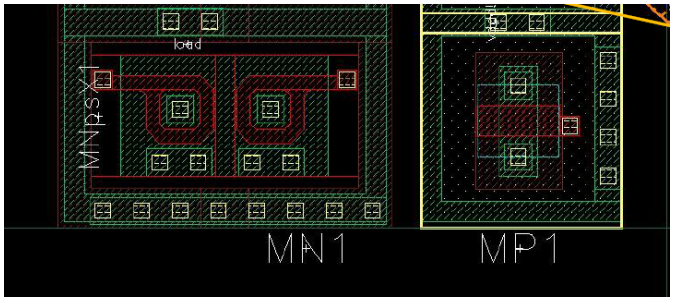


radiation environment:

- 300 Mrad **TID**
- $\Phi = 10^{16}$ n/cm^2 in 10 years

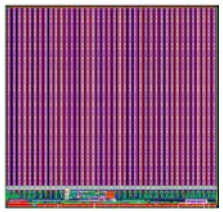
Mitigation techniques adopted:

- Configuration memory with TMR SEU hard custom cells ➔ latches with a Dual Interlocked Cell (**DICE**) architecture
- Digital logic: TMR, Hamming
- Service Record indicating that a SEU has been detected in the command decoder



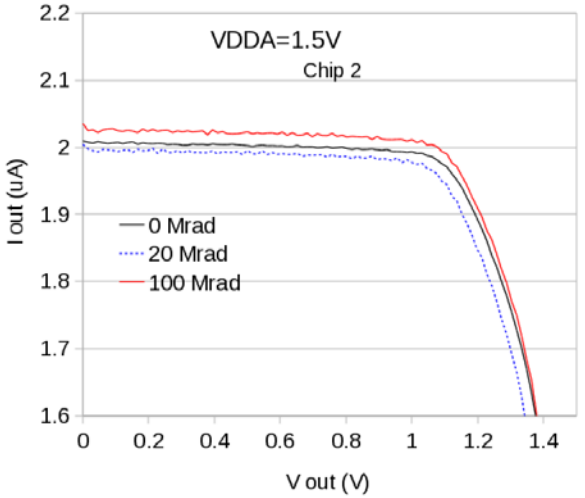
DICE (with ELT !)

FeI4: 130 nm ASIC (irradiation tests before LHC)



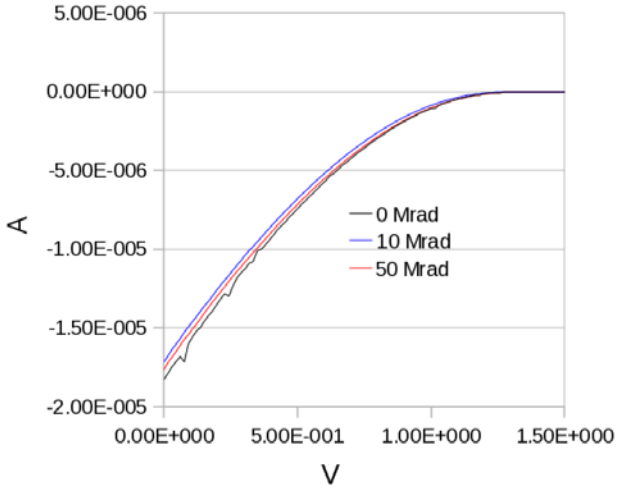
TID (CERN-PS 24 GeV proton beam):

- no change in digital circuits
- current reference variation = 2%
- current mirror variation = 5%
- single pixel noise increase <= 10%



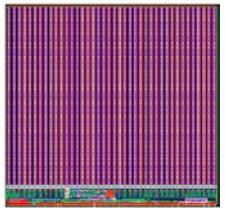
SEU (CERN-PS 24 GeV proton beam):

$\sigma = 2 \times 10^{-16}\ cm^2$



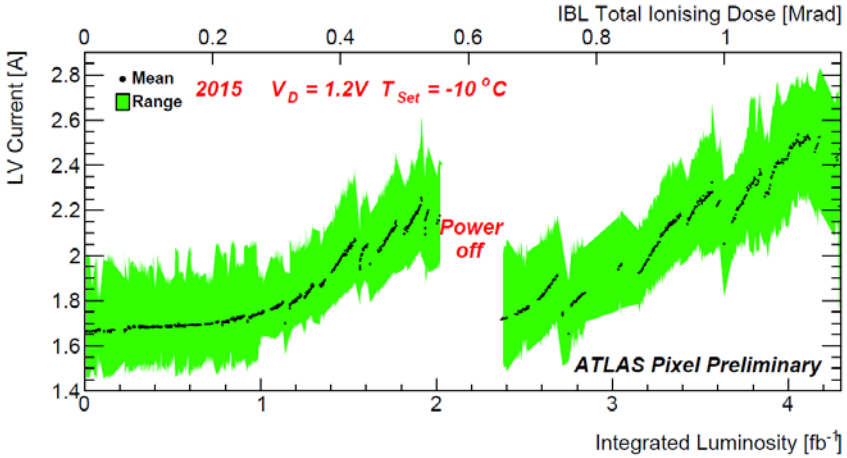
but …

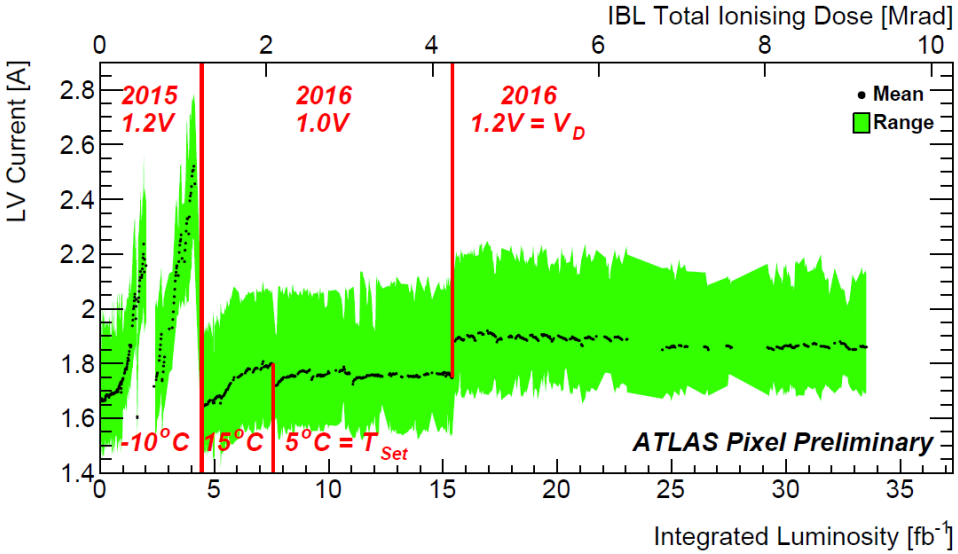
FeI4: 130 nm ASIC (after 2 LHC years)

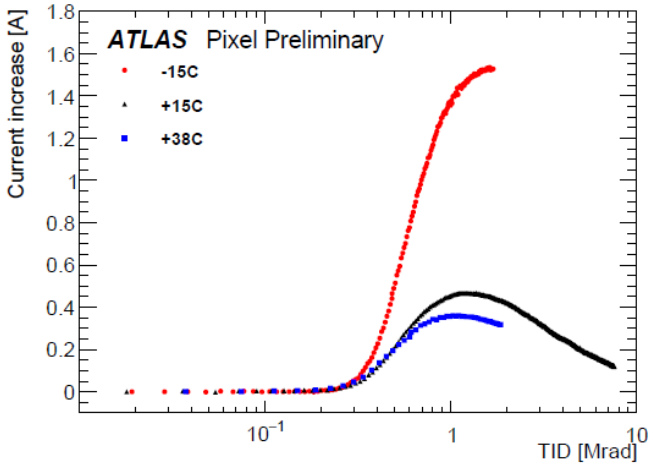


TID

After the first months of IBL data-taking in 2015, a significant increase of the LV current and a shift of the calibration parameters Threshold and ToT were measured.





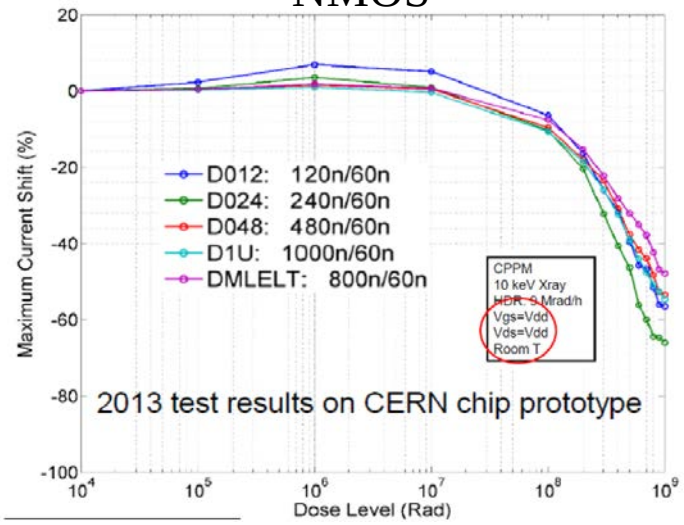


The operating temperature change allowed to stabilize the LV current oscillations

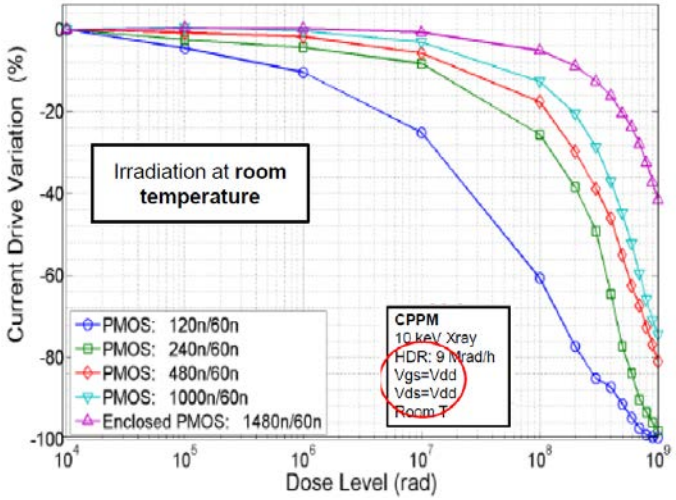
65 nm CMOS technology node (t_{ox} = 1.4 nm)

TID

NMOS



PMOS



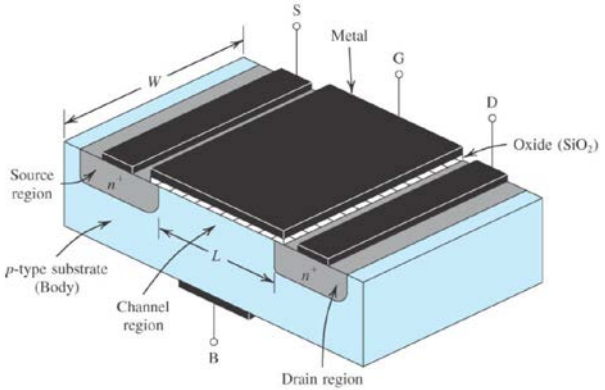
large reduction of I_{ON} for short channel devices

➔ L >= 120 nm

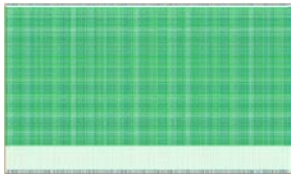
min size PMOS are OFF for **TID** > 500 Mrad

➔ L >= 120 nm, W >= 300 nm

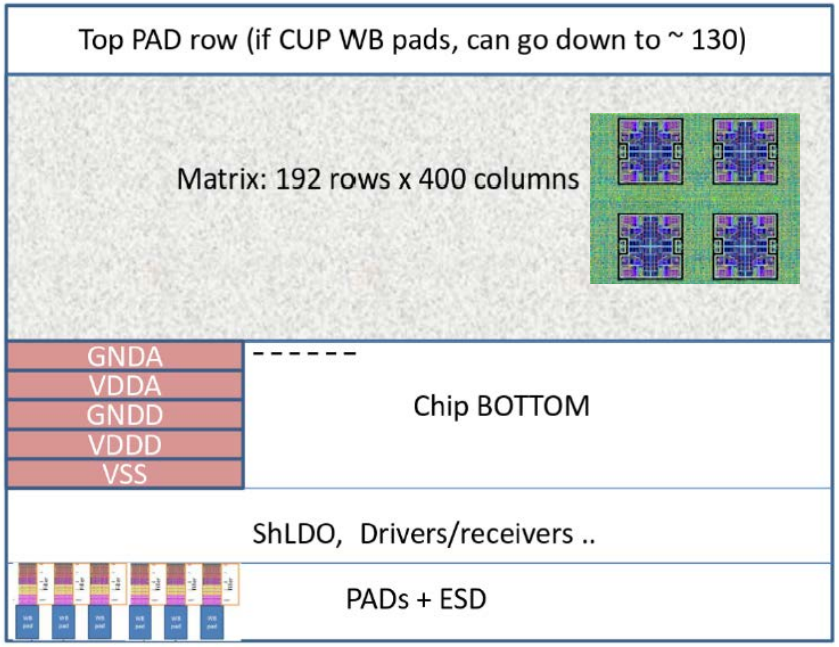
SEU: I did not find anything yet



RD53A: 65 nm ASIC



500M transistors
matrix of 192x400 pixels
(50x50 μm each)



radiation environment:

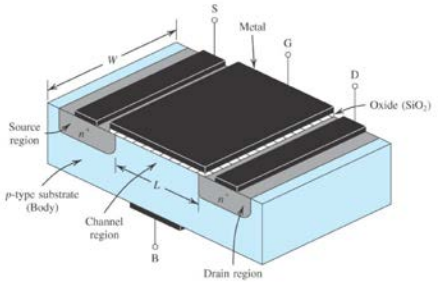
- 500 Mrad **TID**
- $\phi = 5\ 10^6$ n/cm^2 sec

Mitigation techniques adopted:

- global configuration memory is protected with TMR DICE latches
- pixel configuration is protected with DICE latches
- protection of memories and state machines
- SEU-soft dummy registers for monitoring
- **trickle configuration** (continuous external refreshing) → no SEU hard config needed!

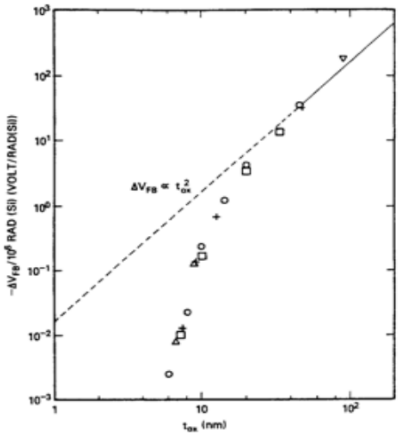
Recommendations (up to **500 Mrad**)

- **Cold** operation < -15°C
- For analog designs:
  - NMOS: **L ≥ 120nm**, any W Ok
  - PMOS: **W ≥ 300nm**, L ≥ 120nm



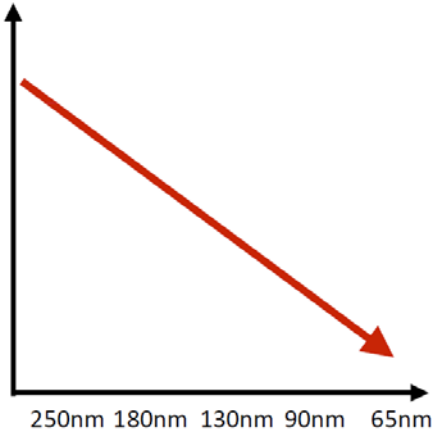
Rad-tol ASIC summary

TID damage



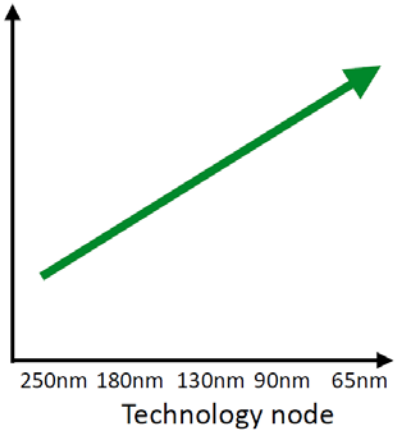
Gate t_{ox}

+



TID tolerance

=



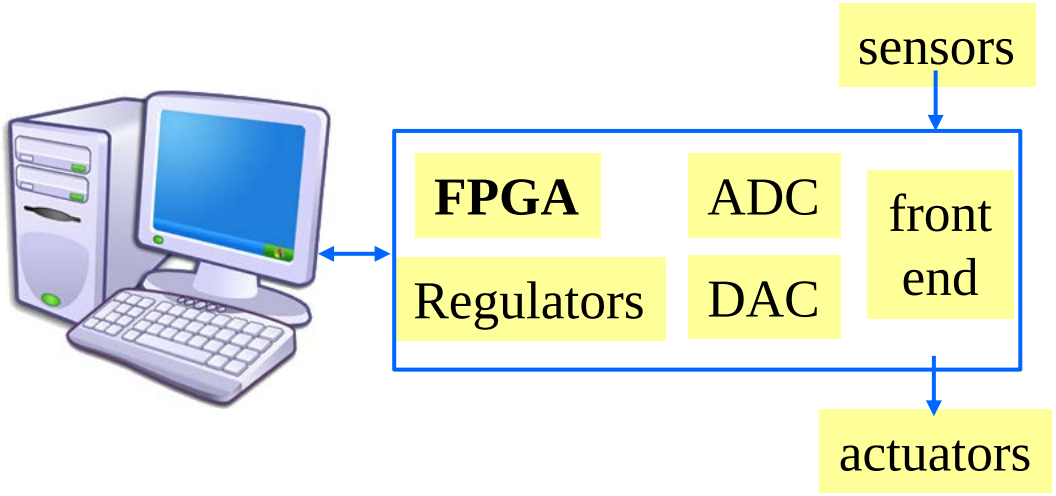
not always true !!!

all processes

Radiation tolerance varies in different fabs and can change over time. It is necessary:

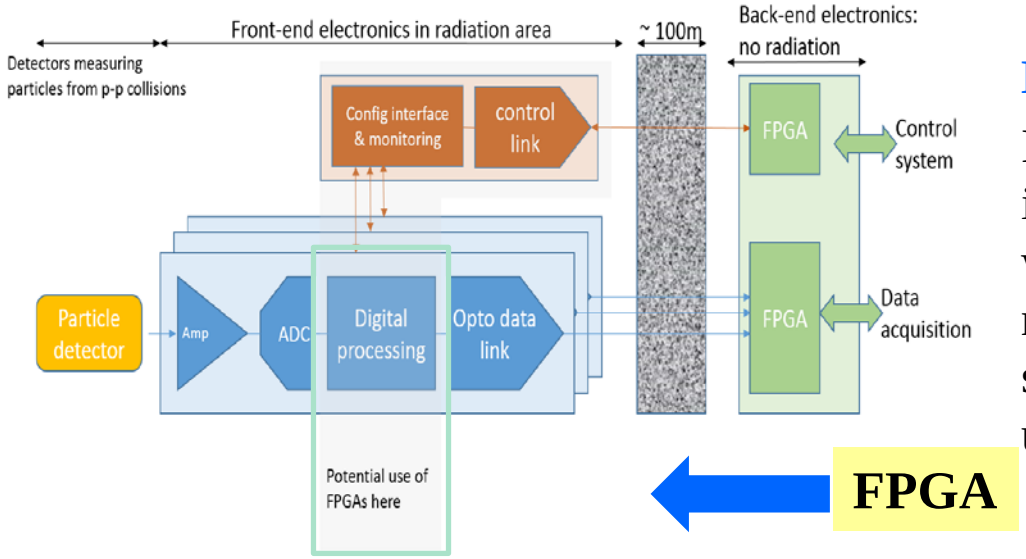
- to only qualify and use one fab
- to pay attention to W/L
- to carefully qualify each ASIC during the prototyping and production phases
- qualify **TID** and **SEE** for each chip depending on the environment it will have to work in

Accelerator and experiment equipment using COTS FPGAs in radiation areas



Accelerator

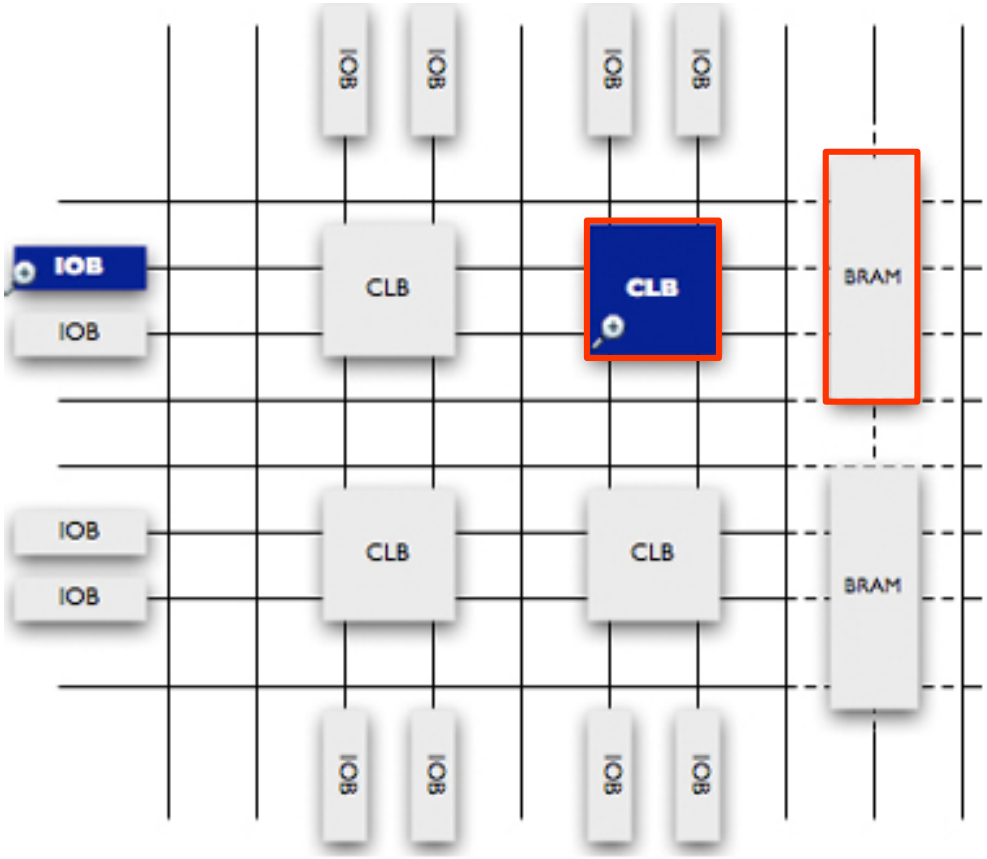
- Cryogenics
- Power Converter
- Quench protection system
- Beam Instrumentation



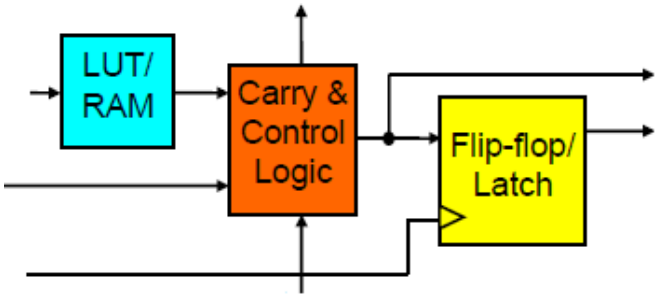
Experiments

In the HEP front-end electronics installed around 2005, FPGAs were mostly used for control and readout logic with external high speed links. With the current upgrades FPGAs are moving in …

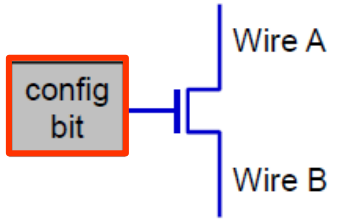
Architecture of a FPGA



CLB: Configurable Logic Block



logic + BRAM

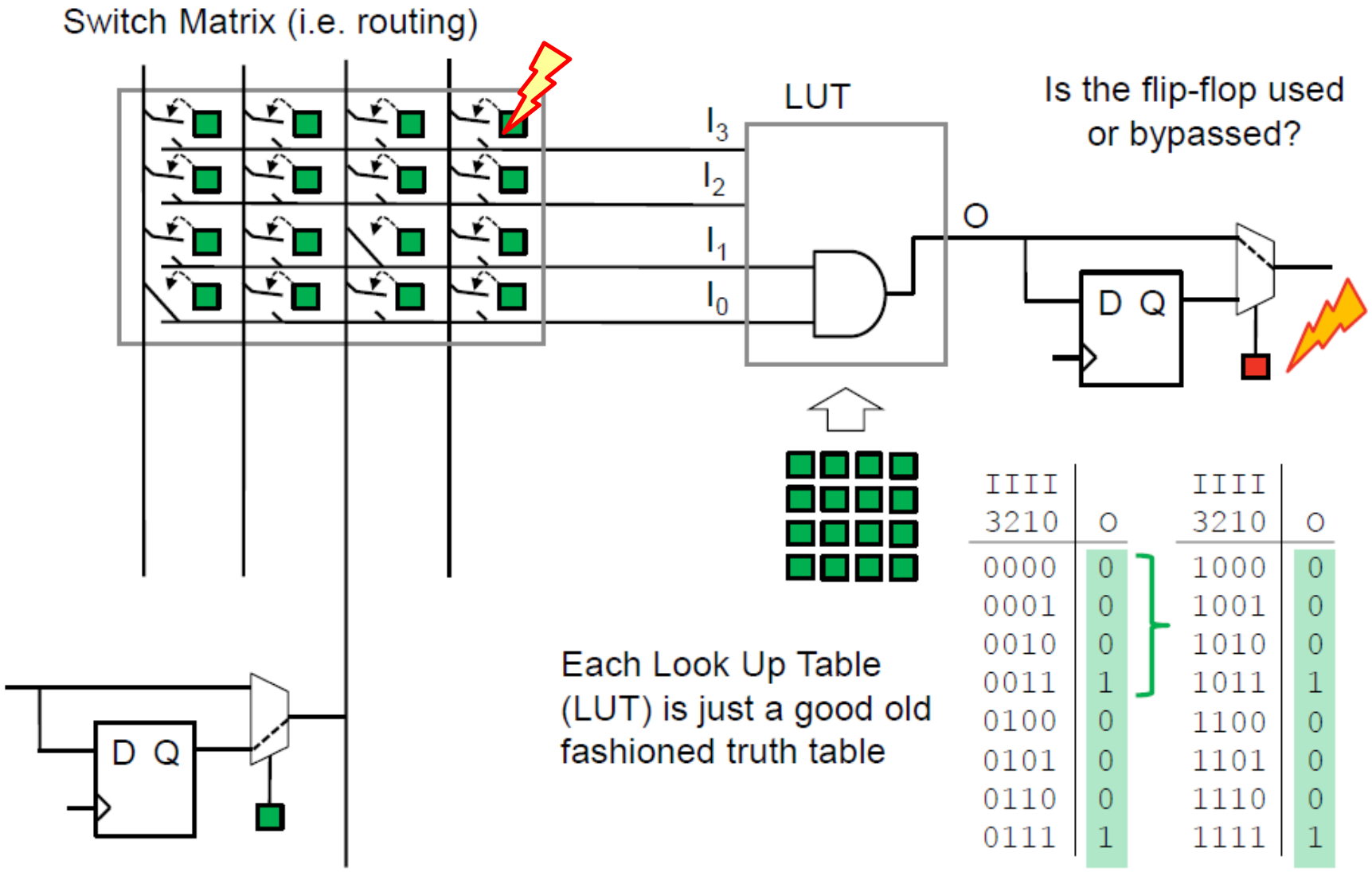


switch

configuration memory

FPGA: it is a user-programmable matrix of logic blocks with programmable interconnections that can implement **any** logic function or algorithm.

SEUs affecting configuration memory



IIII 3210	O
0000	0
0001	0
0010	0
0011	1
0100	0
0101	0
0110	0
0111	1

IIII 3210	O
1000	0
1001	0
1010	0
1011	1
1100	0
1101	0
1110	0
1111	1

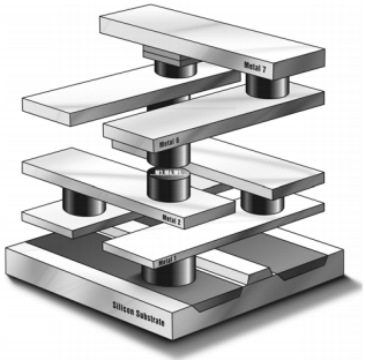
On the market: rad-tol FPGAs & COTS FPGAs

Radiation tolerant FPGAs

configuration memory technology

Microsemi

Antifuse

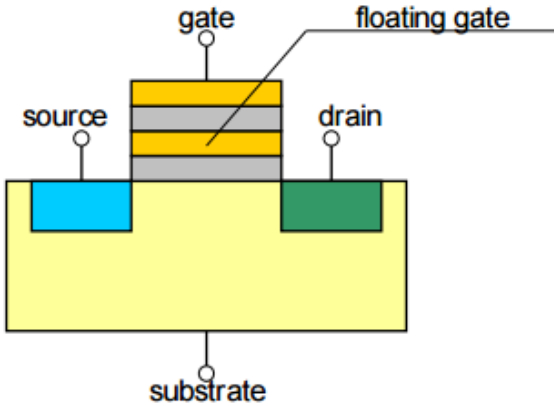


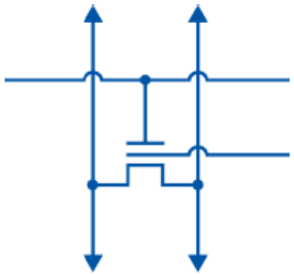
The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection

RTAX, RTSX

Microsemi

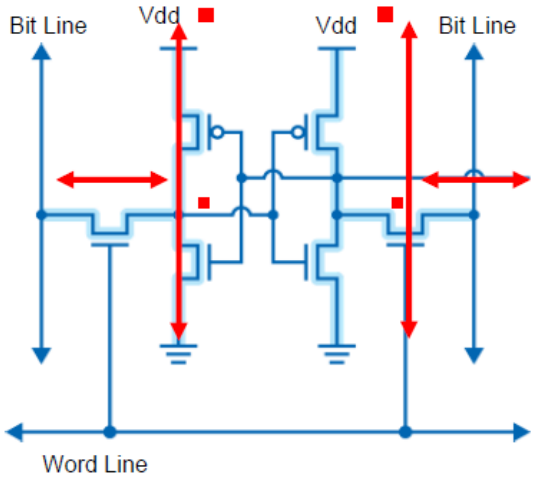
Flash





XILINX

SRAM



XQR5VFX130

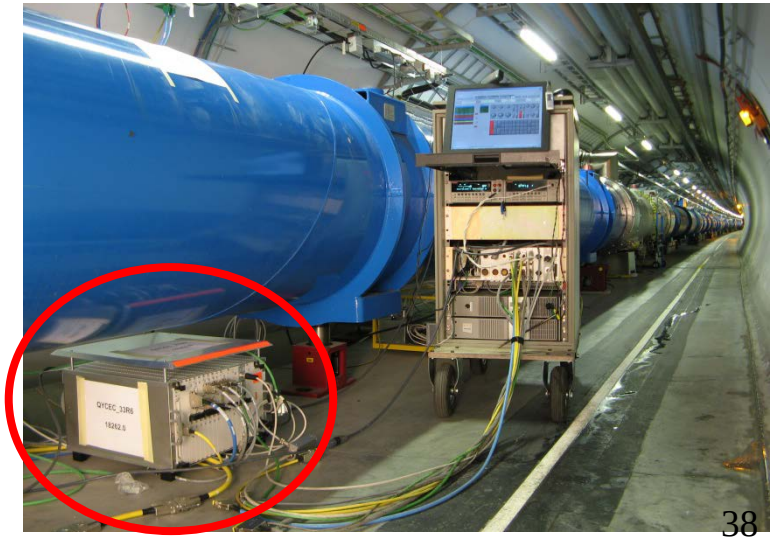
Why choosing a RT Antifuse?

PROs:

- reliability:
  - SEL immune
  - TID:
    - OK up to 300 krad
  - SEU:
    - σ < 1E-9 cm^2
    - LET_{TH} > 37 MeV cm^2/mg
    - RAM bits SEU rate < 1E-10 upsets/bit-day (worst case GEO)
  - no errors in the configuration memory by design
- long life time

CONs:

- very small code possible
- OTP
- **high cost**
- programming not always successful

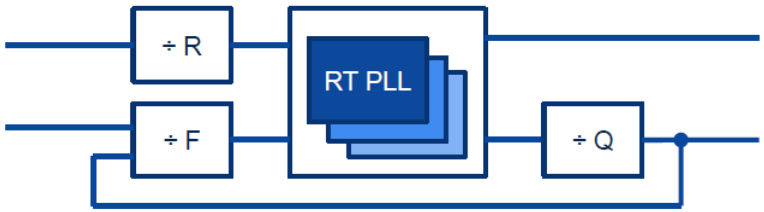


Rad-tol FPGAs: RTG4 (Microsemi Flash based)

UMC 65 nm process

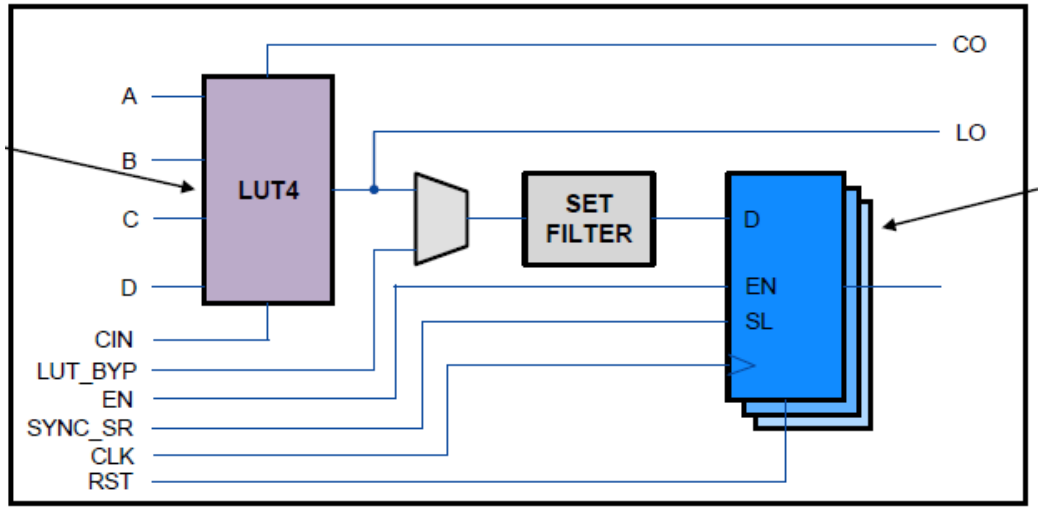
PROs:

- reliability:
  - SEL immune up to 103 MeV cm^2/mg
  - TID:
    - OK up to 125 krad
  - SEU:
    - σ < 1E-11 errors/bit/day
    - LET_{TH} > 37 MeV cm^2/mg
    - RAM bits SEU rate < 1E-10 upsets/bit-day (worst case GEO)
  - no errors in the configuration memory by design
- long life time
- a lot of resources



CONs:

- **high cost**



TMR FF

Rad-tol FPGAs: XQR5VFX130 (Xilinx SRAM based)

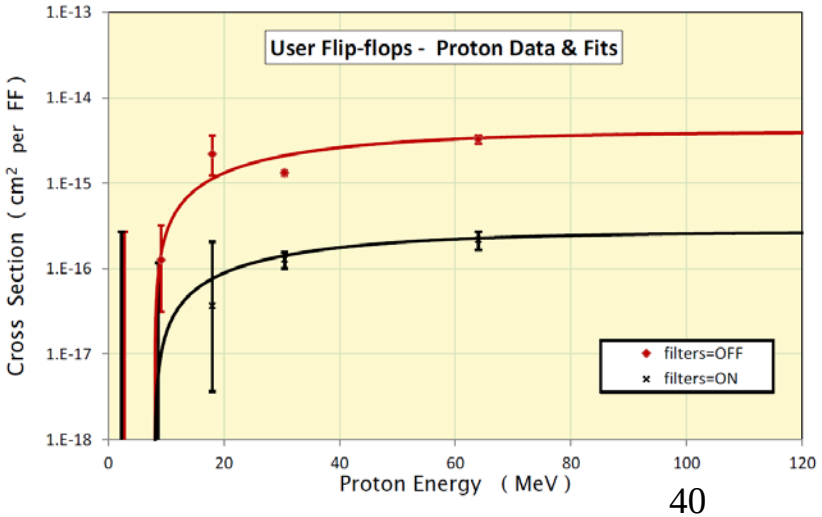
PROs:

- reliability:
  - SEL immune up to 100 MeV cm^2/mg
  - TID:
    - OK up to 1 Mrad(Si)
  - SEU:
    - sigma < $3.8E^{-10}$ errors/bit/day (worst case GEO)
  - SEU Hardened Configuration Memory Cells
- long life time
- a lot of resources (Virtex5 equivalent)

65 nm process

CONs:

- **high cost**
- need to use an old ISE version (13.2)



COTS FPGAs

configuration memory technology

Antifuse

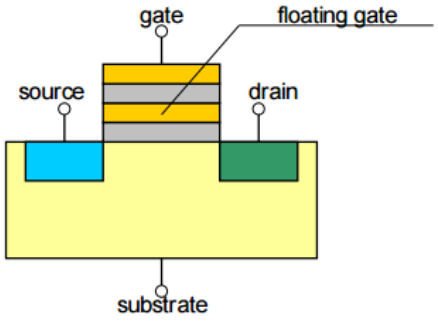
Axcelerator® FPGAs
- Nonvolatile, high-speed antifuse FPGAs
- 125K - 2M system gates
- 350 MHz system performance
- 0.15 µm, CMOS antifuse process

SX-A FPGAs
- Sea-of-modules antifuse FPGAs
- 12K - 108K system gates
- 250 MHz system performance
- 66 MHz PCI compliant

eX FPGAs
- Low-power, low-density antifuse FPGAs
- 3K - 12K system gates
- 350 MHz system performance
- 0.22 µm CMOS antifuse process

MX FPGAs
- Mixed-voltage and 5 V-only operation
- 3K - 54K system gates
- 250 MHz system performance a
- Dual-port SRAM modules & multiplex I/O

Flash



Microsemi SmartFusion®2 SoC FPGA 65 nm

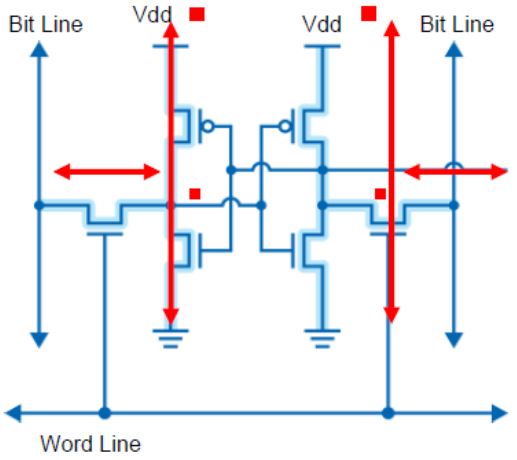
Microsemi IGLOO®2 FPGA 65 nm

Microsemi PolarFire® FPGA 28 nm

Microsemi ProASIC®3 FPGA 130 nm

ProASICPlus 220 nm

SRAM

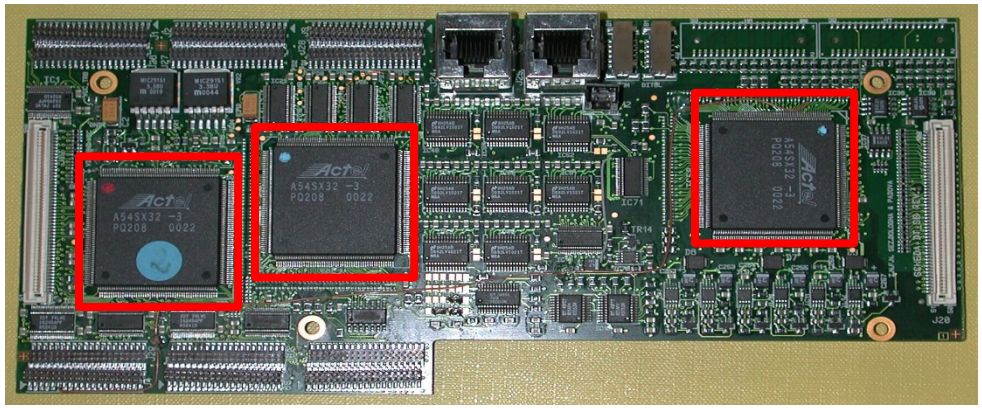


Example: pASIC A54SX32

CMS Muon Barrel radiation environment (in 10 years):

ϕ:	3×10^{10} cm^{-2}
ϕ (neutrons with energy > 20 MeV):	1×10^{9} cm^{-2}
TID:	0.01 krad

p @ 59 MeV

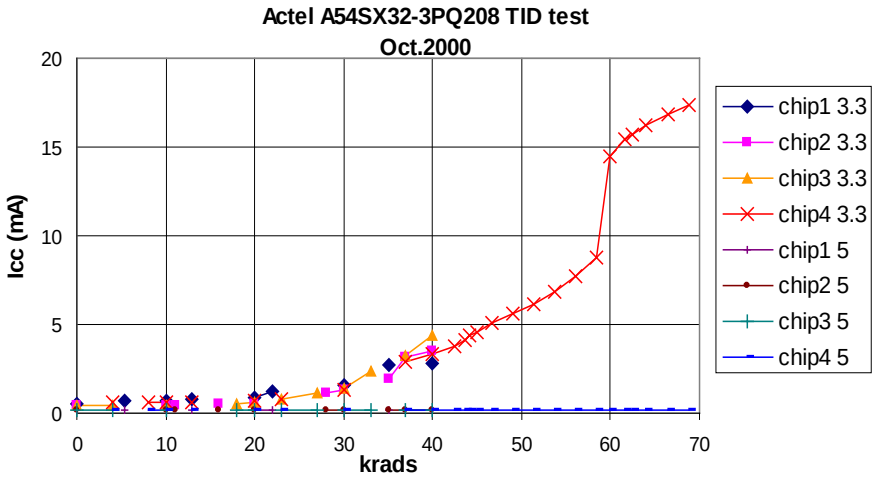


- **Louvain La Neuve** Cyclotron → proton beam
- beam energy: 30 – 65 MeV
- **Φ**: 10^{8} p cm^{-2} s^{-1} (can be reduced to 10^{7} p cm^{-2} s^{-1})
- beam composed by bunches of 7 ns @ 18.3 MHz
- circular section, ∅ 10 cm, uniform density
- equivalence factor: 10^{9} proton cm^{-2} = 1.4 Gy

Example: pASIC A54SX32

- 2 450 bits registers each
- refreshed and monitored @ 1 MHz
- monitoring cycle:
  1. read monitor register
  2. load target register
  3. read monitor register
- searching for **transient** and **static** upset events

TID



SEE

• 1 observed event, for the Actel A54SX32 chips tested (w/o dividing by the # of FF in a chip)

$\sigma_{SEU} < 2.9\ 10^{-12}\ cm^2$ 90% u.l., for 59 MeV protons

• Following **Huhtinen** and **Faccio**, we calculate for the entire TSM system of 750 chips

***R* < 2.2 SEU in 10 years of DT running**

Microsemi Power Matters.
PROASIC®3 FPGA
130 nm

→ medium radiation levels

- PROs:
  - TID limit: ~500 Gy
  - SEL immune
  - configuration memory upset immune
  - small σ_{SEU} with TMR
  - Reprogrammable

- CONs:
  - TID limit is lower than the antifuse
  - reprogrammability feature not working above 200 Gy
  - limited resources in terms of logic gates (i.e. DSP math)

The **GEFE** board is a multipurpose FPGA-based radiation tolerant card. Its intended use ranges from fast data acquisition systems to slow control installed close to the beamlines, in a radioactive environment exposed to total ionizing doses of up to **50 krad** (500 Gy).

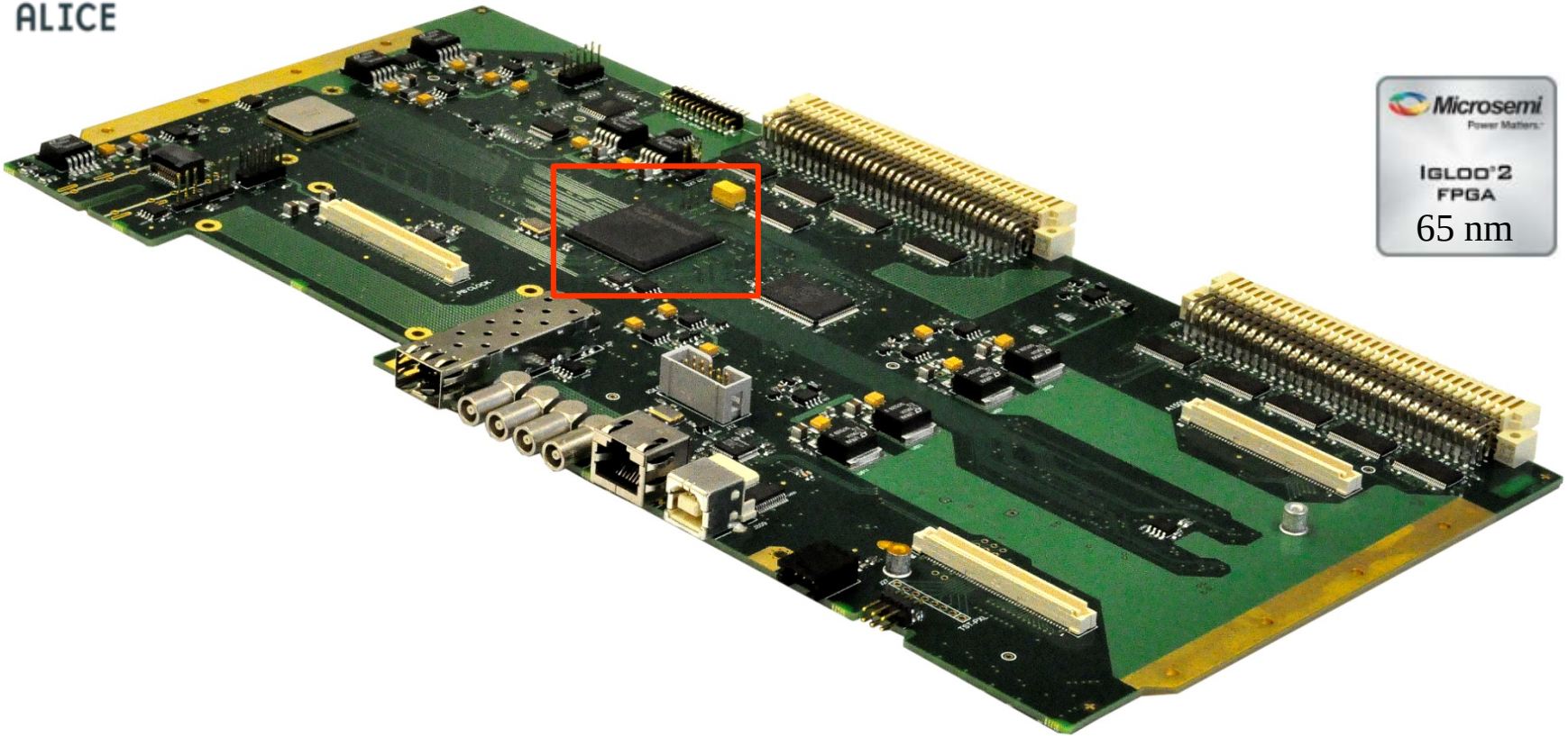
→ low radiation levels

- PROs:
  - TID limit: ~250 Gy
  - **configuration memory upset immune** up to 90.3 MeV cm^2/mg
  - SEL immune up to LET = 24 MeV cm^2/mg
  - small σ_{SEU} with TMR
  - reprogrammable
  - **cheap**

- CONs:
  - TID limit is lower than the ProASIC3
  - **charge pump circuit + Flash transistors sensitive to TID**
  - development tools not so evolved

Feature	Test Fluence (Neutrons/cm^2)	Error Rate Ground Level (Sea Level, NYC, FIT)	Error Rate Aviation (40,000', NYC, FIT)
Flip-flop	4.35 x 10^{11}	218.3 FIT / million flip-flops	1.13 x 10^5 FIT / million flip-flops
LSRAM	1.7 x 10^{11}	340.6 FIT / million bits	1.75 x 10^5 FIT / million bits
uSRAM	1.7 x 10^{11}	175.3 FIT / million bits	9.04 x 10^4 FIT / million bits

Application: DRM2 for ALICE TOF



ϕ: 2.6 10^{10} n/cm^2 (1 MeV neutron equivalent)

Φ: 0.26 KHz/cm^2 (> 20 MeV hadrons)

TID: 0.13 Krad

72 DRM2 boards are needed

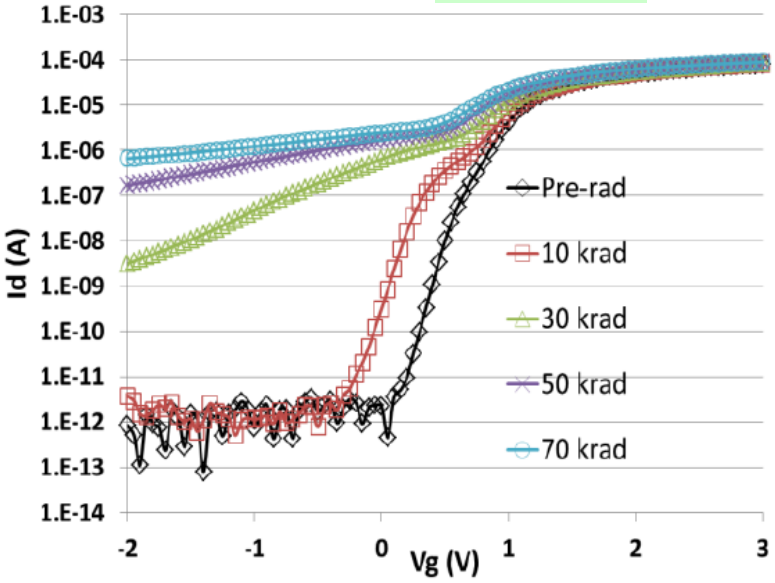
Beware! Igloo2 vs RTG4 under radiation

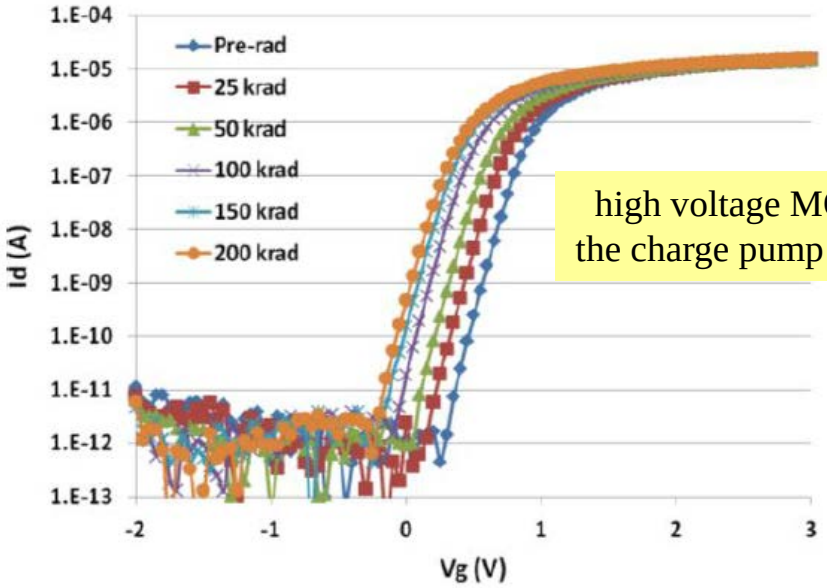
TID

Igloo2

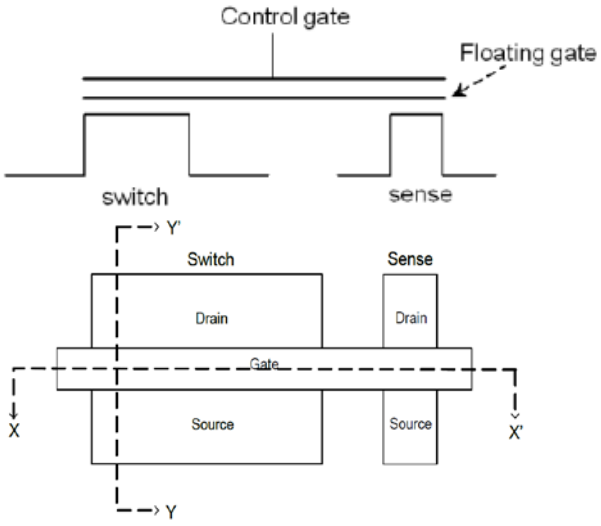
t_{ox} = 29 nm

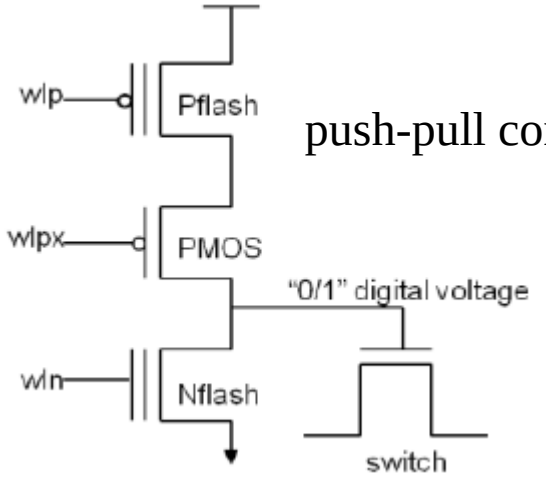
RTG4





high voltage MOS in the charge pump circuit



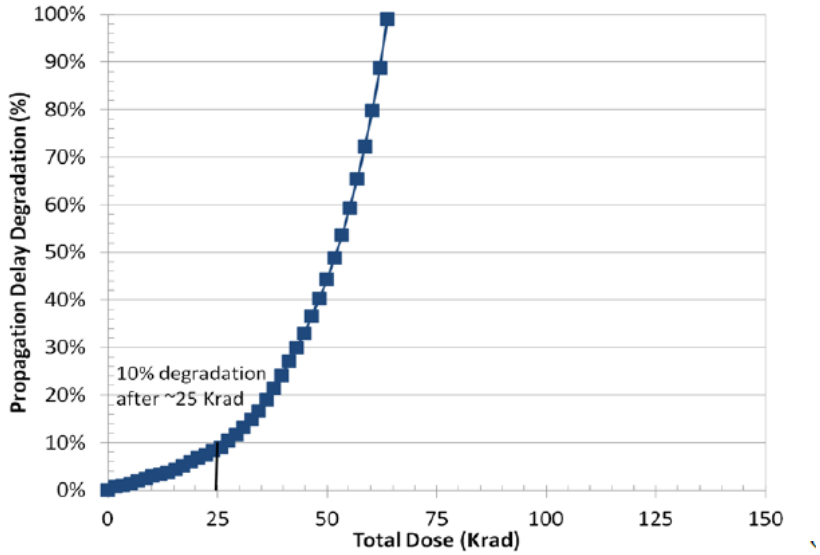


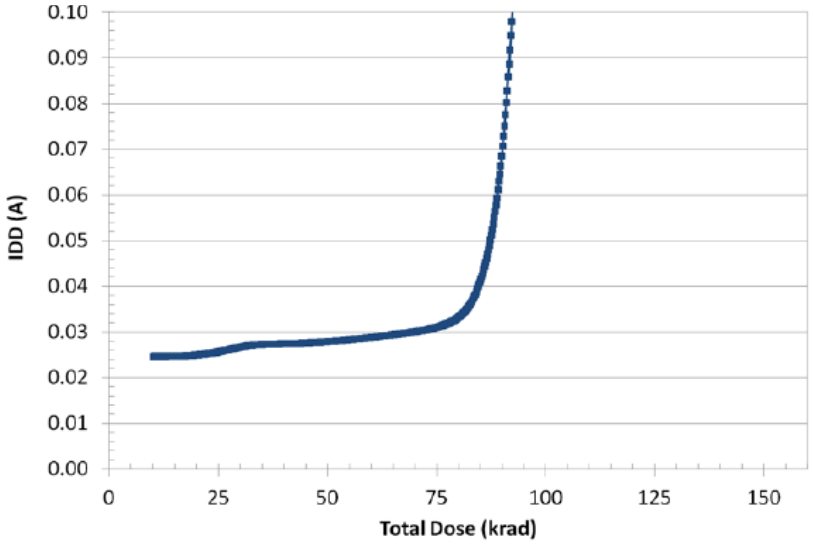
push-pull configuration

Beware! Igloo2 vs RTG4 under radiation

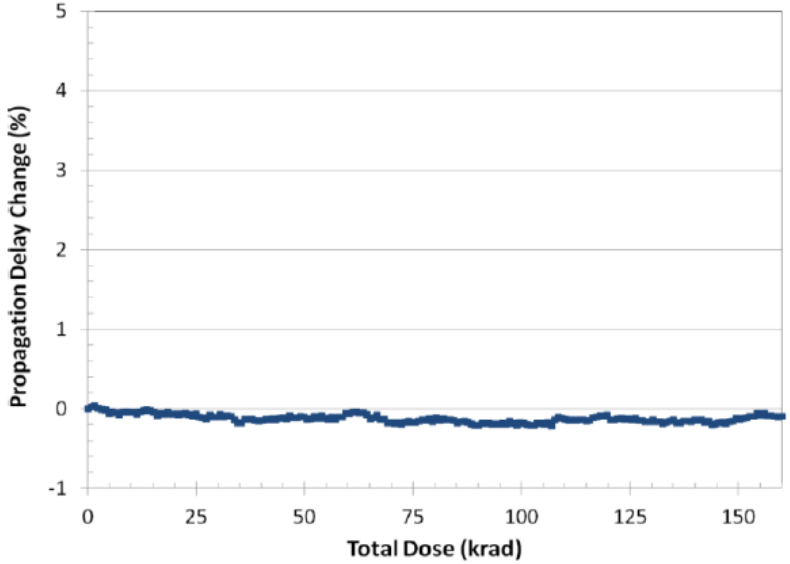
TID

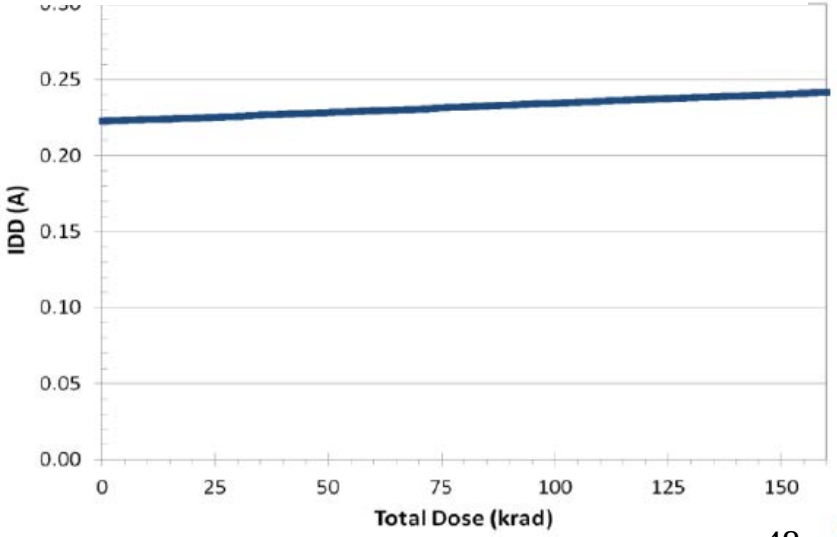
Igloo2





RTG4

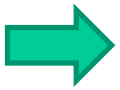




XILINX intel FPGA → **medium radiation levels**

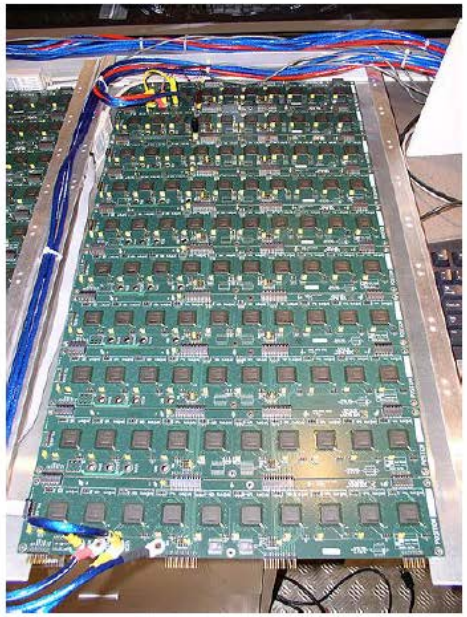
- PROs:
  - plenty of resources, up to date technologies
  - powerful development tools
  - **high TID endurance**
  - not too expensive
  - lot of literature available

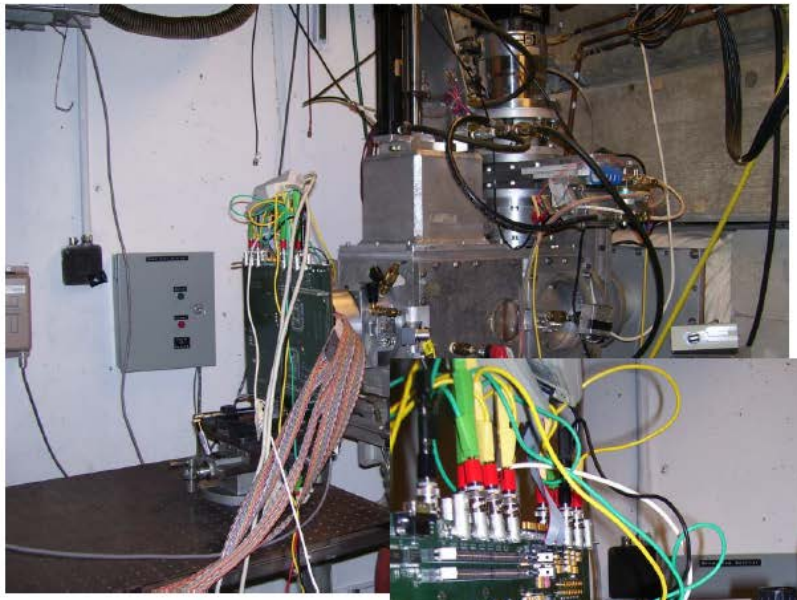
- CONs:
  - **SEUs in configuration memory → scrubbing needed**
  - mitigation needed for FFs and Block RAM
  - they have to be rad-qualified on the field

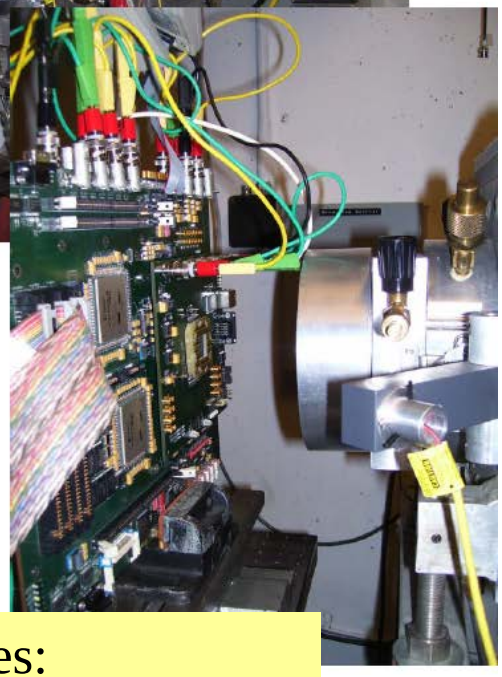


the only choice with high **TID** requirement

Rosetta project

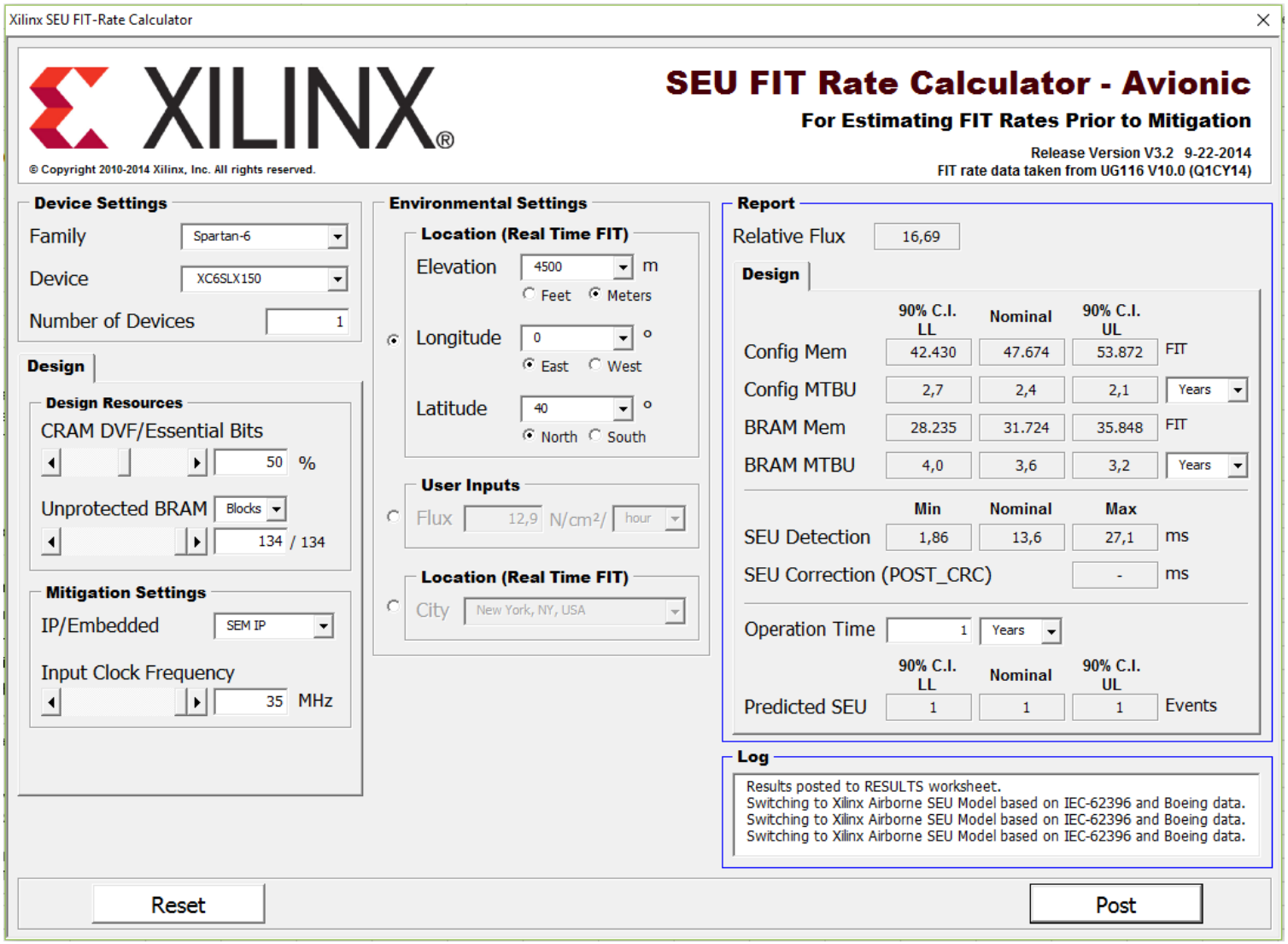






Test currently is operational at 3 altitudes:
– at sea level in San Jose
– at 5,200 feet in Albuquerque
– at 12,250 feet at White Mountain Research Center

SEU fit rate calculator



Xilinx FPGAs neutron cross section per bit

Technology Node	Product Family	Neutron Cross-section per Bit[1]			FIT/Mb (Alpha Particle)[2]			FIT/Mb [6] (Real Time Soft Error Rate)[3]		
		Config. Memory	Block	Error	Config. Memory	Block RAM	Error[4]	Config. Memory	Block RAM	Error[4]
250 nm	Virtex	9.90×10^{-15}	9.90×10^{-15}	±18%				160	160	±20%
180 nm	Virtex-E	1.12×10^{-14}	1.12×10^{-14}	±18%				181	181	±20%
150 nm	Virtex-II	2.56×10^{-14}	2.64×10^{-14}	±18%				405	478	±8%
130 nm	Virtex-II Pro	2.74×10^{-14}	3.91×10^{-14}	±18%				437	770	±8%
90 nm	Virtex-4	1.55×10^{-14}	2.74×10^{-14}	±18%				263	484	±11%
90 nm	Spartan-3	2.40×10^{-14}	3.48×10^{-14}	±18%				190	373	–50% +80%
90 nm	Spartan-3E Spartan-3A	1.31×10^{-14}	2.73×10^{-14}	±18%				104	293	–80% +90%
65 nm	Virtex-5	6.70×10^{-15}	3.96×10^{-14}	±18%				165	692	–13% +15%
45 nm	Spartan-6	1.00×10^{-14}	2.20×10^{-14}	±18%	135	180	–50% +100%	188	395	–11% +12%
40 nm	Virtex-6	1.26×10^{-14}	1.14×10^{-14}	±18%	9	94	-48% +110%	106	251	-12% +14%
28 nm	7 series FPGAs	6.99×10^{-15}	6.32×10^{-15}	±18%	25	22	-64% +374%	83	75	-13% +15%

Example (Φ = 0.26 KHz/cm^2)

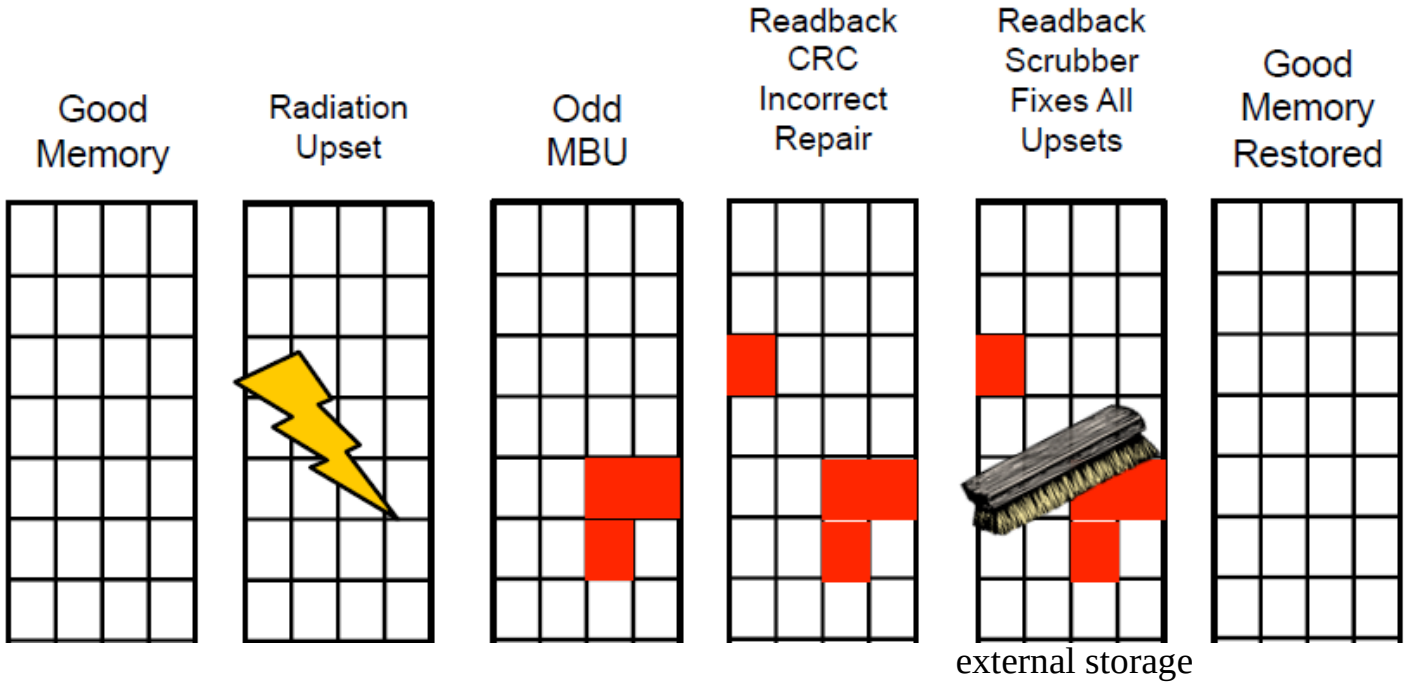
$R = \sigma \times \Phi = 6.32\ 10^{-15} \times 260 = 1.6\ 10^{-12}$ SEUs /(bit s)

For Kintex7 XC7K325T & 72 devices

N_{CRAM}= 67930000 → 1 10^{-4} SEUs/(device s) → 1 SEU/2.7 h → **1 SEU/3min in total**

N_{BRAM}= 16404480 → 2 10^{-5} SEUs/(device s) → 1 SEU/13 h → **1 SEU/11 min in total**

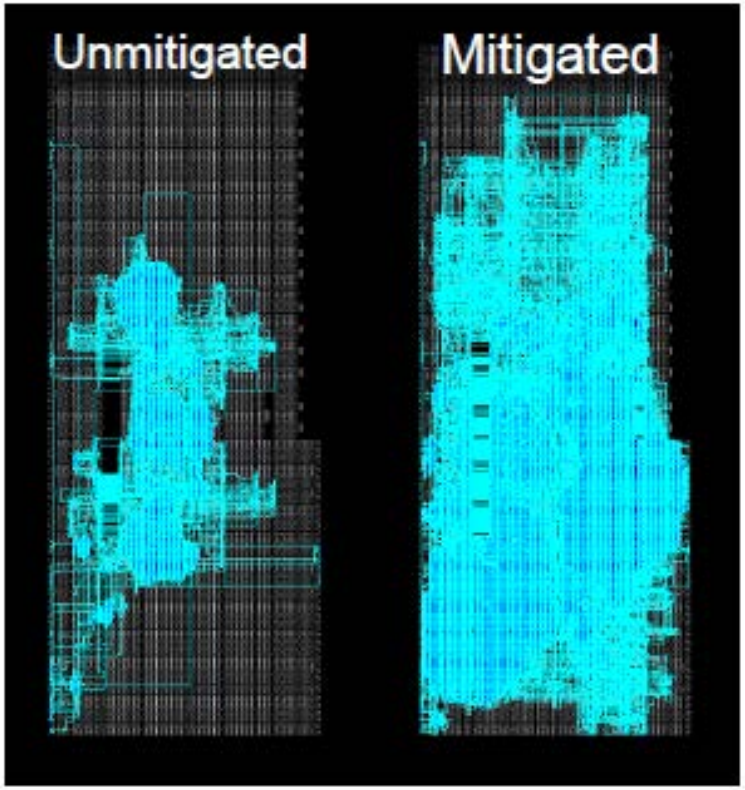
SRAM based FPGA configuration memory: scrubbing



Upset Type	Detection	Correction	Total Scrubbing
SBUs	8.02 ms	4.5 us	8.024 ms
Two-Bit	8.02 ms	1.86 ms	13.38 ms
Odd MBUs	16.04 ms	1.86 ms	21.40 ms
Even MBUs	8.02 ms	1.86 ms	13.38 ms
Full Readback Scrub	1.82 s	1.86 ms	1.822 s

Scrubbing can be done with an internal device (like **SEM IP**) or an external rad-tol device

FPGA TMR: the cost of mitigation

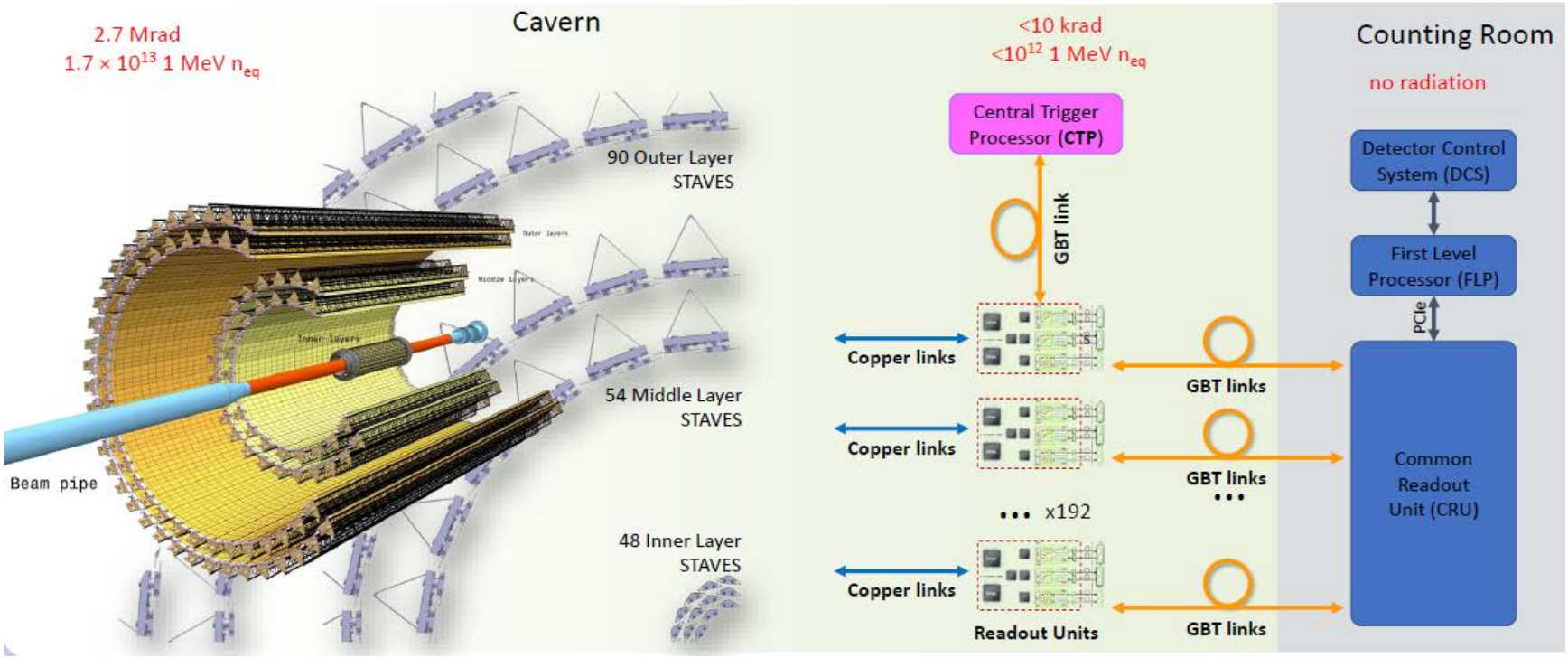


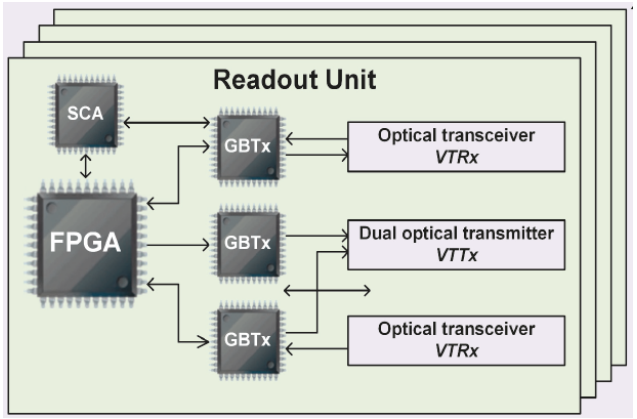
from Michael J. Wirthlin

Description	Unmitigated	TMR No Scrubbing	TMR BRAM Scrubbing	TMR FPGA Scrubbing	TMR Both Scrubbing
Faults Injected (n)	1,831,859	1,369,445	1,502,340	8,840,565	29,443,885
Observed Failures (k)	6,501	1,200	1,100	1,150	2,037
MTBF	282	1,141	1,366	7,687	14,455
Est. Sensitive Bits	240,539	59,393	49,627	8,817	4,689
Improvement	1.00×	4.05×	4.85×	27.28×	51.30×

Synopsys Synplify Premier SW helps implementing TMR

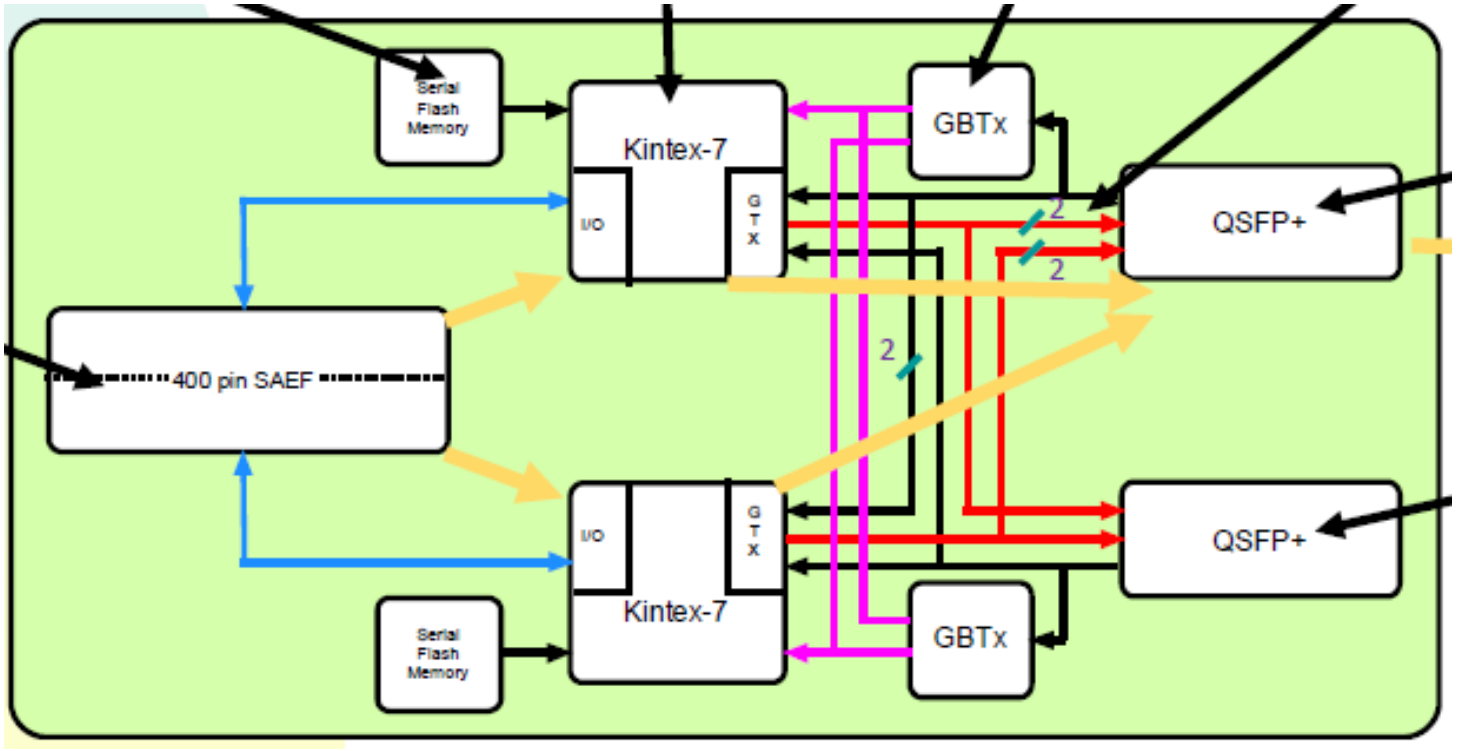
Choosing SRAM-based FPGAs: ALICE ITS upgrade





error mitigation by external scrubbing + TMR !

Choosing SRAM-based FPGAs: ATLAS TileCal upgrade



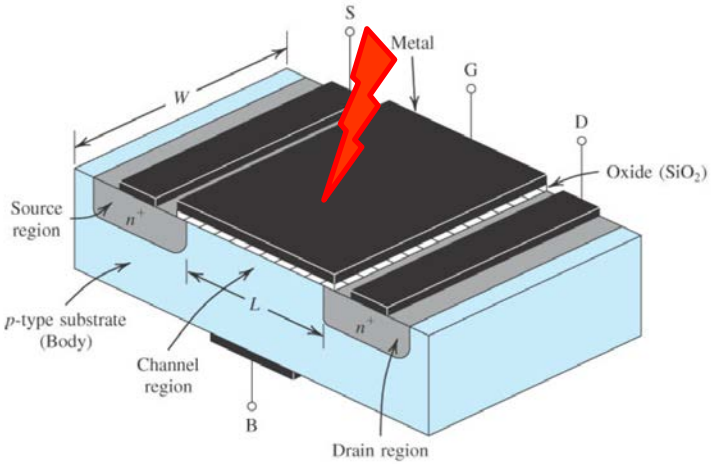
error mitigation by redundancy !

TID: < .2 Gy/year
$<10^{10}$ p/cm^2/year

Irradiation of samples

TID

- photons:
  - ^{60}Co
  - X-ray tubes
- protons



SEE

protons (E > 20 MeV)
neutrons (E > 20 MeV)
heavy ions

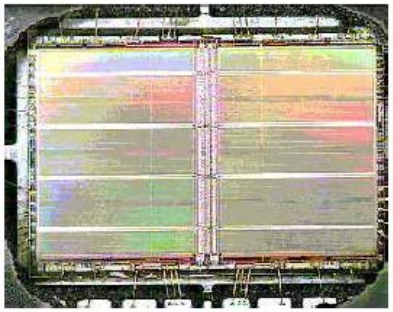
protons can be used to study both **TID** and **SEE**

TID Co-60 Testing
- No device preparation required

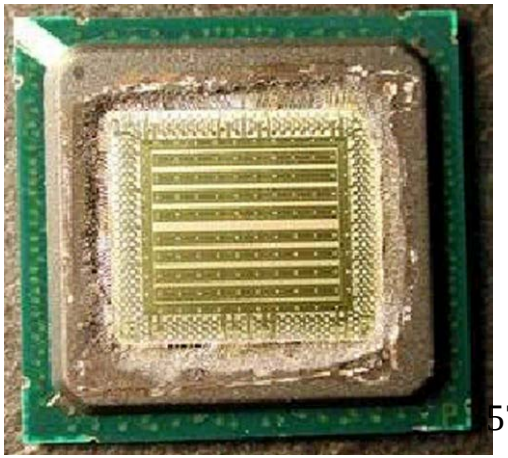
Displacement damage and SEE Proton Testing
- No device preparation required

SEE Heavy ion Testing
- Device preparation required

de-lidding



delidded Virtex-II

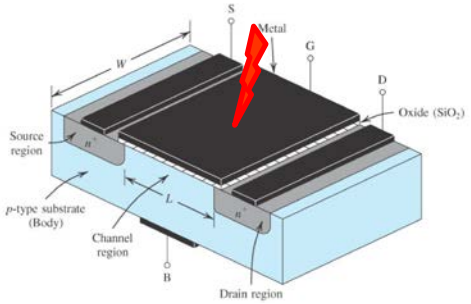


Irradiation facilities in Europe

Several European Accelerator Facilities have ions and proton energies suitable for SEE testing:

- Proton Irradiation Facility (**PIF**) at the Paul Scherrer Institut (PSI), Villigen, Switzerland (used since 1992)
- Heavy Ion Irradiation Facility (**HIF**) at the University Catholique de Louvain (UCL), Louvain-la-Neuve, Belgium (used since 1996)
- RADiation Effects Facility (**RADEF**) at the University of Jyväskylä, Jyväskylä, Finland – (used since 2005)
- Cyclotron-based fast neutron facility at NPI Rez (Prague):
  - **Φ**: 10^{11} n/cm^2 s up to 32 MeV
- The Svedberg Laboratory proton beam facility (Uppsala):
  - **Φ**: 10^{11}-10^{12} p/cm^2 s from 20 up to 180 MeV

Irradiation facilities in Italy



Legnaro (SIRAD):

- ion species from ^{1}H (22-30 MeV) up to ^{197}Au (1.4 MeV/a.m.u.)
- LET from 0.02 MeV×cm^2/mg (^{1}H) up to 81.7 MeV×cm^2/mg (^{197}Au)
- high **Φ** (>10^8-10^9 ions/cm^2 s) or low **Φ** (>10^2-10^6 ions/cm^2 s) irradiation
- neutrons (0-24 MeV)
- **TID**: X-rays @ 120 rad(Si)/s, γ-rays @ 1-5 rad(Si)/s with Co-60

TANDEM accelerator

CN accelerator

Catania (LNS): 20 MeV/n heavy ions for **SEE**
60 MeV protons for **DD**

Pavia (CNAO): 250 MeV protons and 480 MeV carbon ions

Trento (TIFPA): 60-200 MeV protons for **TID** + **SEE**

…

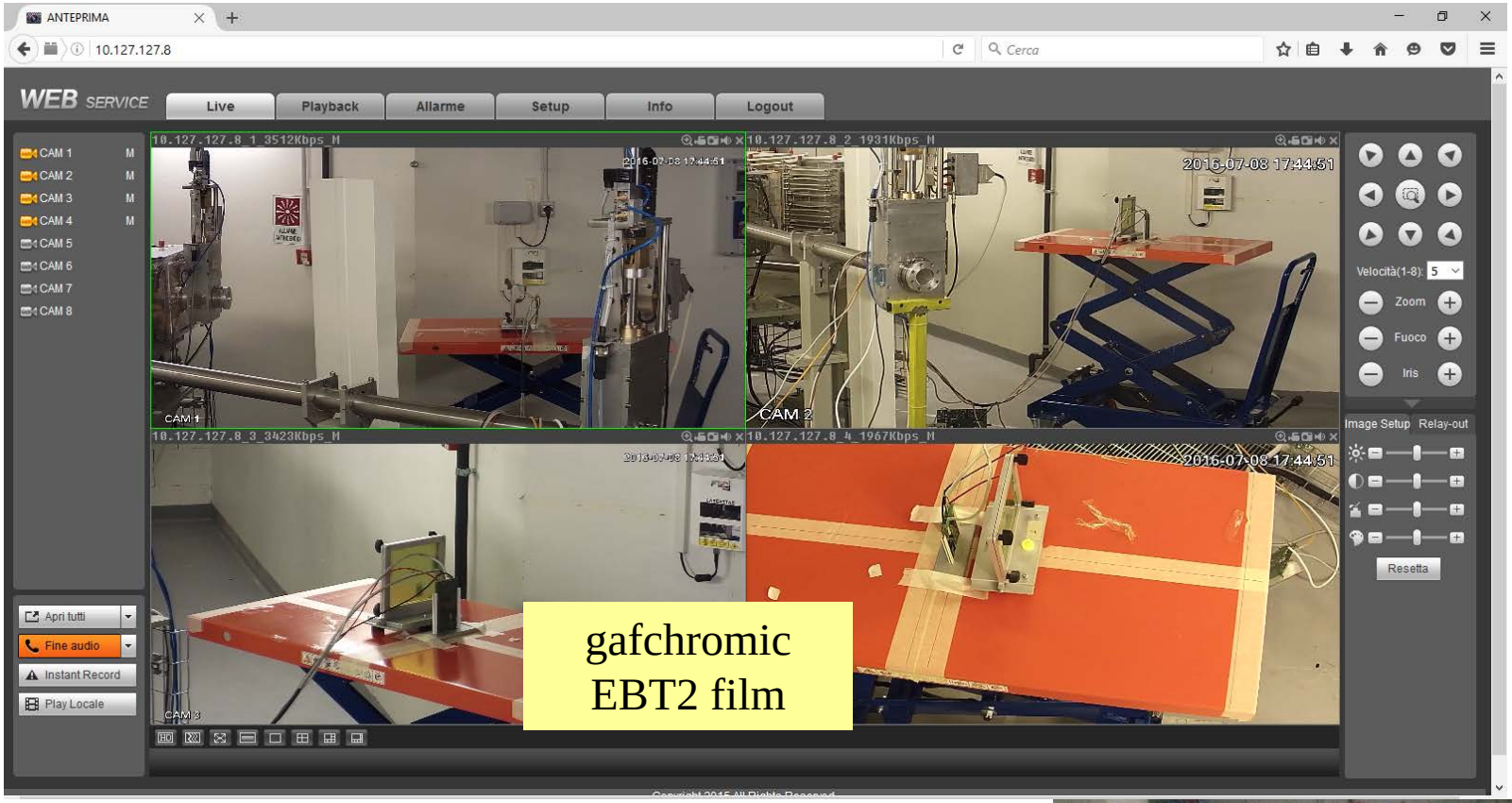
Proton therapy Center (Trento)

- New irradiation facility developed jointly by **INFN TIFPA** and Trento proton therapy center
- 60-200 MeV proton beam (Φ = O(10^7-10^9 p/(cm^2 s))
- proton beam spot with r∼1 cm (σ = 3.4 mm)

One cyclotron line is devoted to researchers with the following time slots:

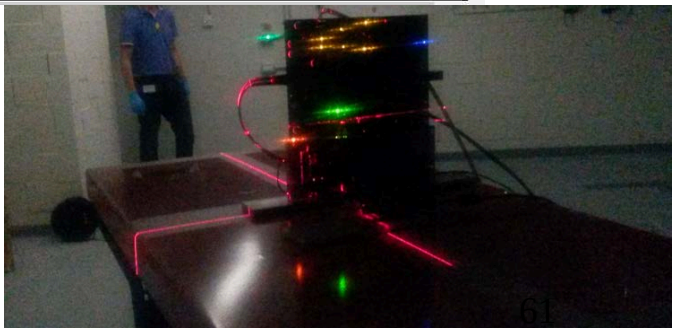
- MON-FRI: h 18-22
- SAT: h 8-14

Proton therapy Center for COTS qualification

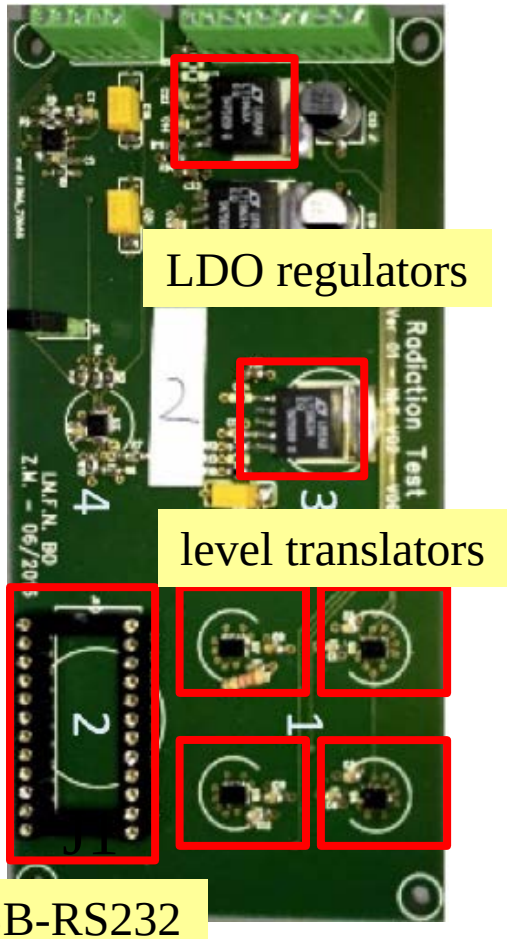


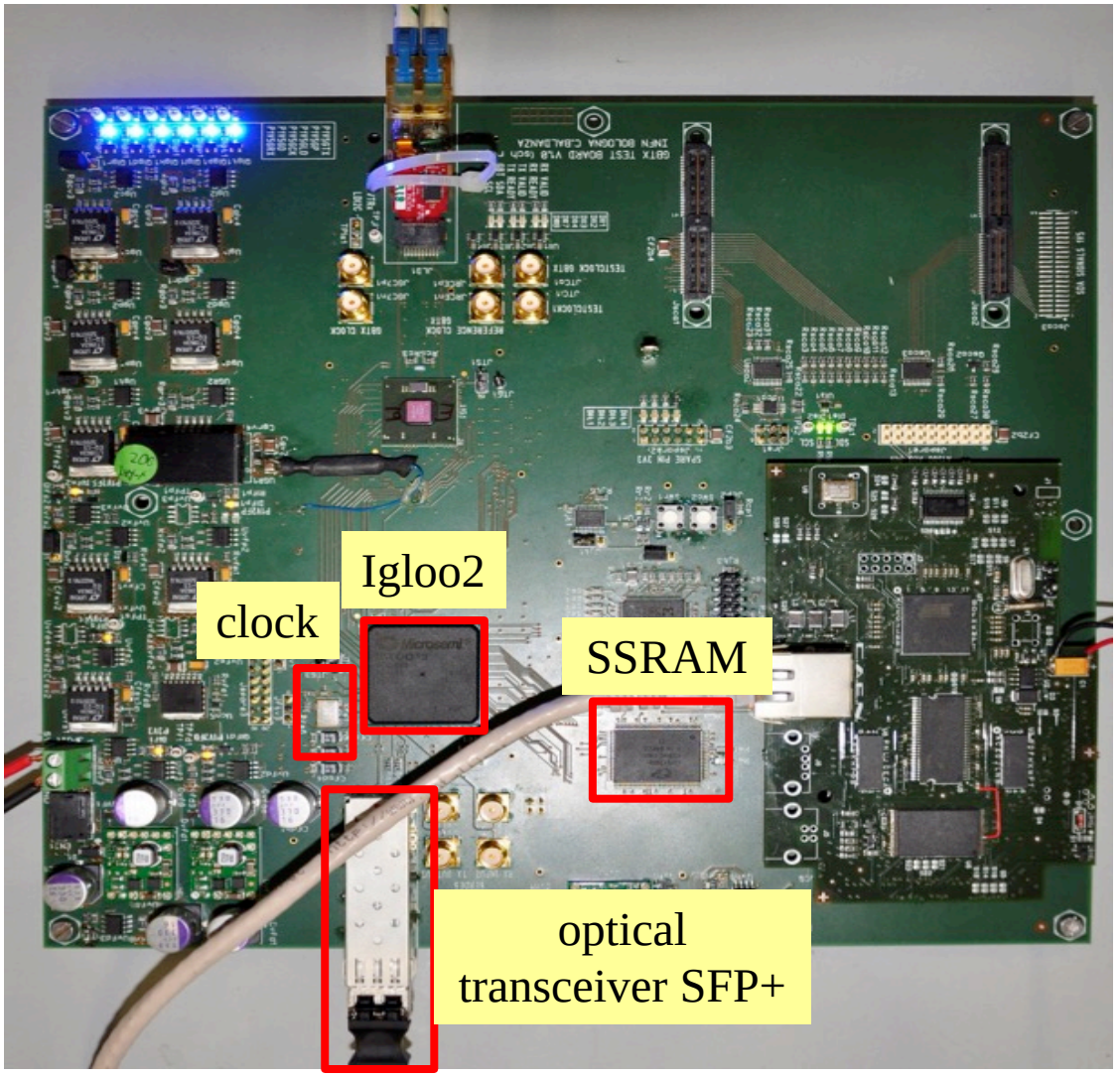
Our choice:

- 200 MeV proton beam (Φ = O(10^7-10^9 p/(cm^2 s))
- proton beam spot with r~1 cm (s = 3.4 mm)



Proton therapy Center (Trento): tested devices

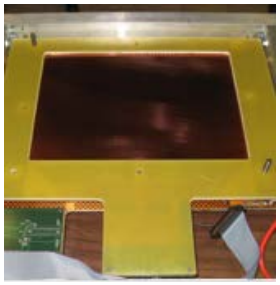




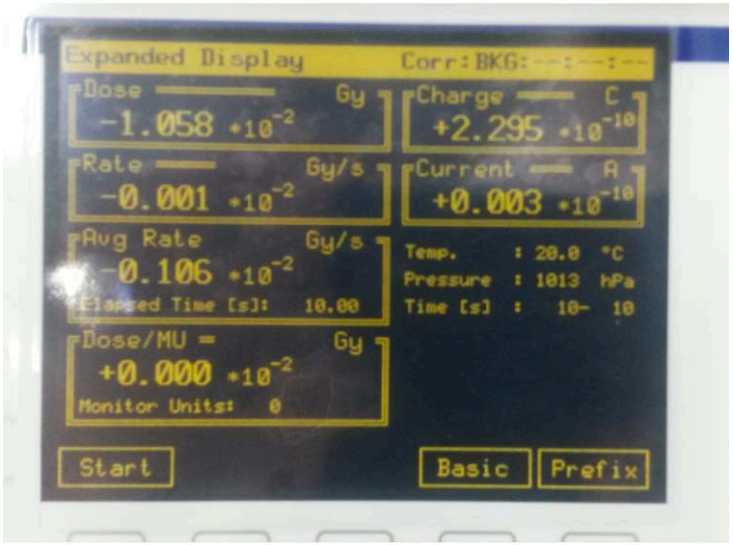
Target **TID**: 0.13 Krads, tested up to **1.3 Krads** (10x security factor)

Irradiation tests @ Trento

Faraday's cup



strip chamber



1 nA	→ 2.273E-10 C/10 s	→ 4.34 10^7 p/(cm^{2}s)
2 nA	→ 4.970E-10 C/10 s	→ 9.50 10^7 p/(cm^{2}s)
5 nA	→ 1.278E-9 C/10 s	→ 2.44 10^8 p/(cm^{2}s)
10 nA	→ 2.7E-9 C/10 s	→ 5.1 10^8 p/(cm^{2}s)

Φ → dose with Faccio's table

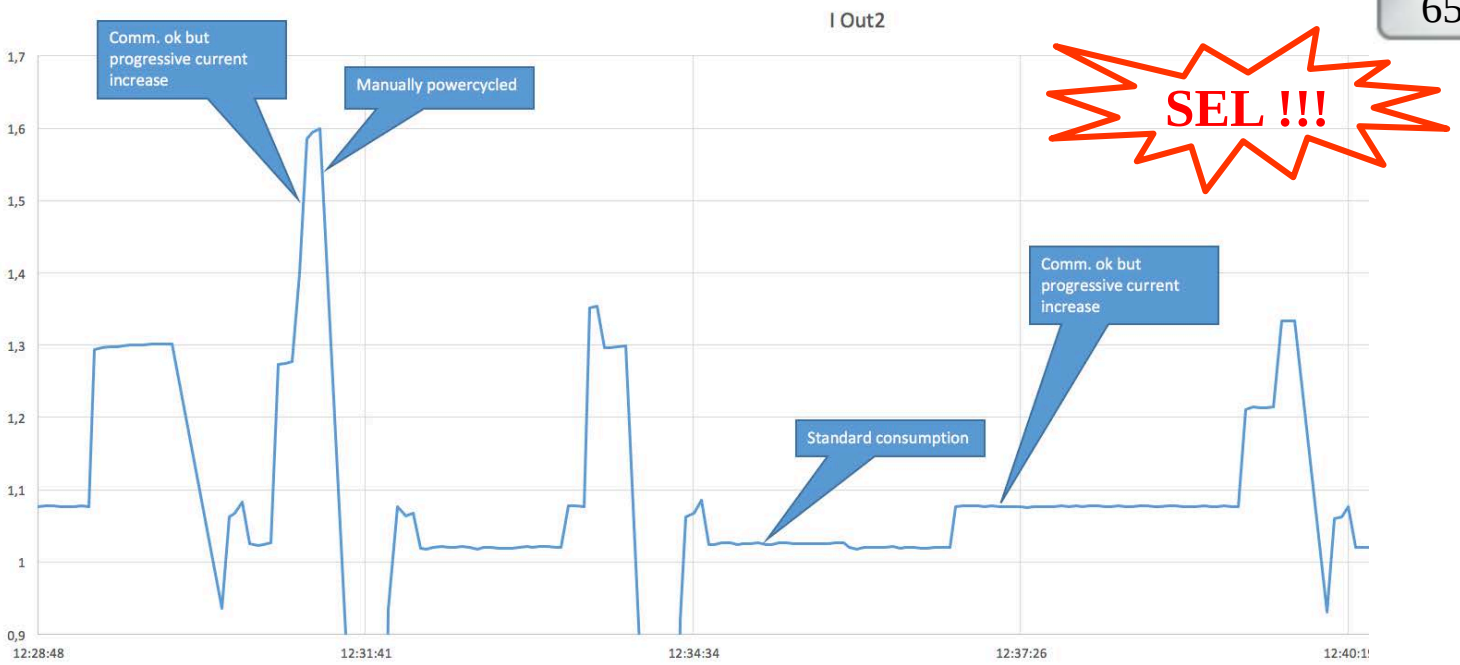
Results:

- **TID:**
  - ✓ USB-RS232 adapter, clock, level translators and low drop regulators: OK!
  - ✓ IGLOO2 reprogrammed successfully after **1.3 krads**
  - ✗ Optical transceivers (**Finisar**) failed after few krads → we then tested **Avago** SFP+ with much better performances (no SEL)
- **SEE:**
- ✓ IGLOO2 BRAM σ_{SEU} registered (??? due to SEL …)
- ✓ **SSRAM σ_{SEU}: 1.2 10^{-15}/(cm^2 bit) (no SEL)**

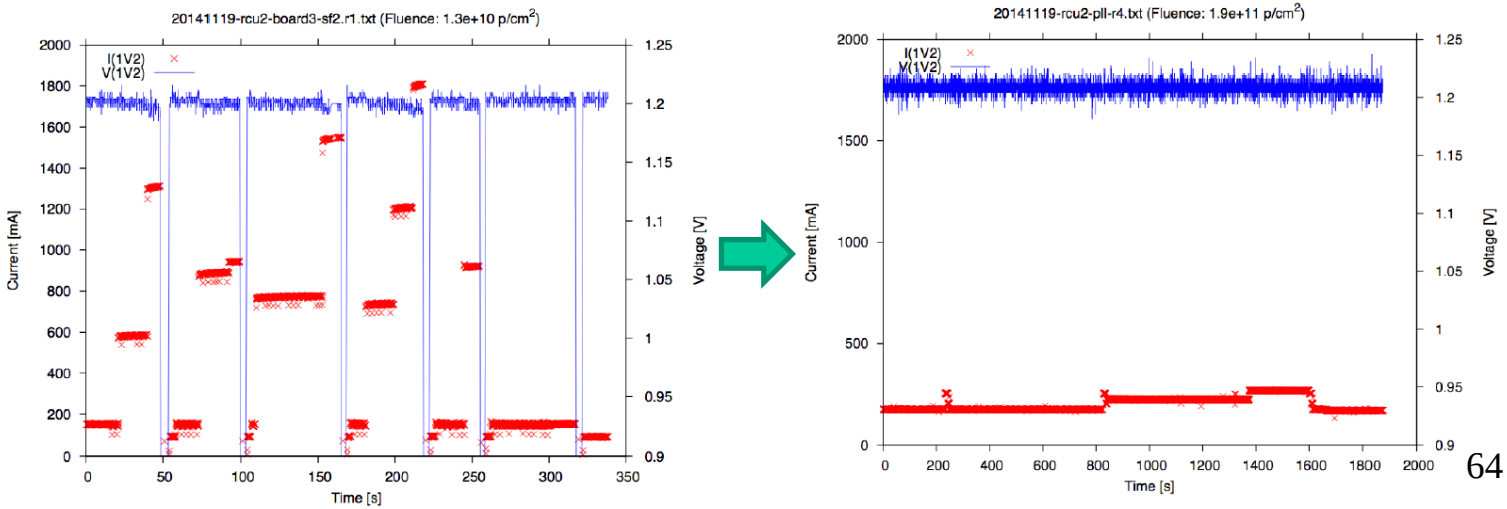
Proton therapy Center (Trento): testing Igloo2

Microsemi Power Matters.
IGLOO 2 FPGA
65 nm

our tests



literature results from Uppsala (found later!)



CHARM @ CERN
(Cern High Energy AcceleRator Mixed-Field Facility)

Main purpose

Radiation tests of electronic equipment and components in a radiation environment similar to the one of the accelerator

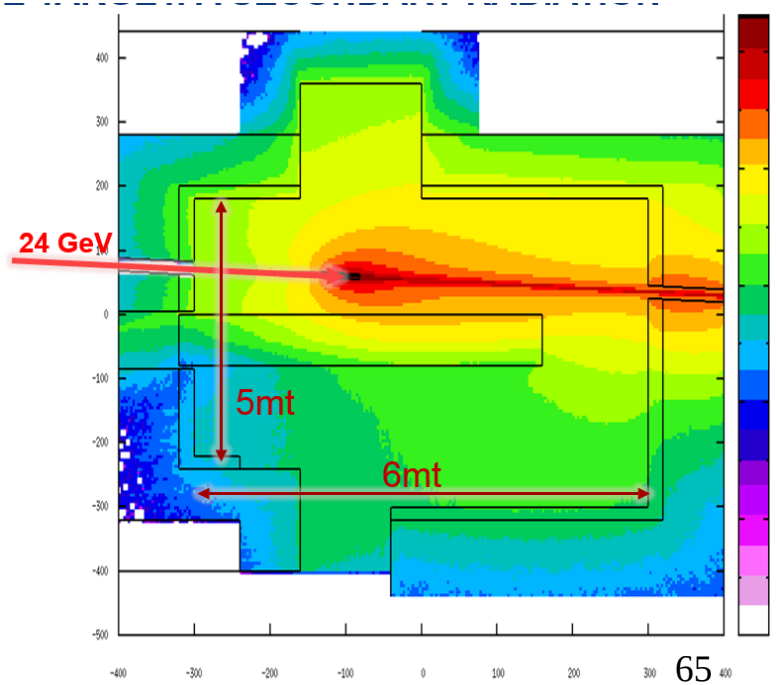
Large dimension of the irradiation room

- large volumes electronic equipment
- high number of single components
- full systems

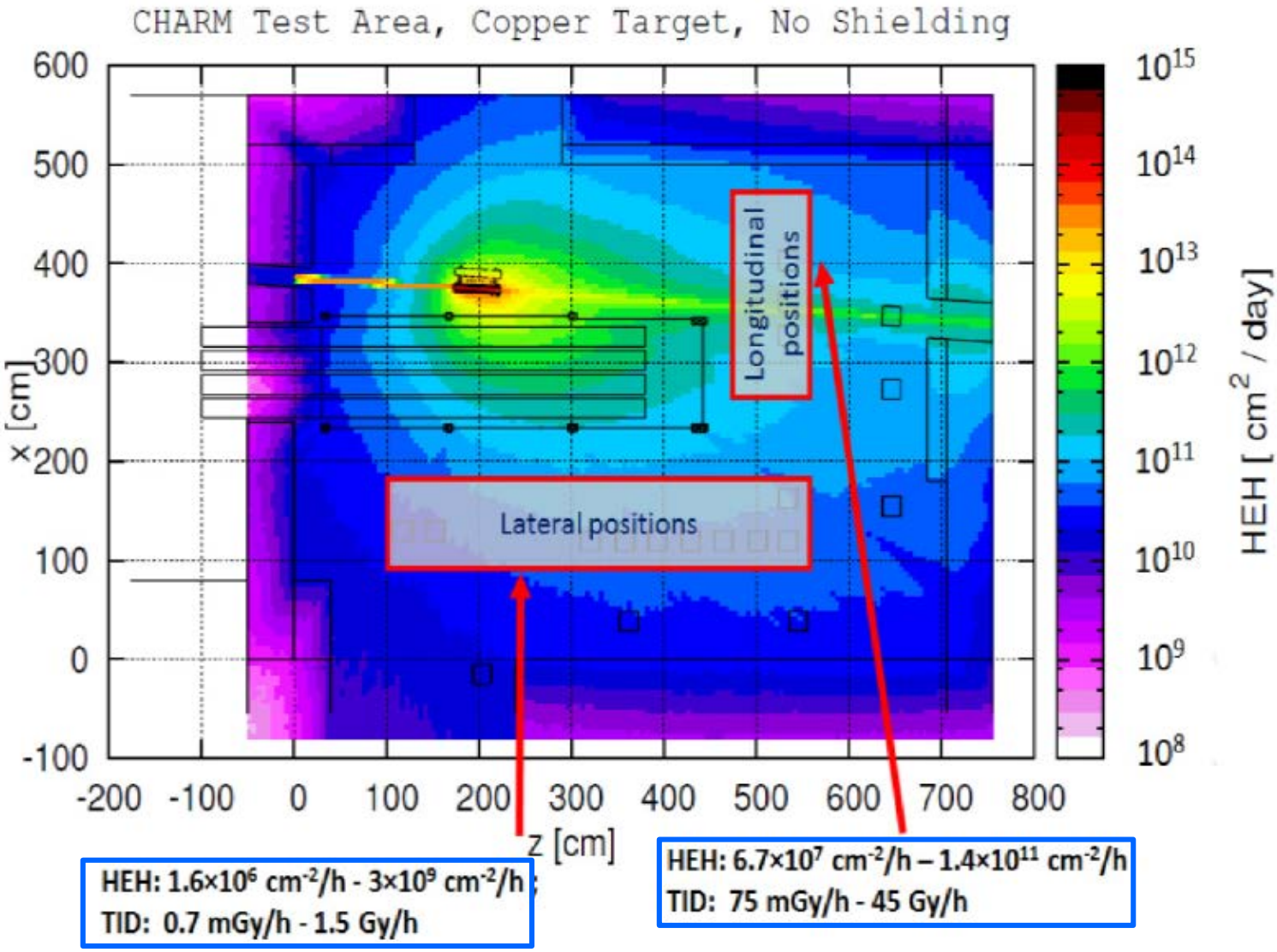
Numerous representative radiation fields

- Mixed-Particle-Energy: Tunnel and Shielded areas, atmospheric and space environments
- direct beam exposure (proton beam 24 GeV)

Primary protons impinge the target (concrete, iron): a secondary field is created



CHARM @ CERN


CHARM Test Area, Copper Target, No Shielding
600
500
400
300
200
100
0
-100
x [cm]
-200 -100 0 100 200 300 400 500 600 700 800
z [cm]
Longitudinal positions
Lateral positions
10^{15}
10^{14}
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
HEH [cm^2 / day]
HEH: 1.6×10^6 cm^{-2}/h - 3×10^9 cm^{-2}/h
TID: 0.7 mGy/h - 1.5 Gy/h
HEH: 6.7×10^7 cm^{-2}/h – 1.4×10^{11} cm^{-2}/h
TID: 75 mGy/h - 45 Gy/h

Where to get info on rad-tol devices

From **Tullio Grassi**:
https://twiki.cern.ch/twiki/bin/viewauth/FPGARadTol/InformationOfInterest

RADWG: Radiation Working Group (RadWG)
http://radwg.web.cern.ch/RadWG/Pages/info.aspx

ATLAS radiation hard electronics
http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm#Database

TWEPP
Microelectronics WG + FPGA working group

Radiation conferences

NSREC (Nuclear and Space Radiation Effects Conference)
RADECS (RADiation and its Effects on Components and Systems)

Conclusions

- Rad-tol devices are on the market, but they are way too expensive
- We need to qualify COTS components or design ASICs and test them

ASICs:

- modern silicon technologies are very robust against **TID**
- apply mitigation techniques
- choose a fab and keep using it!
- qualify samples at irradiation sites (protocol)!

FPGAs:

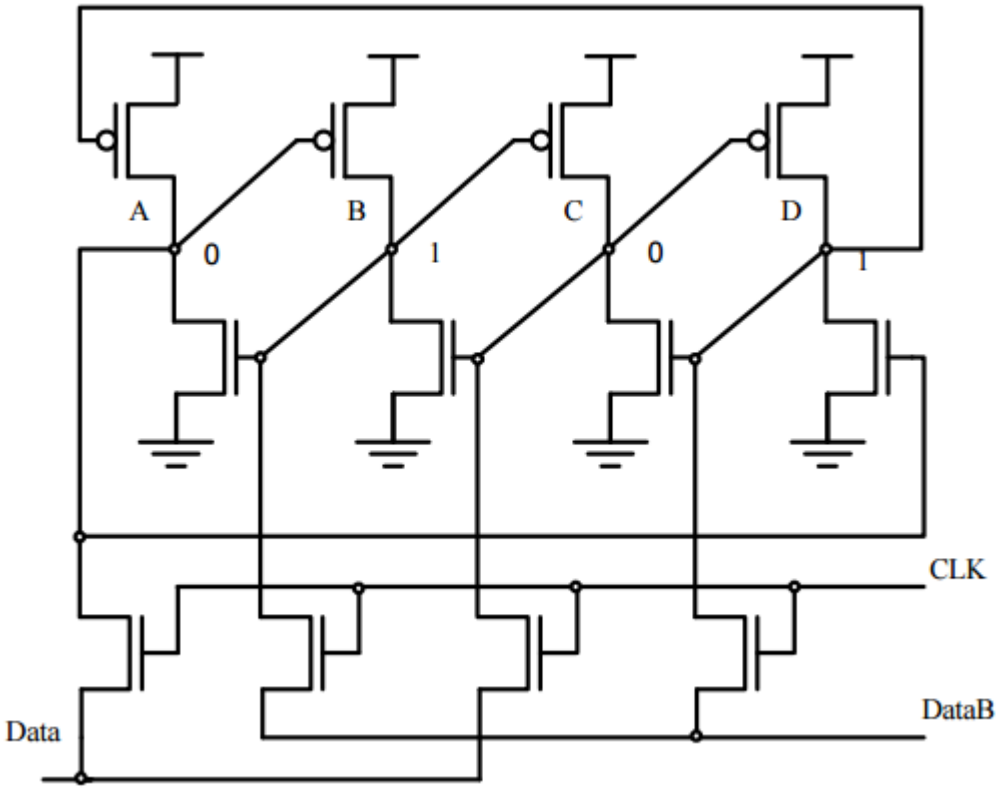
- **TID** < 20 Krads → use Flash-based devices
- **TID** > 20 Krads → use SRAM-based devices (implement scrubbing + TMR) or antifuse
- purchase samples from the same production lot!
- apply mitigation techniques
- qualify samples at irradiation sites (protocol)!

then

- qualify systems at irradiation sites (protocol)!

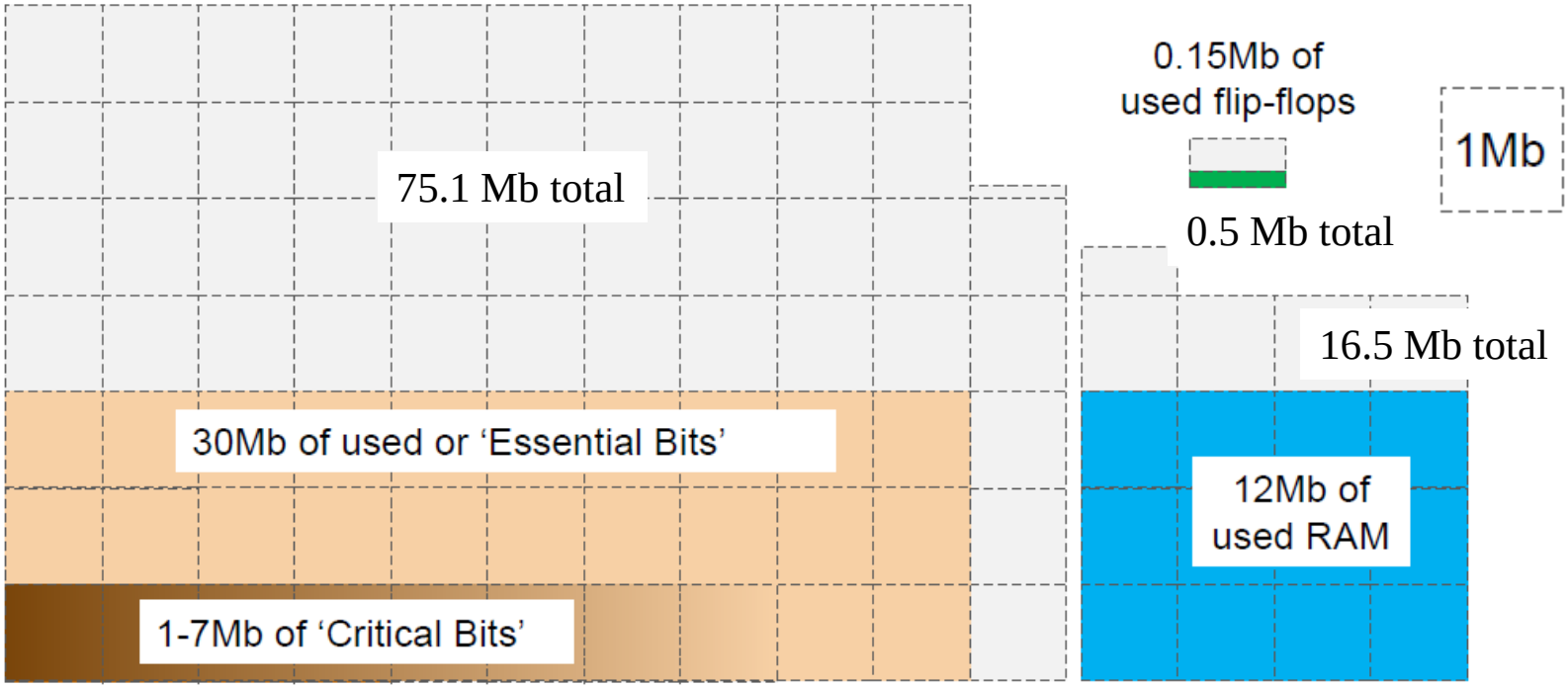
Backup slides

DICE storage cell



SRAM based FPGA configuration memory: scrubbing

An upset in any configuration bit does not create a soft functional error per se.
The bit has to be one that is critical to the function in order for a soft error to occur. The number of unused bits and non-critical bits reduces the soft error rate by what is known as the **device vulnerability factor (DVF)**.
The DVF for a typical design is 5% (one in 20 upsets, on average, cause a functional soft error.



Exploit **fault injection** to see how SEUs really affect your design !!!

FPGA vs ASIC use @ CERN

Accelerator

- In the accelerator sector the use of ASICs is very limited due to the high development time and resources needed
- **COTS FPGAs** are the primary choice

Experiments

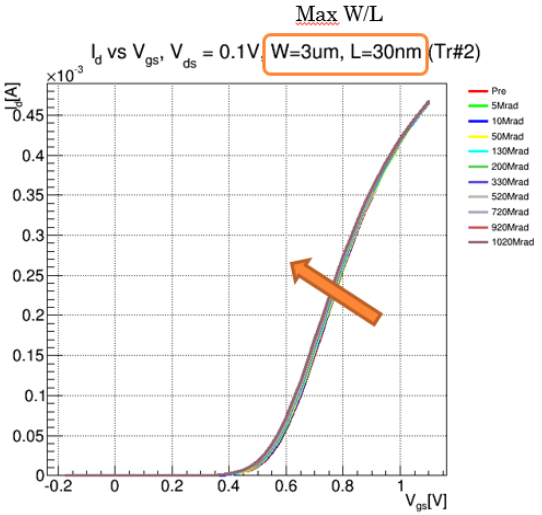
- In the experiments the high radiation levels close to the interaction points and the high performances required a custom ASIC development
- In environments with **low/medium radiation** and where power/integration issues are less critical **FPGAs are now an attractive alternative !!!**

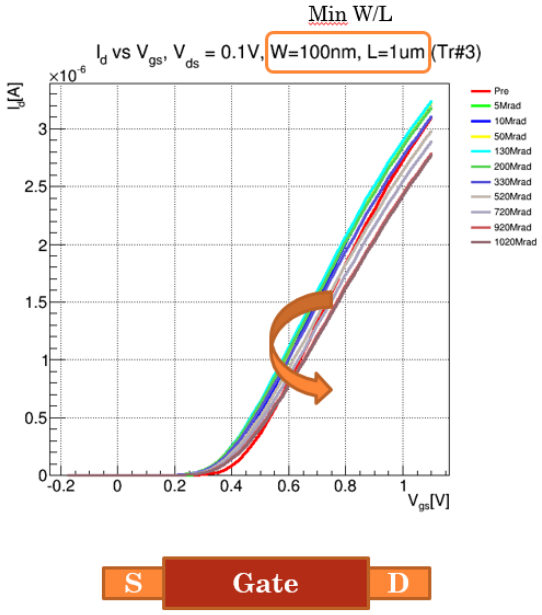
Benefits

- COTS: low cost (high volume required)
- low development costs
- re-programmable
- well developed & affordable platforms of tools

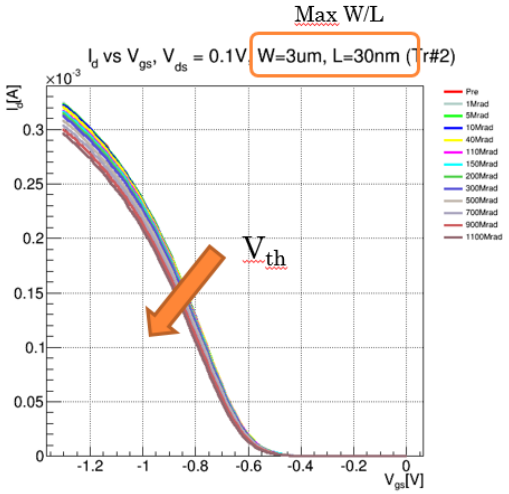
28 nm CMOS technology node (high-k instead of SiO_2)

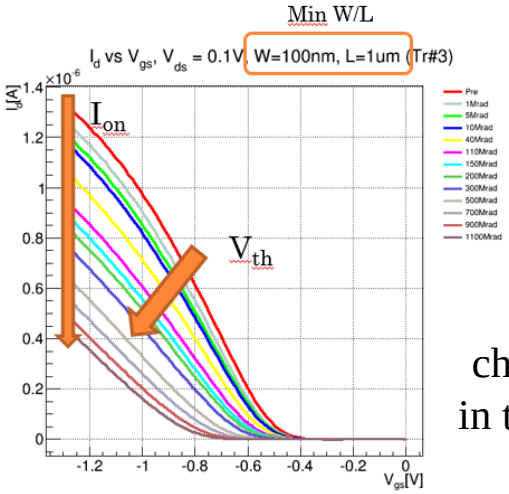
TID (X-ray facility in Padova, 8 Mrad/h)





NMOS



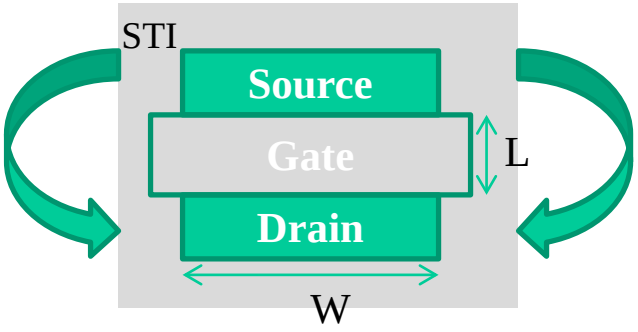


PMOS

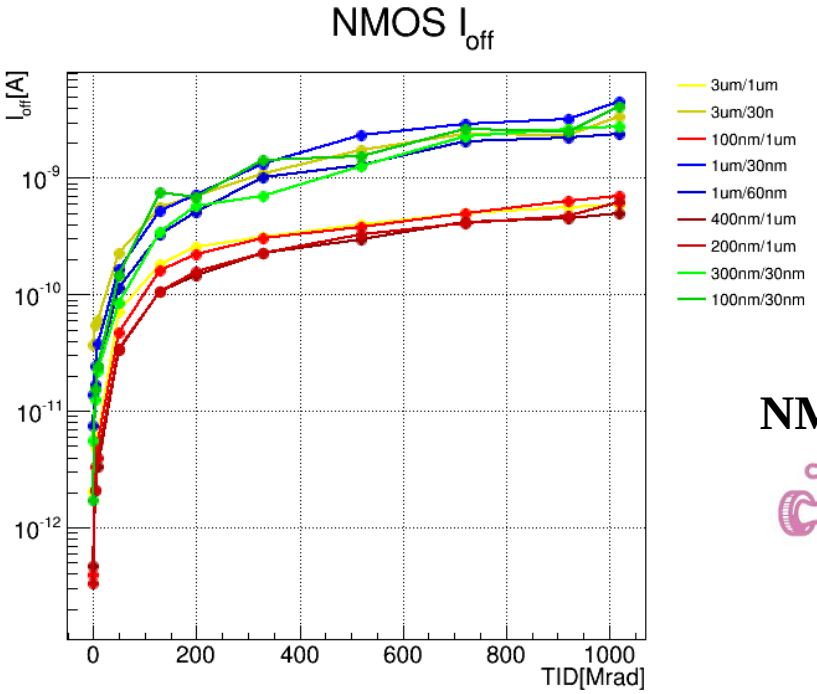
charge trapping in the STI oxides

28 nm CMOS technology node (high-k instead of SiO_2)

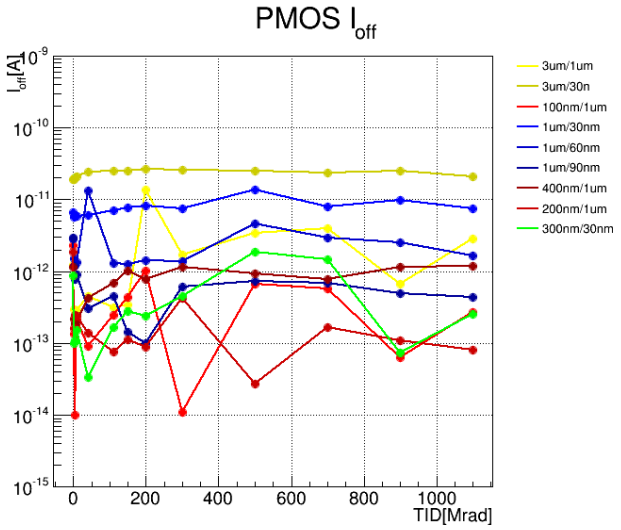
leakage current (I_d @ V_{gs} =0) increases between 2 and 3 orders of magnitude for NMOS



no increase in leakage current (pMOSFETs are not subject to sidewall leakage current)

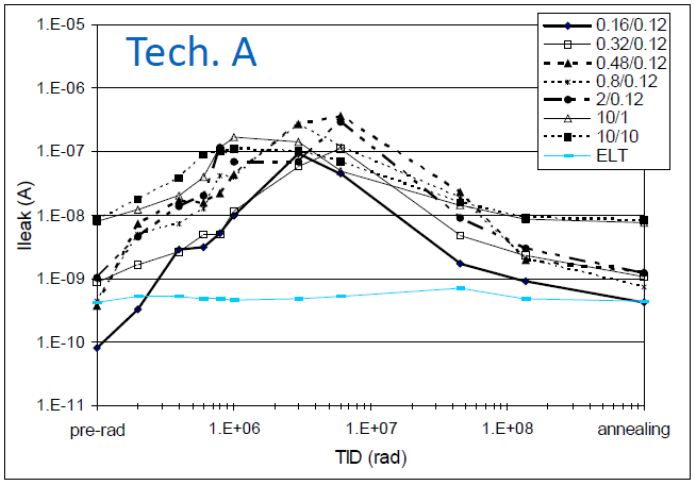


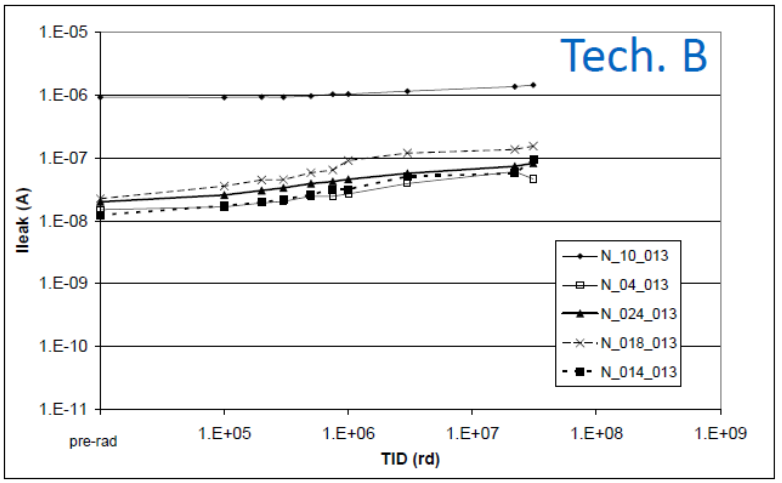
NMOS



PMOS

130 nm CMOS technology node





leakage paths are technology dependent

→ one technology fab has to be chosen

I/V curve of a Floating Gate device (Flash)

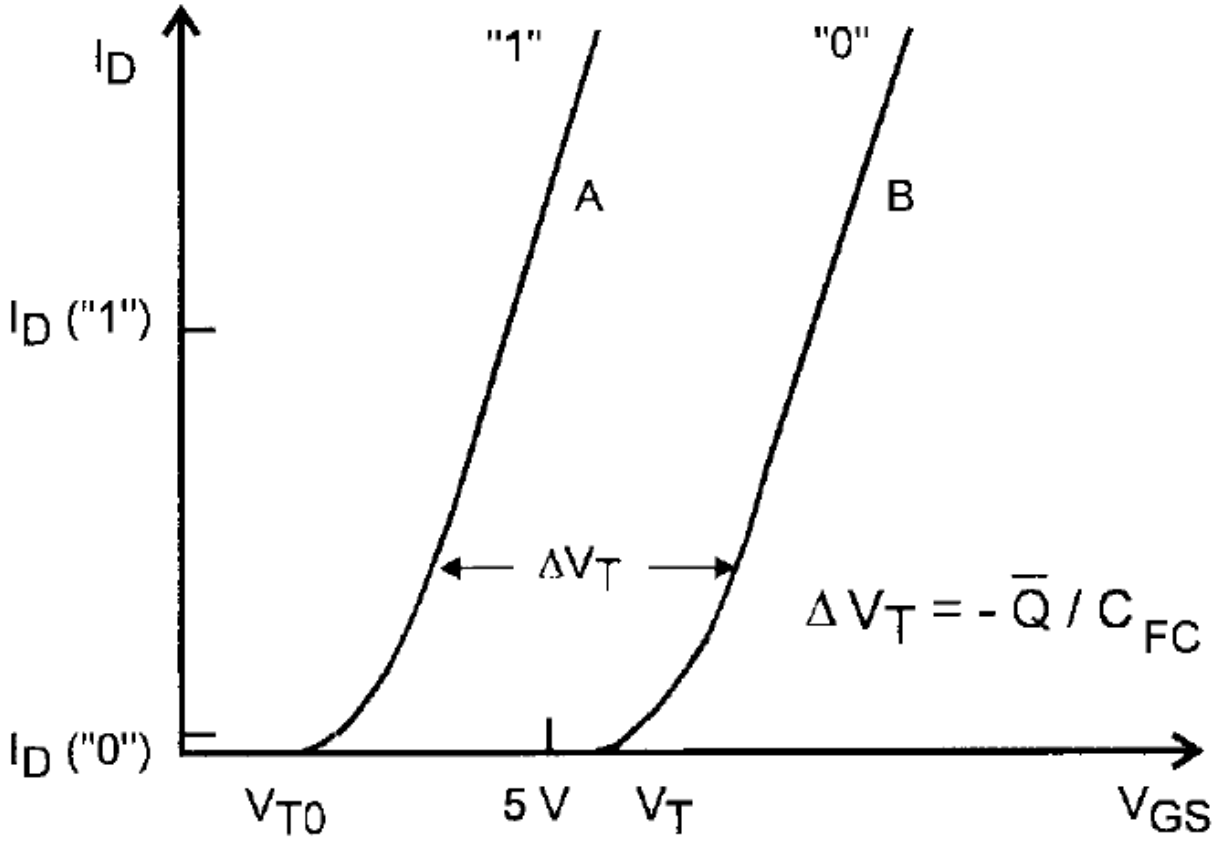
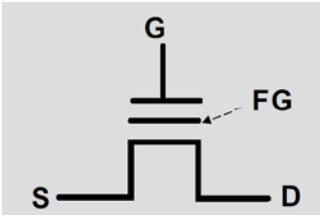


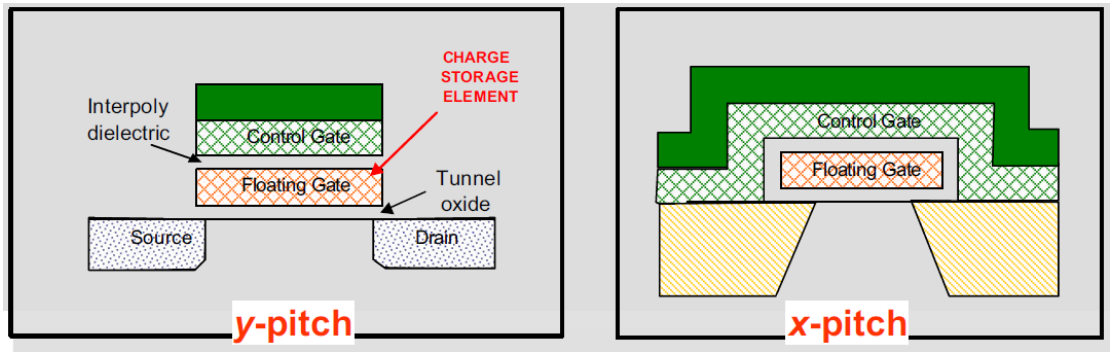
Fig. 4. I–V curves of an FG device when there is no charge stored in the FG (curve A) and when a negative charge $\bar{Q}$ is stored in the FG (curve B) [14].

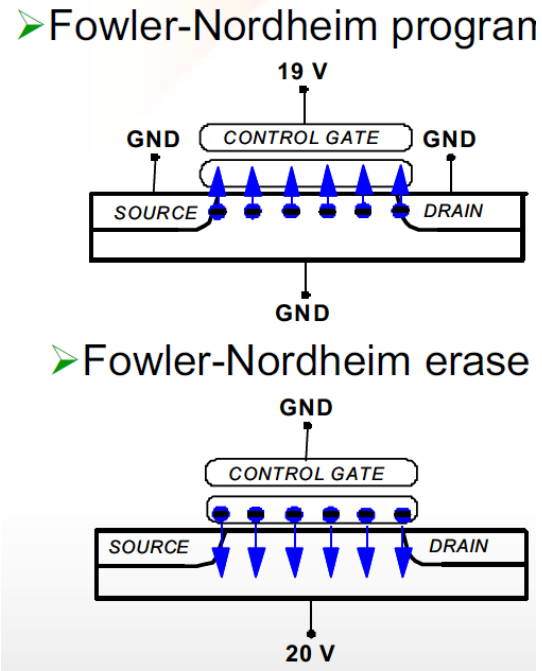
Flash: charge injection mechanisms



- Hot-electrons injection
- Fowler-Nordheim tunneling mechanism
  - high E through a thin oxide

With a relatively thick oxide (20–30 nm) one must apply a high voltage (20–30 V) to have an appreciable tunnel current. With thin oxides, the same current can be obtained by applying a much lower voltage. An optimum thickness (about 10 nm) is chosen in present devices, which use the tunneling phenomenon to trade off between **performance constraints** (programming speed, power consumption, etc.), which would require thin oxides, and **reliability concerns**, which would require thick oxides.





Microsemi SmartFusion®2 SoC FPGA 65 nm

Microsemi IGLOO®2 FPGA 65 nm

SRAM bits scrambling

A0	A1	A2	A3	A4	A5	A6	A7
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	C2	C3	C4	C5	C6	C7
D0	D1	D2	D3	D4	D5	D6	D7
E0	E1	E2	E3	E4	E5	E6	E7
F0	F1	F2	F3	F4	F5	F6	F7
G0	G1	G2	G3	G4	G5	G6	G7
H0	H1	H2	H3	H4	H5	H6	H7

A single radiation event can cause a multiple-bit upset (MBU).
If the SRAM bits in a logical word are physically adjacent, the MBU can result in uncorrectable errors.
For example, words D and E have *uncorrectable* multi-bit errors.

A0	A1	A2	A3	A4	A5	A6	A7
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	C2	C3	C4	C5	C6	C7
D0	D1	D2	D3	D4	D5	D6	D7
E0	E1	E2	E3	E4	E5	E6	E7
F0	F1	F2	F3	F4	F5	F6	F7
G0	G1	G2	G3	G4	G5	G6	G7
H0	H1	H2	H3	H4	H5	H6	H7

A0	B1	C2	D3	E4	F5	G6	H7
G7	H0	A1	B2	C3	D4	E5	F6
E6	F7	G0	H1	A2	B3	C4	D5
C5	D6	E7	F0	G1	H2	A3	B4
A4	B5	C6	D7	E0	F1	G2	H3
G3	H4	A5	B6	C7	D0	E1	F2
E2	F3	G4	H5	A6	B7	C0	D1
C1	D2	E3	F4	G5	H6	A7	B0

If the SRAM bits in each logical word are physically separated, the probability of the MBU resulting in uncorrectable errors is dramatically reduced.
For example, words D, E, F, and G have single-bit errors which are *correctable*.

A0	B1	C2	D3	E4	F5	G6	H7
G7	H0	A1	B2	C3	D4	E5	F6
E6	F7	G0	H1	A2	B3	C4	D5
C5	D6	E7	F0	G1	H2	A3	B4
A4	B5	C6	D7	E0	F1	G2	H3
G3	H4	A5	B6	C7	D0	E1	F2
E2	F3	G4	H5	A6	B7	C0	D1
C1	D2	E3	F4	G5	H6	A7	B0

SRAM as a SEU monitor

Design, Testing and Calibration of a "Reference SEU Monitor" System.

by

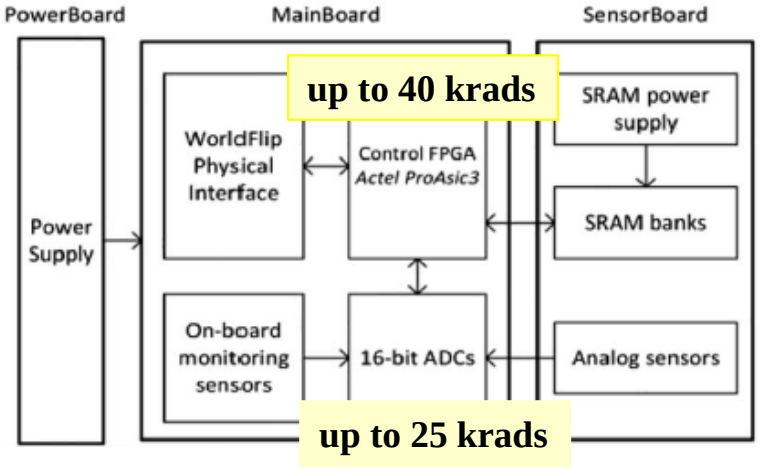
[1]R. Harboe-Sørensen, [2]F.-X. Guerre & [2]A. Roseng.

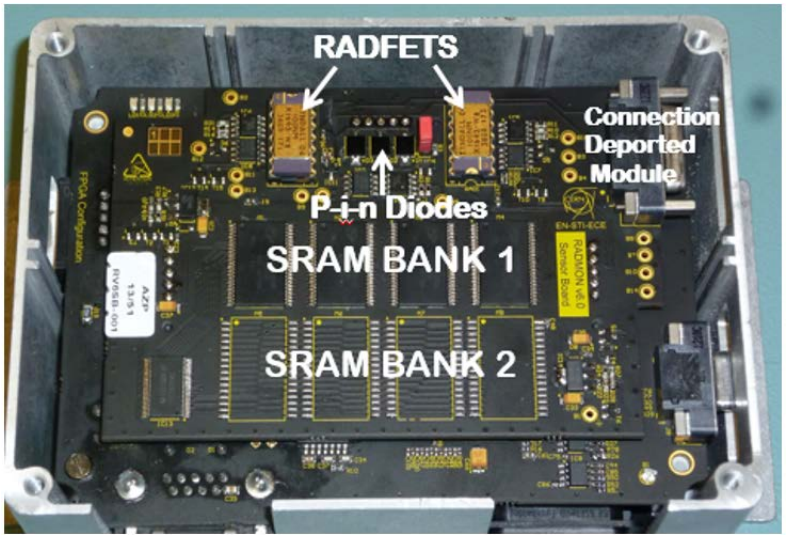
[1]European Space Agency/ESTEC - The Netherlands
[2]Hirex Engineering, Toulouse - France

Abstract

This presentation summarises steps taken by ESA in order to construct and calibrate a 'Reference SEU Monitor' system intended for use as a reference system at accelerators. Beam characteristics can be verified by experimenters via this simple system, which uses an SRAM as the detecting element and a laptop as the controller.

RadMon in the LHC tunnel

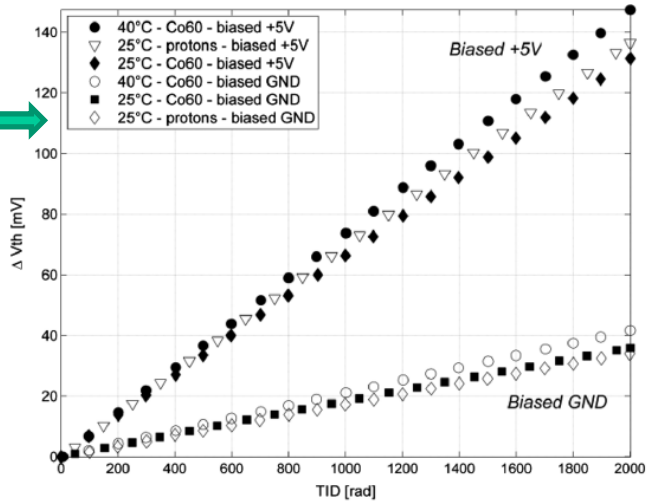


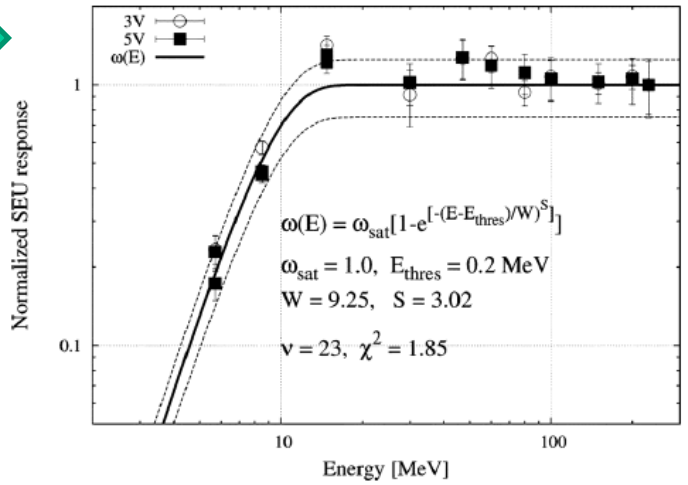


HEH and thermal neutron fluence with SRAM memories

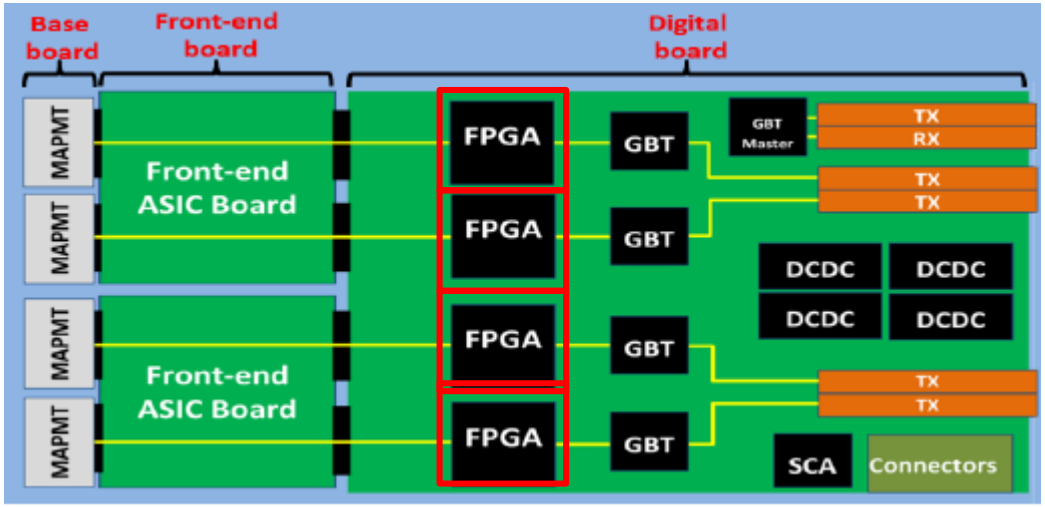
TID with RadFET

DD with PIN diode





Choosing SRAM-based FPGAs: LHCb RICH photodetectors



Region	TID [krad]	Neutrons: 1 MeV n_{eq} [cm^{-2}]	Hadrons: >20 MeV [cm^{-2}]
RICH1	200(30)	3×10^{12} (1.5×10^{12})	1.2×10^{12} (0.5×10^{12})
RICH2	80(22)	1.5×10^{12} (0.8×10^{12})	0.5×10^{12} (2.8×10^{11})

With such high TID values the only options are **SRAM-based or anti-fuse FPGAs**: currently a Kintex-7 being studied

Device Status Report

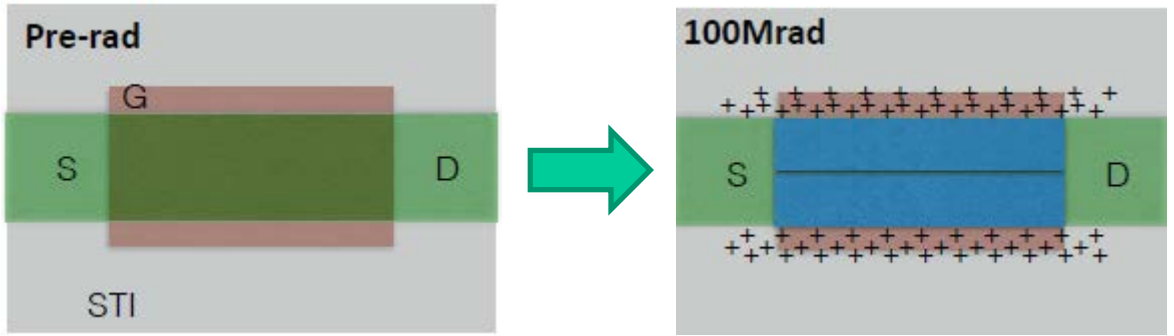
Device: M2GL090T (M2GL090T) Programmer: 86988 (usb86988)

```
Device Status:
        IDCode (read from the device) (HEX):        2F8071CF

        Device Certificate
                Family:                             Igloo2
                Die:                                M2GL090

        Design Information
                Design Name:                        DRM2_top
                Design checksum (HEX):              D43
                Design Version:                     0
                Back Level:                         0
                Operating voltage:                  1.2V
                Internal Oscillator:                50MHz

        Digest Information
                Fabric Digest (HEX):                24757afd3e69b38195ca8dd76a1ea54a
                                                    0000f78130fa81a379418ec7d7af14e4

                eNVM_0 Digest (HEX):                55b852781b9995a44c939b64e441ae27
                                                    24b96f99c8f4fb9a141cfc9842c4b0e3

                eNVM_1 Digest (HEX):                55b852781b9995a44c939b64e441ae27
                                                    24b96f99c8f4fb9a141cfc9842c4b0e3

        Device Security Settings
                Factory test mode access:           Allowed.
                Power on reset delay:               100ms
                System Controller Suspend Mode:     Disabled.

        Programming Information
                Cycle count:                        129
                VPP Range:                          HIGH ( VPP >= 3.3V )
                Temp Range:                         HOT

                *Algorithm Version:                 2
                * Programmer:                       FlashPro 4
                * Software Version:                 FlashPro v11.7
                * Programming Software:             FlashPro Express
                * Programming Interface Protocol:   JTAG
                * Programming File Type:            STAPL

NOTE: * - The above Information is only relevant if the device was programmed through JTAG or SPI Slave mode.
```

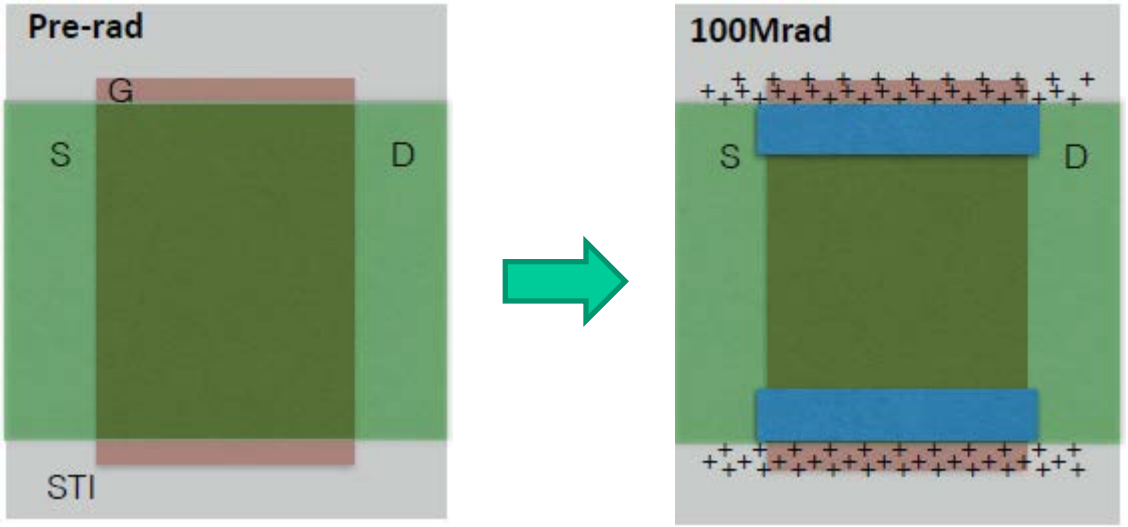
how many times the FPGA has already been programmed

130 nm CMOS technology node

min
size W



moderate
size W



avoid min size W !

RINCE (Radiation Induced Narrow Channel Effect)

There is also a similar effect on **RISCE** (Radiation Induced Short Channel Effect)

IMEC MPW calendar for 2017

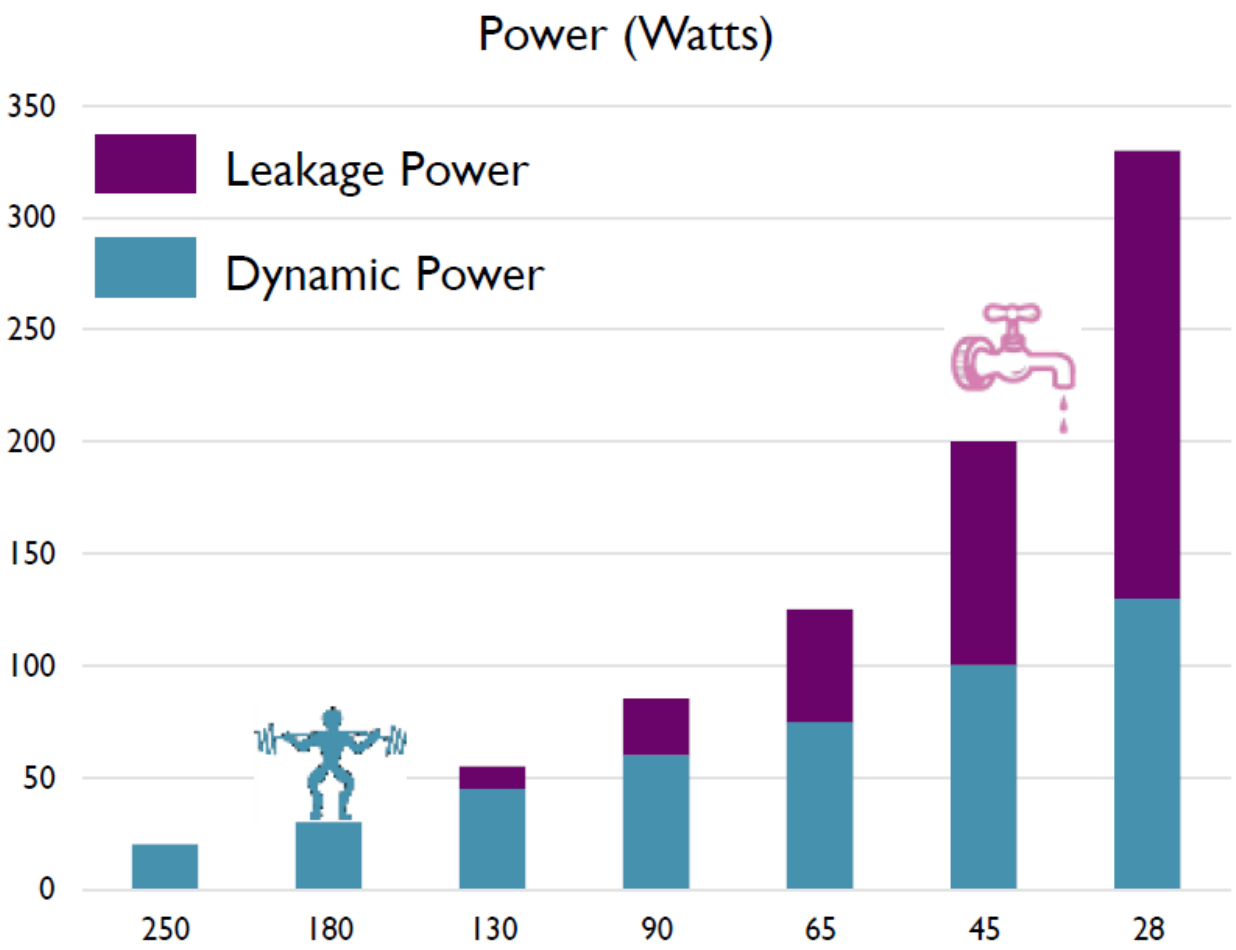
TSMC	J	F	M	A	M	J	J	A	S	O	N	D
TSMC 0.18 CMOS Logic or Mixed-Signal/RF, General	3,25	7,22	1,29	12,26	9,24	7,21	12,26	8,23	12,27	4,25, 31	22	5
TSMC 0.18 CMOS High Voltage BCD Gen Generation 2		7,22	1,29	12	3	7,22	27	31	5	5,16, 20	24	
TSMC 0.13 CMOS Logic or Mixed-Signal/RF, General or Low Power (8-inch)		7	14		9	14		9	14		9	
TSMC 0.13 CMOS Logic or Mixed-Signal/RF, General or Low Power (12-inch)				12		25			8			
TSMC 90nm CMOS Logic or Mixed-Signal/RF, General or Low Power			1	26		28		30			1	
TSMC 65nm CMOS Logic or Mixed-Signal/RF, General or Low Power	3	1,22		5,26	31	28		2,30		4,25	29	
TSMC 40nm CMOS Logic or Mixed-Signal/RF, General or Low Power (no triple gate oxide)	25	15	29	19	24	21	26	23	27	18	22	
TSMC 28nm CMOS Logic, HPL/HPM/HPC, RF HPL/HPC (reserve 4 months in advance)		1	1	5	3	7	5	9	6	11	8	13

Data in RED are preliminary scheduled

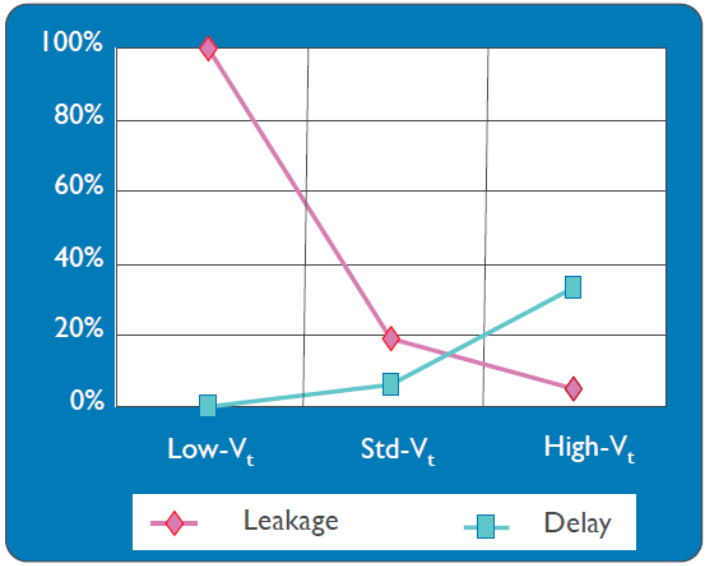
UMC	J	F	M	A	M	J	J	A	S	O	N	D
UMC L180 Logic GII/Mixed-Mode/RF	30		27			5	24			2		4
UMC L180 EFLASH Logic GII (1)			6				3				13	
UMC CIS180 Image Sensor 1P4M – CONV diode (1)			27							10		
UMC CIS180 Image Sensor 2P4M – ULTRA diode (1)			27							10		
UMC L130 Logic/ Mixed-Mode/RF			6			26					6	
UMC L110AE Logic/Mixed-Mode/RF	3	27		24		19		28		30		11
UMC L65N Logic/Mixed-Mode/RF - LL		6		3*	1	19*	31		18*	30		11
UMC L65N Logic/Mixed-Mode/RF - SP		6		3*	1	19*	31		18*	30		11
UMC 55N EFLASH EEPROM LP SPLIT GATE				3		19			18			11
UMC 40N Logic/Mixed-Mode – LP		6	27		1	26	31			2	20	
UMC 28N Logic/ Mixed-Mode – HPC (1)		21				12			11		27	

Other foundries are also available:

- ON Semiconductor (from 0.7µm to 0.18 µm)
- AMS (from 0.35 µm to 0.18 µm)
- IHP (from 0.25 µm to 0.13 µm)
- X-FAB (0.18 µm)


Power (Watts)
350
300
250
200
150
100
50
0
Leakage Power
Dynamic Power
250
180
130
90
65
45
28

USE MULTIPLE VT CELLS



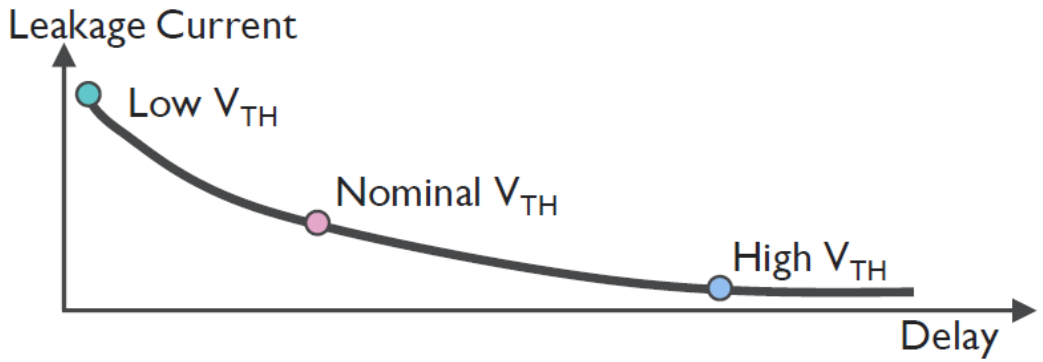
Multiple threshold technologies more common

Low V_t device = fast, high leakage

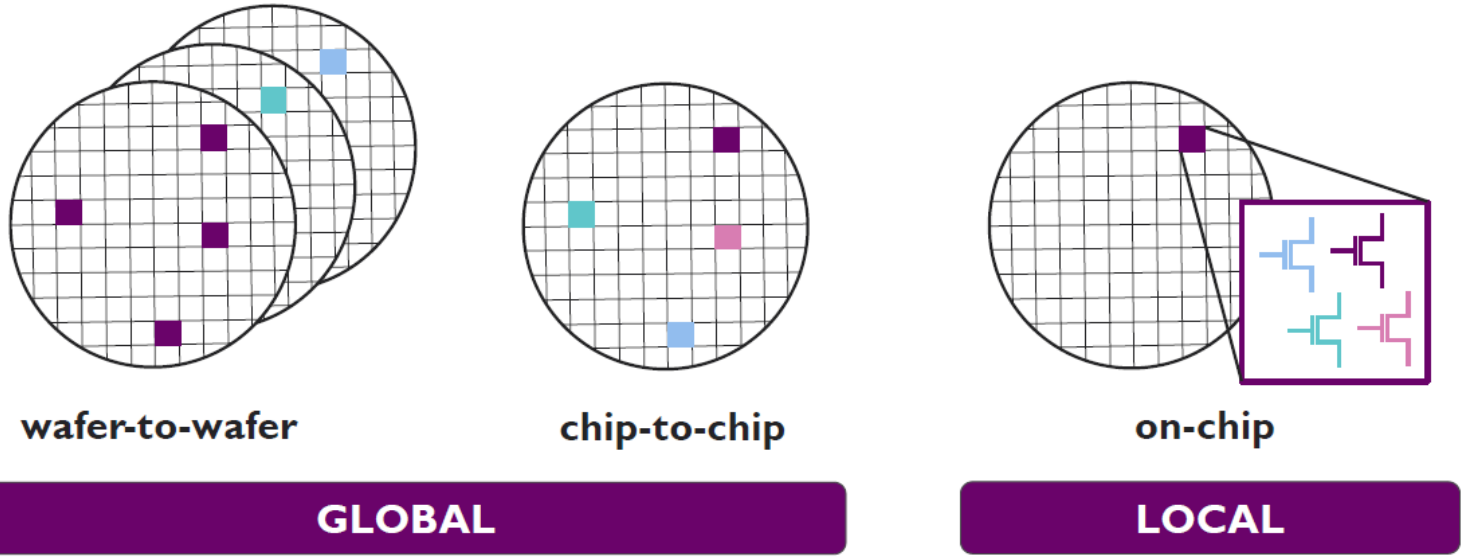
High V_t device = slow, low leakage

Achieves both active and standby leakage reduction

- Multi-V_t process reduces leakage power by an order of magnitude



VARIATION



INCREASE OF THE IMPACT OF THE VARIATIONS

	Tox (Å)	ΔTox (Å)	ΔTox/Tox	Lg (nm)	ΔL (nm)	ΔL/Lg
130nm	22	1	4.5%	130	5	3.1%
90nm	16	1	6.3%	90	5	5.6%
65nm	12	1	8.3%	65	5	7.7%

Lg (nm)	250	180	130	90	65	45
Vt (mV)	450	400	330	300	280	200
σ-Vt (mV)	21	23	27	28	30	32
(σ-Vt)/Vt	4.7%	5.8%	8.2%	9.3%	10.7%	16%

CHIPS (WAFERS & DIES)