

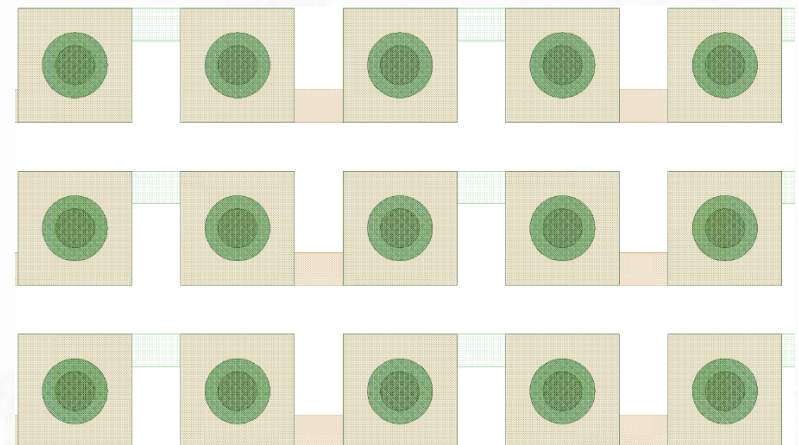
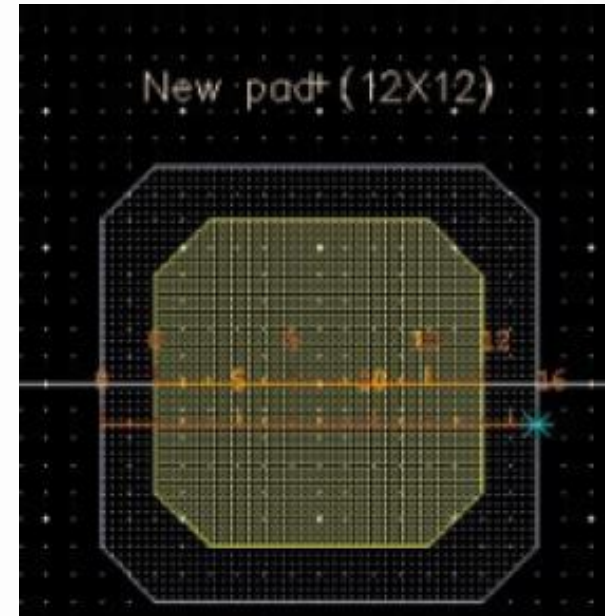
Pixel Module Summary

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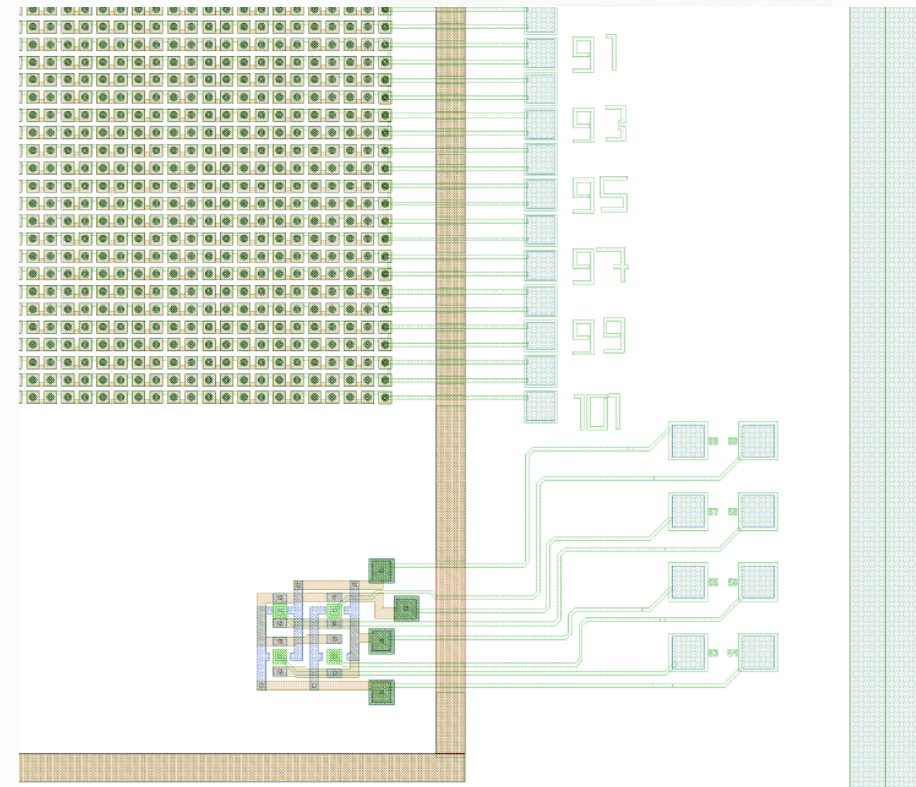


- Will not summarize the pixel module and sensor sessions from the last two days.
 - please go to the indico sites if you are interested in the details:
 - Modules: <https://indico.cern.ch/event/587242/>
 - Sensors: <https://indico.cern.ch/event/587234/> and <https://indico.cern.ch/event/587238/>
- Here I will raise a few issues which have not been discussed during this week but are probably important to a wider community:
 - Daisy chain program for bump bonding qualification
 - Pixel modules types and module sizes
 - Pixel sensor market survey prparations

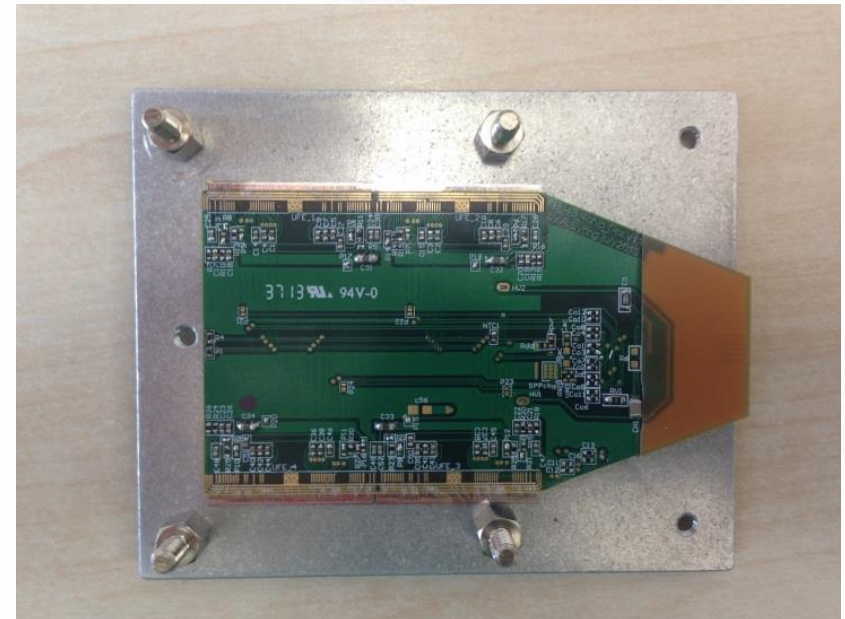
- For bump bonding qualification 300 mm dummy (daisy chain) wafer are useful for certain aspects:
 - bump deposition with bump density of 400 per mm^2
 - flip chip tests
- MPI (Anna, Julien) prepared a draft design with:
 - die size 2 cm x 2 cm with 400 x 400 pixel array of $50 \times 50 \mu\text{m}^2$ pixel size
 - metal layer, passivation layer and bump mask (UBM and/or bump deposition)
 - 35 μm square metal pads for “sensor” and 16 μm for “FE”, 12 μm passivation openings and 20 μm UBM/bump pads
 - daisy chains connects rows accessible from both sides



- Sensor and FE on the same 300mm wafer processed at IZM
 - only one mask set needed
 - about 100 dies per wafer
- 3 configurations possible:
 - only metal and passivation
 - metal, passivation and UBM (sputtered Ti/W + Cu)
 - metal, passivation, UBM and bump deposition (electroplated SnAg)
- ‘inofficial’ quotation from IZM:
 - masks + 10 wafers for metal & passivation: 20.000€ (~1.000 per additional wafer)
 - masks + 10 wafers including bumping: 28.000€ (~1.300 € per additional wafer)



- Currently we have 3 different module types in the different pixel layouts:
 - single chip modules, double-chip modules (like in IBL) and quad-modules (2 x 2 chips)
 - currently we're using the FE-I4 chip size (400 x 336 pixels of 50 μm x 50 μm) and the derived quad and double-chip module sizes for prototyping
- Most of the parameters of the modules are NOT defined by now:
 - final chip size \rightarrow constraint by several things like maximum data rate at minimal radius, die size etc.
 - modules sizes are intervened with local support and pixel layout
 - space between chips and modules and between modules on local support
 - Thicknesses of sensors and chips in the different layers \rightarrow there exist a large variety, connected to the costs and risks



- Started to prepare for the pixel sensor market survey:
 - up to now Anna, Sebastian, Richard, Fabian were involved
 - like to enlarge the group, i.e. Paolo, Steve (as PLs) plus some representative from the US and Japan
 - still discussing whether we should aim for a combined market survey with CMS
 - for strips this delayed considerable the progress and the timelines for CMS pixel are quite different
- Scope of the market survey:
 - only for the outer parts of the pixel system, i.e. this means just n-in-p planar pixel on 6'' or 8'' wafers
 - inner parts like 3D sensors or thin n-in-p or n-in-n planar are smaller orders and don't require a market survey
- Next steps:
 - plan for meeting of all contributors (November 24 perhaps) to agree on the next steps
 - start preparing the technical specifications - Anna agreed to coordinate this effort
 - get in contact with CMS colleagues to discuss the possibility of a combined market survey.