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NA62 FIRST LEVEL TRIGGER PROCESSOR

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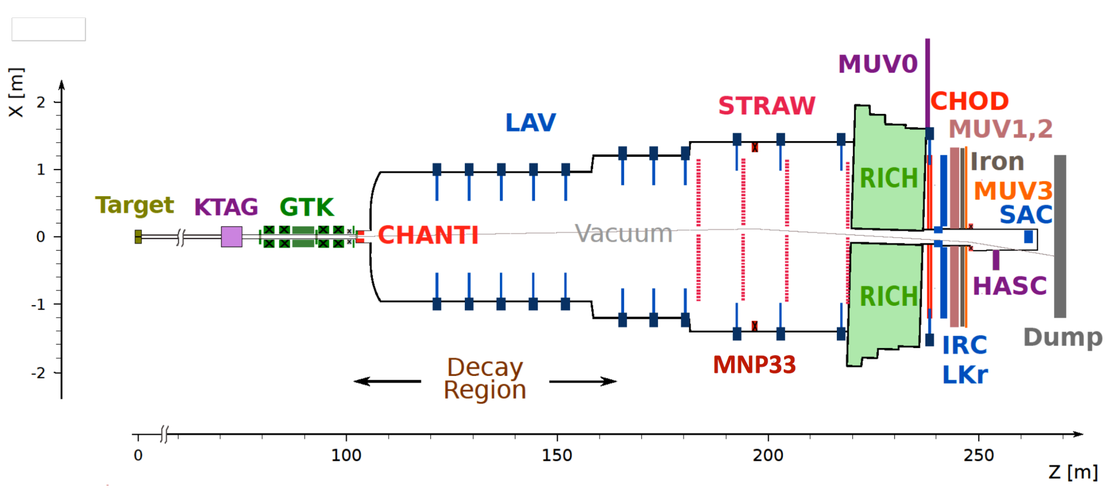
NA62: *High intensity beam*:
Central challenge for high rate experiments is the design of the trigger and data acquisition system simply to collect a sizable sample of the signal events.
The trigger system has therefore to guarantee a high acceptance for the signal events, keeping at the same time a high rejection of known decays accounting for most of the rate.



Main Goal : Measuring $K^+ \to \pi^+ \nu\bar{\nu}$ with 10% precision.
Statistics : 750 MHz intensity beam + large signal acceptance.
Systematics : Large background rejection + redundancy.

SM BR prediction: $(8.4 \pm 1.0) \times 10^{-11}$

Actual measurement: $(17.3 \pm 11.0) \times 10^{-11}$

Technique : High momentum kaon decay in flight.
Basic ingredients : Precise timing, kinematic cuts, accurate PID, vetoes.
Signal signature : One K^+ track, one π^+ track.

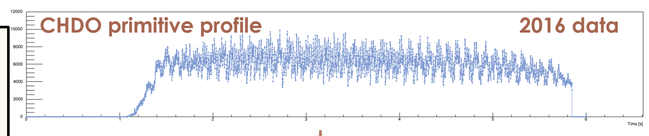
NA62 Trigger Levels:

- L0: Hardware synchronous level. 10 MHz to 1 MHz. Max latency: 1 ms.
- L1: Software level. "Single detector". 1 MHz to 100 kHz. Max latency: O(1 s).
- L2: Software level. "Complete information". 100 kHz to O(kHz). Max latency: spill period O(10 s) .

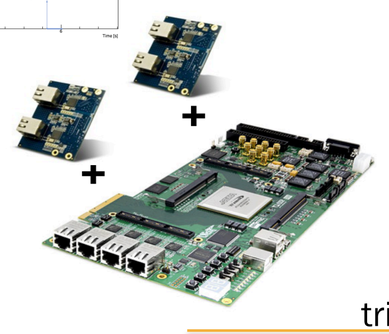
L0 Trigger Processor Features:

- Raw data (primitives) are sent in ethernet packets from detectors to L0TP via Ethernet using UDP protocol in frames of **6.4 us**.
- 10 MHz of input rate.
- L0TP realigns primitives in time.
- Compares them with pre-selected masks generating triggers @ 1 MHz.
- Triggers are sent to the TTC system after fixed latency up to 1 ms.
- Fully FPGA based.

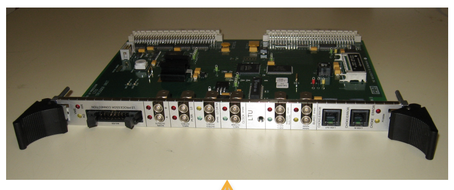
Primitives from
- RICH
- Charged Hodoscopes
- Calorimeters
- Large Angle Vetoes
- Muon Veto System



primitives

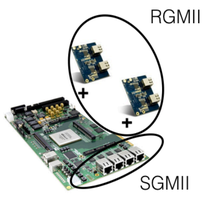


triggers



Logic Trigger Unit
- Receive trigger from the L0TP.
- Encode triggers.
- Transmit triggers via optical fiber to detectors.

1) Receiving UDPs with primitives



SGMII/RGMII interface: module developed by Ferrara for the GTK IO.

Frame decoding: GBE: 8 ns = 1 byte

Header
…Data…
End of packet (EOP)

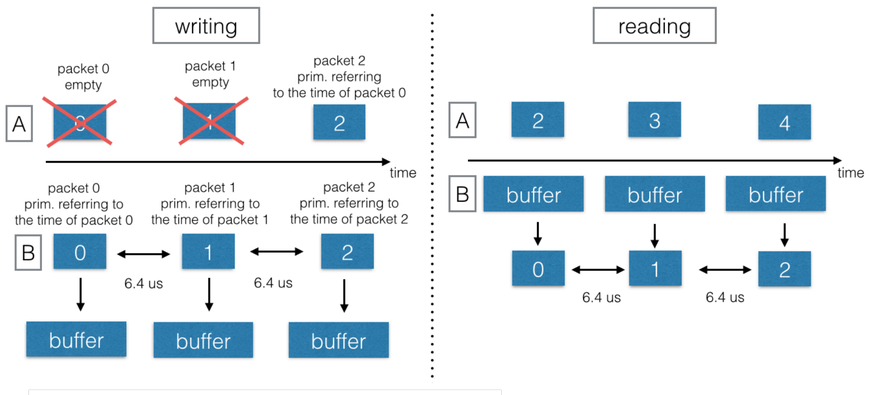
number of primitives in a packet

BUFFER (FIFO) with data delay generator

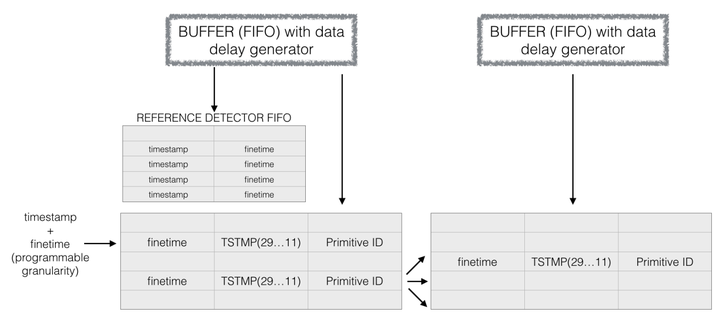
Count and reject packets

logic for alignment

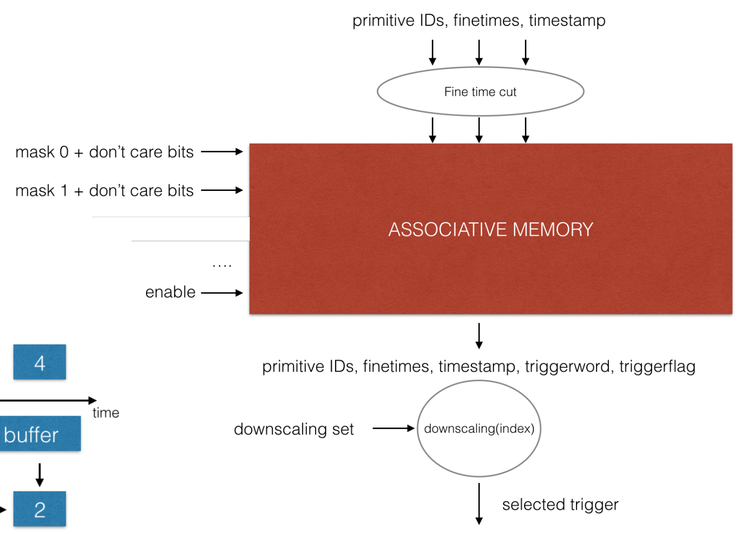
2) UDP realignment



3) Primitive realignment



4) Associative Memory



5) Output to detectors and PC-Farm