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Detector-embedded tracking using the RETINA algorithm

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The slowing down of Moore's law and the growing requirements of future HEP experiments with ever-increasing data rates pose important computational challenges for track reconstruction systems, encouraging the exploration of new methodologies. We propose that a significant benefit could come from making track reconstruction to happen transparently in specialized devices, as part of the detector readout ("detector-embedded tracking"), thus freeing computing resources for higher level tasks. With this long-term goal in mind, we have studied the potential of a track reconstruction approach based on a massively parallel pattern recognition algorithm, inspired by the processing of visual images by the natural brain ('RETINA algorithm'). This technique allows a large efficiency of utilization of the hardware, low power consumption and very low latencies, when implemented in state-of-art FPGA devices. Based on this methodology, a system has been proposed within the LHCb phase-II upgrade project to perform track reconstruction in the forward acceptance region in real-time. This innovative device will perform track reconstruction in parallel with the event-building process, in a short enough time to provide reconstructed tracks transparently to the processor farm, as if they had been generated directly by the detector. We describe the architecture of the system, bearing some resemblance to the Microsoft 'Catapult' system for cloud acceleration, and the performance measurements obtained from hardware prototypes developed in the past two years within the INFN RETINA project.

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