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Design and simulation of a TDC to 20ps in BiCMOS for different applications.

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ABSTRACT:

The measurement of time plays a fundamental role in many physics experiments. The TDC, Time to Digital Converter, is a device that returns a time interval every time the there's two input pulses. This device can be applied in many physics experiments because we are can convert physical events in pulses so as to measure the time between two pulses. In the data output from the TDC they are presented in binary order to simplify the work in the following processing steps. It can be applied in many fields where it is required a very accurate temporal resolution, such as for example high-energy physics[3,4,5,7] and in the medical. The TDC we are planning has a time resolution of 20ps, it uses the SiGe BiCMOS technology 0.13um[1,2] and it will be used in the medical field in particular in the TOF-PET[6] that leverages the time of flight for the reconstruction of the image.

Block diagram and functioning , one TDC channel, first run.

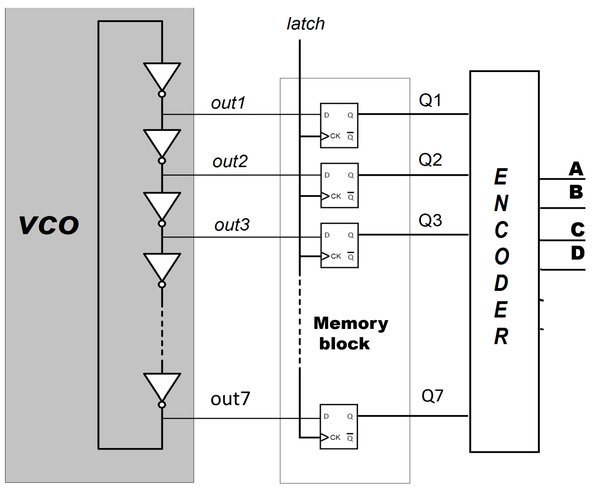


Fig. 1: Diagrams blocks of the first prototype of the TDC, run in February 2016

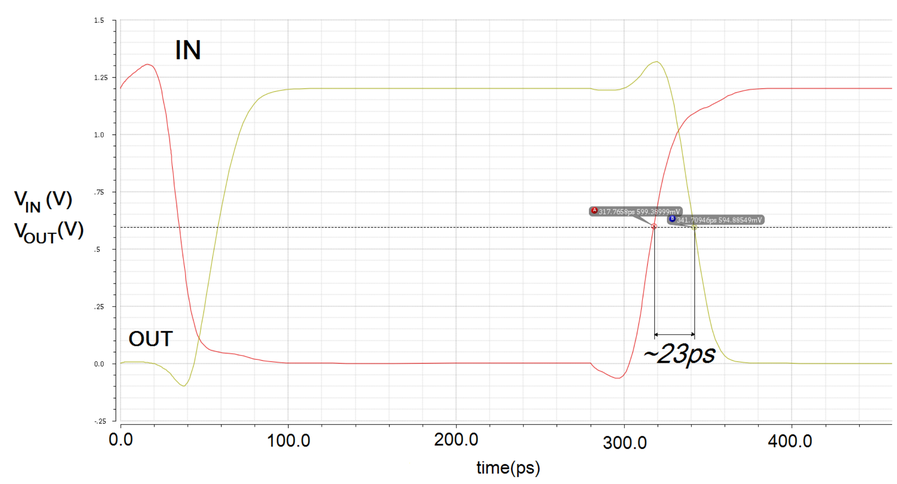
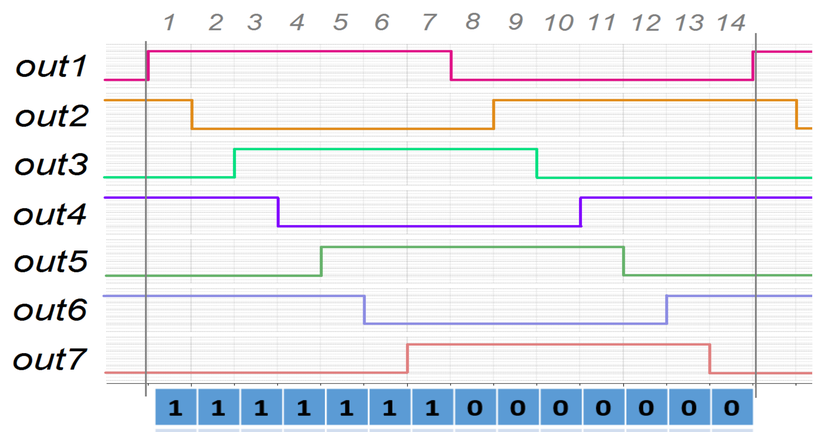


Fig. 2: Example delay time of the VCO, powered at 2.5V



1	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
1	0	0	0	0	0	0	0	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	1	1	1	1
0	0	0	0	1	1	1	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	0

Fig. 3: Out of the VCO and respective binary code that will be read from the block memory.

VCO

In this device, varying the supply voltage of a logic gate, we can control the transit time of a signal that passes through it. For the VCO we have chosen to use an odd number of inverters, using negative feedback, to create a ring oscillator that we control by power supply. This operation makes it possible to create a local controlled oscillator with a operating range of this devise is between 1ns and 18ps. In the fig.2 we can see the simulation of the seven outputs of the VCO, supplied at 2.5V that its has a delay time of about 23ps. The structure of the ring oscillating permit to divide the period in 14 different intervals. The size of each interval is determined by the supply voltage of the gate. In the fig. 3 each interval corresponds to a unique binary combination that will be read and sampled by the memory block.

MEMORY BLOCK

The secondo block is the memory, is realized by 7 flip-flops. They are used for reading and storing the temporal intervals of the VCO. The sampling frequency is controlled by a external signal, called LATCH, which is connected to pin clock present in all the FLIP-Flops. From the simulations we found that the maximum sampling frequency is 100MHz.

ENCODER

Is a device that encodes the 14 intervals of the VCO in a 4-bit binary code. On the fig. 4 there is the internal circuit made of logic gates.

The finaly layout is realized without the help of auto-ruting programs to maximize the gains, favouring the fast and delicate part of the TDC.

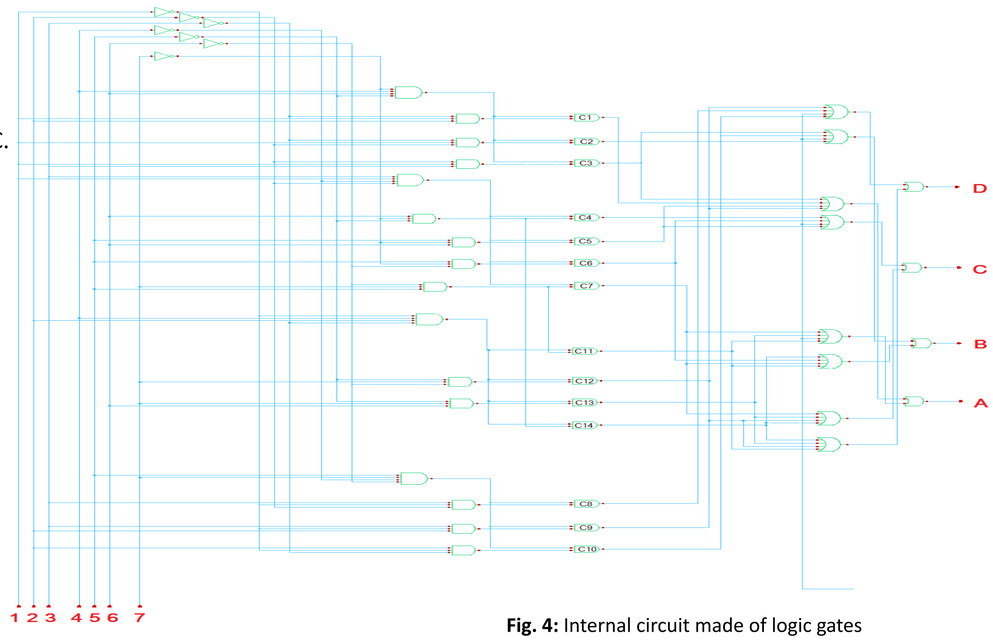


Fig. 4: Internal circuit made of logic gates

Layout run1

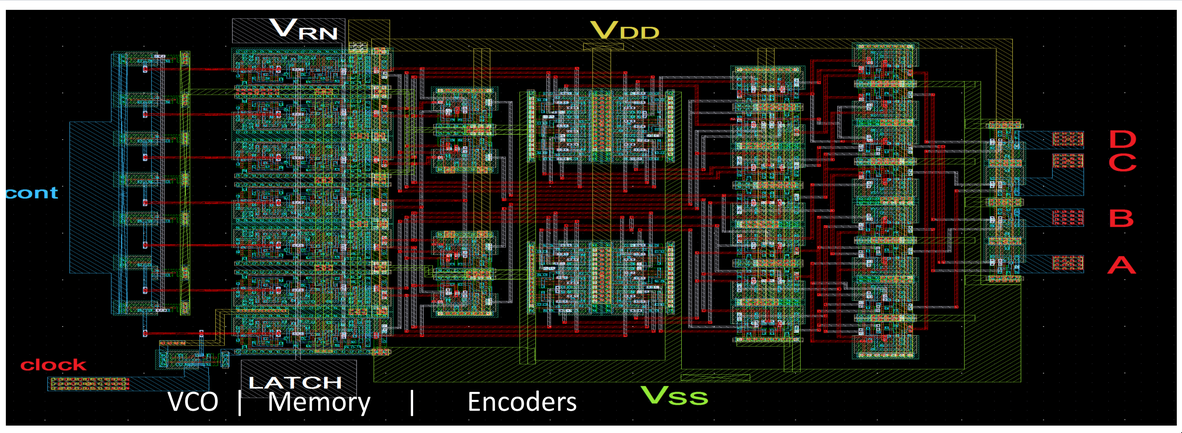


Fig. 5: Finaly layout realized for run1.

Simulation and results

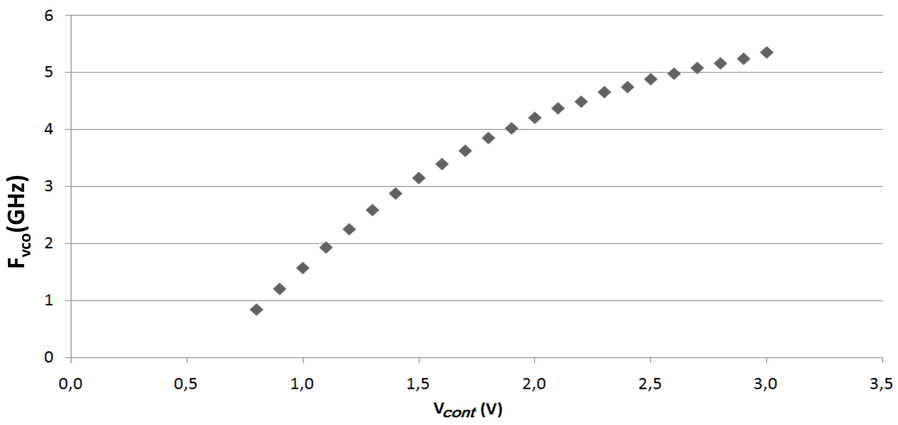


fig. 6: Range Frequency oscillation Vs applied voltage.

VCO results.

On fig 6 there is the results of the simulations to the fig 7 the results of the test bench. Comparing them, we observe a decrease of about 35%, as we expected passing from the simulation on the test bench. The oscillations shown in red are caused because we applied a higher voltage respect the foundry declarations. We can see that the measurement are repeatable in the operating range of 0.7V - 2.4.

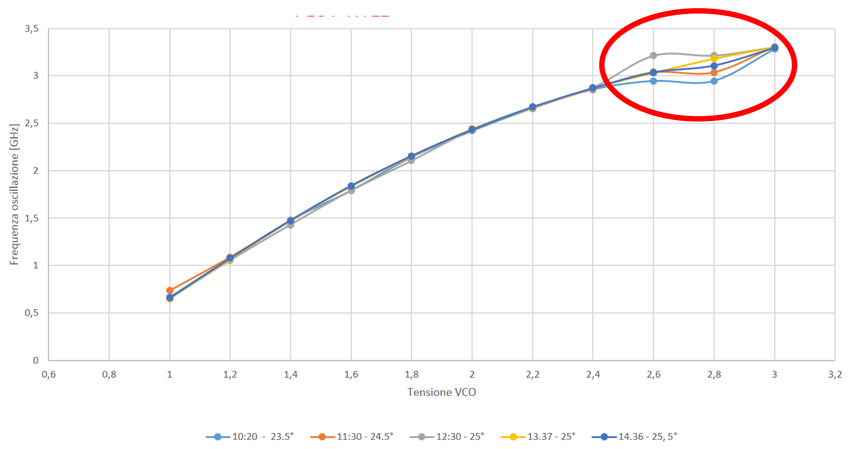


Fig. 7: Range Frequency oscillation Vs voltage applied.

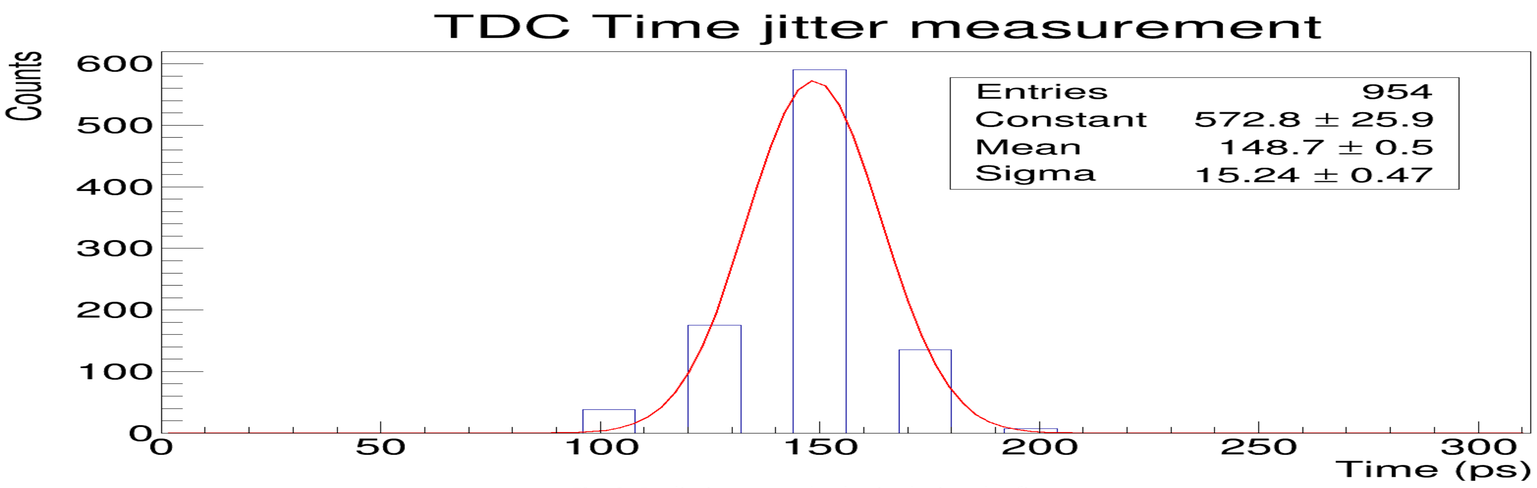


Fig. 8: Preliminary result obtain during the first prototype

TDC results

The test on the TDC has been executed measuring the time corresponding to the rise time of a signal at 100MHz, generated by a stimulus system MFS 9003 of the Tektronix. The difference of the times ΔT, measured on a sample of 954 events, is shown in fig. 8 and exhibits a gaussian jitter 15.2ps; since it corresponds 2 values, the error on the single measure è σ/√(2) = 10.77ps.

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