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A New Generation Pixel Readout ASIC in 65nm CMOS for HL-LHC experiments

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A first prototype of a readout ASIC in CMOS 65 nm for a pixel detector at High Luminosity LHC is described. The pixel cell area is of 50x50 um2 and the matrix consists of 64x64 pixels. The chip was designed to guarantee high efficiency at extreme data rates for very low signals and with low power consumption. Two different analogue very-front-end designs, one synchronous and one asynchronous, were implemented, both occupying an area of 35x35 um2. ENC value is below 100 e- or an input capacitance of 50 fF and in-time threshold below 1000 e-. Leakage current compensation up to 50 nA with power consumption below 5 uW. A ToT technique is used to perform charge sampling with 5-bit precision using either a 40 MHz clock or a local Fast Oscillator (up to few hundred MHz). Internal 10-bit DAC's are used for biasing, while monitoring is provided by a 12-bit ADC. A novel digital architecture has been developed which maintains high efficiency (above 99.5%) at pixel hit rates up to 3 GHz/cm2, trigger rates up to 1 MHz and trigger latency of 12.5 us. The total power consumption per pixel is below 5 uW. Analogue dead-time is below 1%. Data are sent via a serializer connected to a CMOS-to-SLVS transmitter working at 320 MHz. All IP-blocks and very-front-ends used are silicon proven and tested after high irradiation doses of 500-800 Mrad. The chip was designed as part of the Italian INFN CHIPIX65 project and in close synergy with the international CERN RD53 collaboration on 65 nm CMOS and was submitted in July 2016 for production. Test results of the prototype will be described. All ASIC functionalities are fully working, with a complex digital design working while the analog very front end works at 250e- threshold, confirming the fast, low noise and low power performances.

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