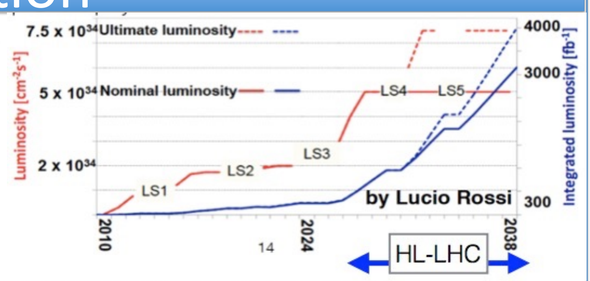
A New Generation Pixel Readout ASIC in 65nm CMOS for HL-LHC experiments

E. Monteil[1,2], L. Pacher[1,2], A. Paterno' [1,3], S. Marconi[4,13], F. Loddo[5], N. Demaria[1], L. Gaioni[6,10], F. De Canio[6,15], G. Magazzu'[7], G. Traversi[6,10], A. Rivetti[1], M. Da Rocha Rolo[1], G. Dellacasa[1], G. Mazza[1], F. Rotondo[1], R. Wheadon[1], C. Marzocca[5,8], F. Licciulli[5], F. Ciciriello[5,9], V. Re[6,10], L. Ratti[6,15], P. Placidi[4,13], A. Stabile[11], S. Mattiazzo[12], C. Veri[14]

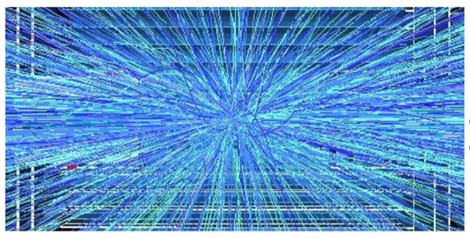
Introduction

Pixel detectors for HL-LHC experiments require the development of a new generation front-end chip to stand unprecedented radiation levels, very high hit rates and increased pixel granularity.



The main requirements for the HL-LHC detectors are:

- Small pixels: 50x50 µm²
- Trigger up to 1 MHz with 12.8 µs latency
- For innermost layer:
  - Pixel hit rate up to 3 GHz/cm²
  - Radiation: 1 Grad in 10 years
  - Data readout up to 4-5 Gbs/s



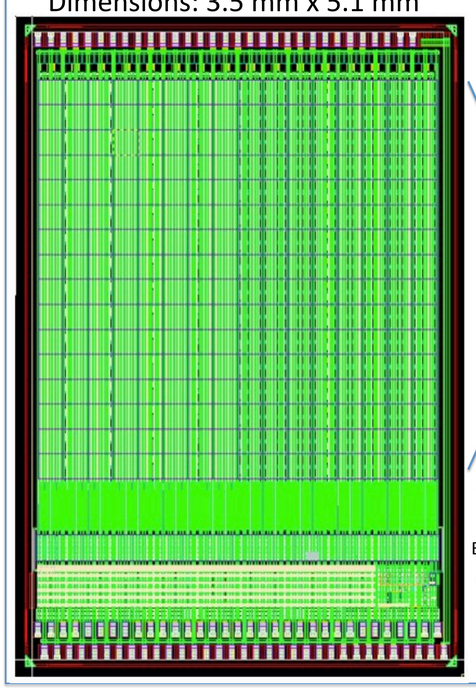
Typical HL-LHC event with Pile-Up equal to 140-200

In this context the CHIPIX65 project has been approved by INFN in fall 2013, with the goals of:

- Developing a CHIP for PIXel detectors in 65nm CMOS technology for the first time in HEP experiments
- Propagate the use of the 65nm technology inside INFN
- 8 sections involved (Bari, Lecce, Milano, Padova, Pavia/Bergamo, Perugia, Pisa, Torino)
- Funding member of the CERN RD53 collaboration

CHIPIX65 demonstrator

Dimensions: 3.5 mm x 5.1 mm



Main aspects:

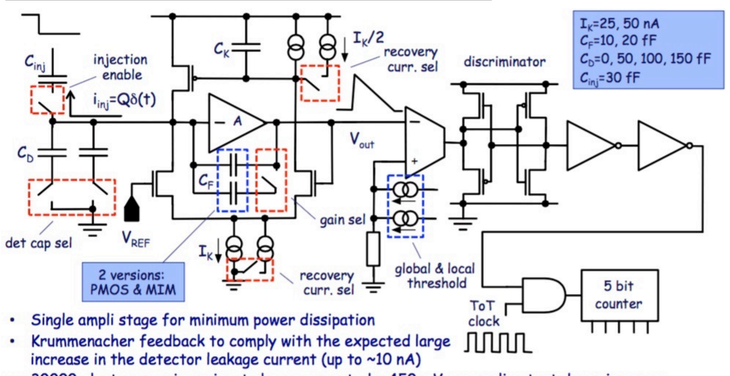
- Small and complex 64x64 pixel matrix (50x50 µm² each) featuring new solutions compatible with RD53A
- Two analog FEs (asynch and synch)
- A novel digital architecture
- Bias network and monitoring
- Chip configuration based on SPI protocol
- Usage of CERN I/O library

Design flow:

- Digital-On-Top chip assembly
- Top-down hierarchical flow
- Pixel matrix composed of 16x16 pixel regions (master and clone)
- A pixel region contains the digital architecture and the analog FEs

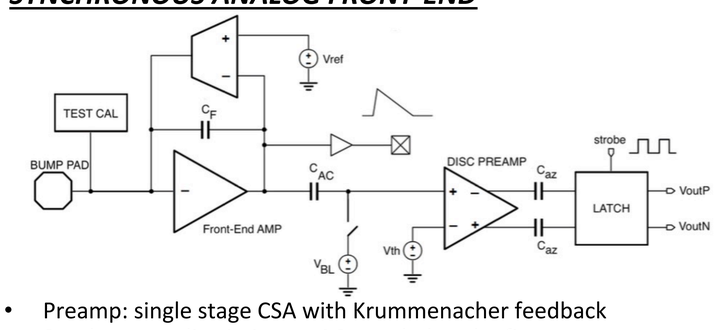
Building blocks

ASYNCHRONOUS ANALOG FRONT-END



- Single ampli stage for minimum power dissipation
- Krummenacher feedback to comply with the expected large increase in the detector leakage current (up to ~10 nA)
- 30000 electron maximum input charge expected, ~450 mV preampli output dynamic range
- Selectable gain, recovery current and detector emulating capacitance
- 40 MHz clock, 5 bit dual edge counter, 400 ns maximum ToT

SYNCHRONOUS ANALOG FRONT-END

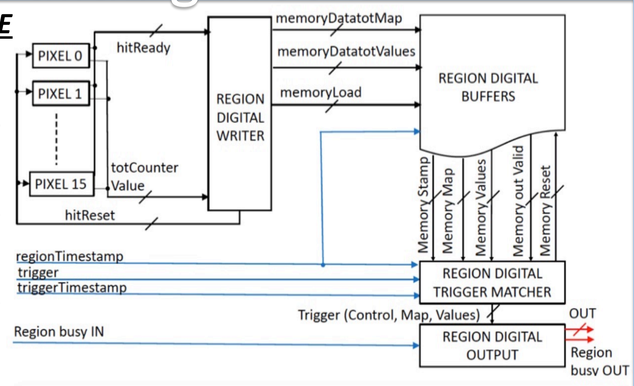


- Preamp: single stage CSA with Krummenacher feedback
- Synchronous discriminator AC coupled to the first stage
- Offset compensation done with capacitors (no trimming needed)
- Fast ToT using the latch as a local oscillator (up to 800 MHz)

DIGITAL ARCHITECTURE

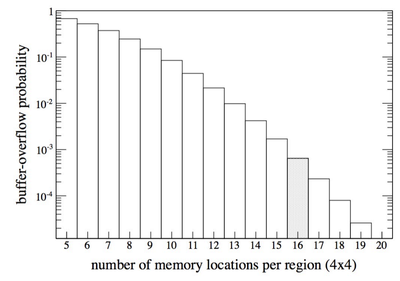
Pixel region choice:

- Focused on a centralised fully shared latency buffer
- 4x4 pixel region
  - Allows better sharing of resources like trigger matching
  - Number of memory locations/pixel should scale by a factor of about 2



- Digital region operating modes:
  - Triggerless/triggered/debug
  - Binary Only/5-bit-ToT
  - High/Low deadtime (to match Slow or Fast ToT from analog)

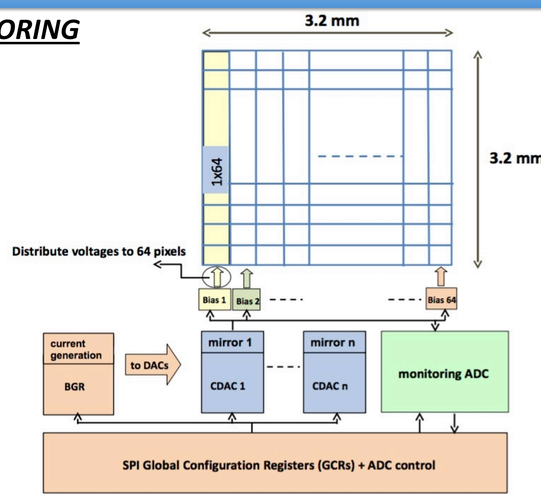
- Total power: around 6 µW/pixel



	Inefficiencies (digital) @ 3 GHz/cm²
Trigger latency	12.8 µs
Particle loss	<0.1%
Single pixel efficiency	99.9% (digitized 5-bit ToT info except for 0.4% with binary info only)
Ghosts probability	<0.03%

BIAS AND MONITORING

- 16 current DACs
- Currents mirrored from DACs to bias cells
- Compatible with a matrix of 400x400 pixels

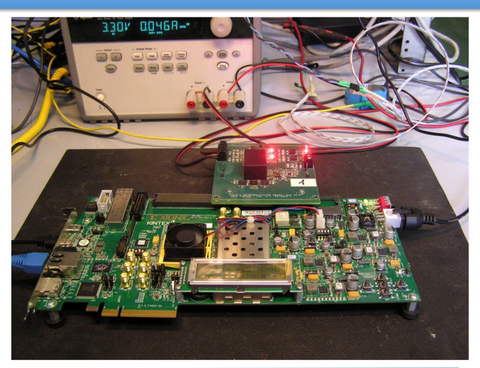


- DAC:
  - 10-bit current steering DAC – LSB = 100 nA
  - 8+2 segmented DAC (2 binary weighted + 8 unitary decoded cells)
  - Characterized in lab
  - X-ray irradiation tests at Padova showed no significant degradation
- ADC:
  - 12-bit ADC for monitoring slowly varying signals
  - Conversion rate: 5kSample/s
  - Voltage-to-current architecture
  - Large capacitance for better precision
- BANDGAP:
  - Temperature range: -40°C/80°C
  - Irradiated up to 800 Mrad
  - Trimming can correct process and radiation-induced variations with a mismatch < 2%

Measurement results

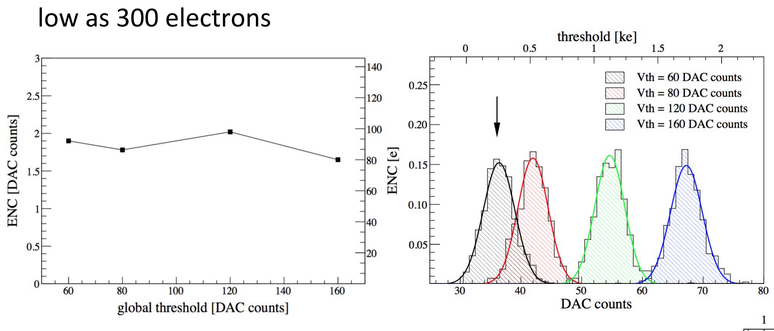
EXPERIMENTAL SETUP

- Full digital ASIC/FPGA interface (FMC)
- Chip wire-bonded to a custom test board
- FPGA Xilinx Virtex 7 board
- LabView data acquisition test interface

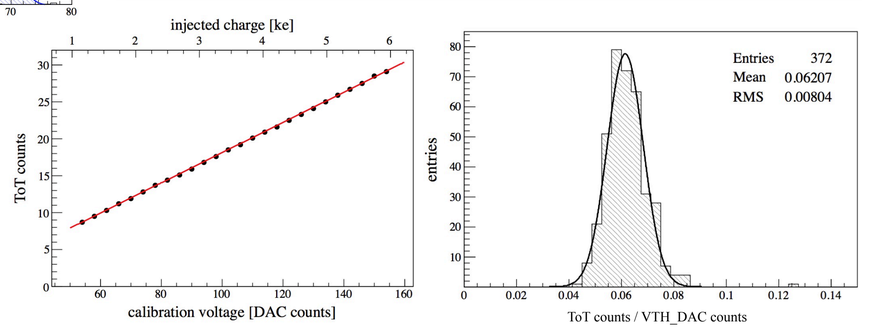


SYNCHRONOUS ANALOG FRONT-END

- Using the S-curve technique, noise and threshold have been measured for 1024 pixels inside the matrix for different values of the global threshold
- The ENC is independent of the global threshold and is around 90 electrons
- The chip has been successfully operated with thresholds as low as 300 electrons



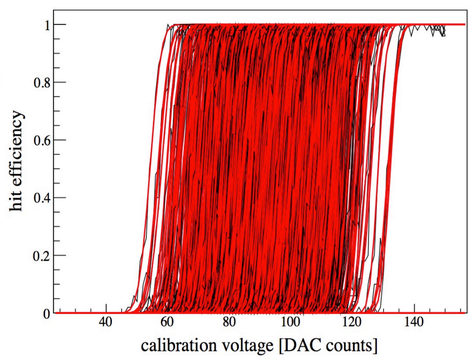
- The local oscillator for fast 5-bit ToT counting has been activated with a frequency equal to 320 MHz
- The ToT linearity has been verified for a single pixel
- Mismatch effects lead to a variation of the ToT value between pixels
- The RMS of the resulting distribution is around 12% of the mean value
- This result is compatible with the CAD simulations



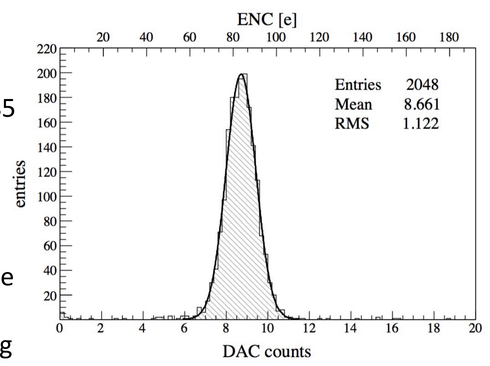
ASYNCHRONOUS ANALOG FRONT-END

- The S-curve technique has been used also for the measurements on the asynchronous design
- All pixels have been tested and proved to be fully working

- First measurements have been performed in the untrimmed configuration
- The plot on the right shows the superimposition of the S-curves for all pixels

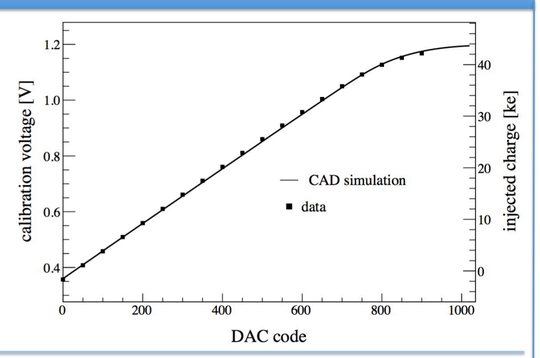


- The untrimmed threshold dispersion is 450 electrons RMS
- The ENC is equal to 85 electrons
- Both results are compliant with CAD simulations
- Measurements on the threshold tuned configuration ongoing



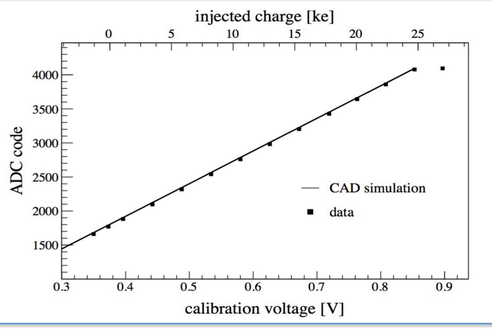
DAC

- The output of the DAC used for the injection of the calibration signal has been measured
- A very good agreement with the CAD simulations has been obtained



ADC

- The calibration voltage has been fed into the monitoring ADC
- A linear ADC characteristic has been obtained, also in this case showing a good agreement with simulations



Conclusions

- CHIPIX65 is a INFN project with around 40 people and 8 institutes and is a very active part of the CERN RD53 collaboration
- The CHIPIX65 demonstrator is an intermediate step towards the RD53A prototype. It is characterized by a matrix of 64x64 pixels
- The chip contains two flavors of analog front-ends, a novel Pixel Region digital architecture and several building blocks for bias and monitoring
- First measurements have shown that all the building blocks are fully working
- The main features of the synchronous front-end like offset compensation and fast ToT work properly, with a ENC of 90 electrons
- The asynchronous front-end in untrimmed configuration shows threshold dispersion of 450 e^- and ENC of 85 e^-
- The bias and monitoring blocks have been characterized obtaining results compliant with CAD simulations

[1] INFN Torino [2] Università di Torino [3] Politecnico di Torino [4] INFN Perugia [5] INFN Bari [6] INFN Pavia [7] INFN Pisa [8] Politecnico di Bari [9] Università di Bari [10] Università di Bergamo [11] INFN Milano [12] Università di Padova [13] Università di Perugia [14] Università del Salento [15] Università di Pavia

IFAE 2017 – XVI Incontri di Fisica delle Alte Energie – Trieste, April 19th-21st 2017