HVCMOS EXPERIENCE FOR LHCB

… and some comments on Mechanics/Cooling

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TECHNOLOGY MOVES QUICKLY

- What do we have "now" for tracking
  - Hybrid pixels
  - CMOS

- *Quest*
  - Low power
  - Low mass
  - High Spatial Resolution (1-10um)
  - High Temporal Resolution (< 1ns)

HVCMOS

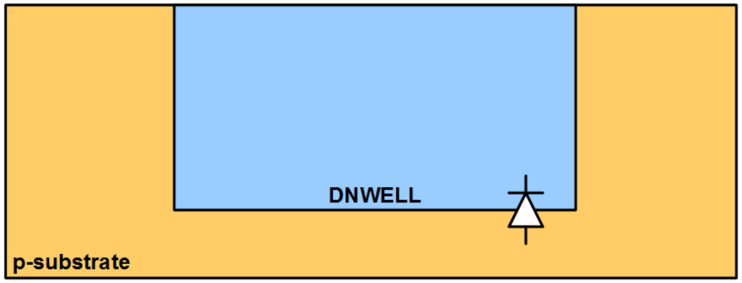
- Thanks to HVCMOS team @Liverpool
  - Eva Vilella-Figueras
  - Joost Vossebeld (mu3e)
  - Gianluigi Casse (FBK)
- ATLAS colleagues
- Manchester…
- Many others

HV-CMOS SENSORS - TECHNOLOGY DETAILS

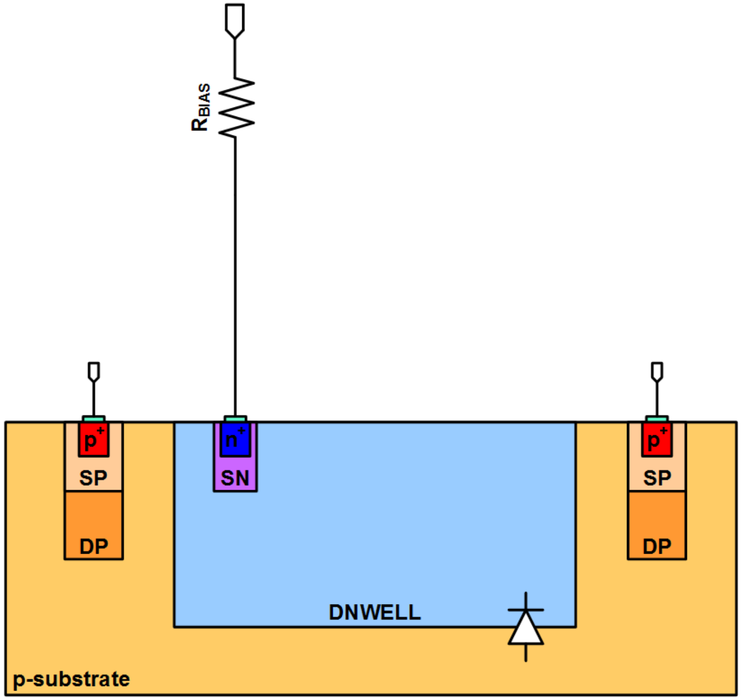
- The majority of commercial HV-CMOS technologies use p-type substrates

HV-CMOS SENSORS - TECHNOLOGY DETAILS

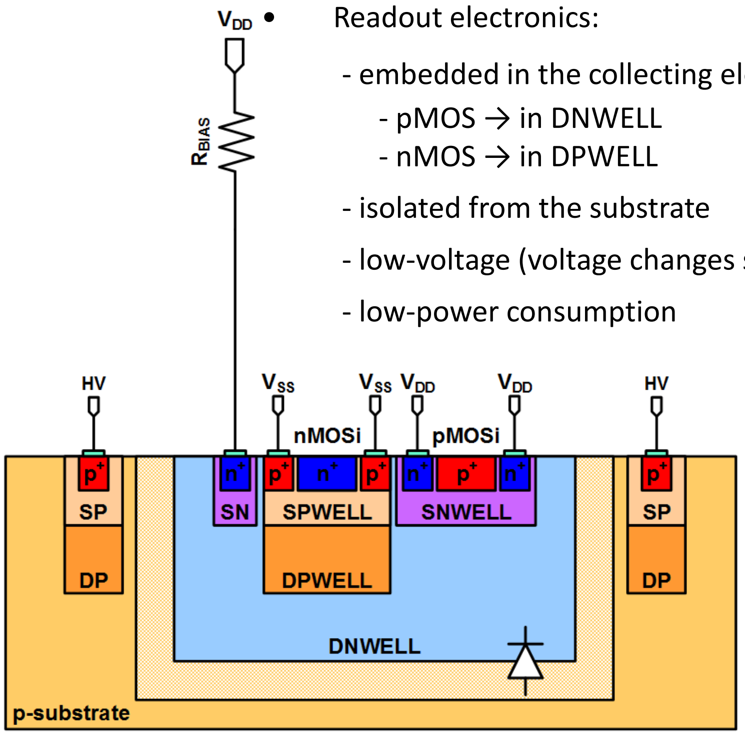
- A DNWELL/p-substrate diode is the sensing element



HV-CMOS SENSORS - TECHNOLOGY DETAILS

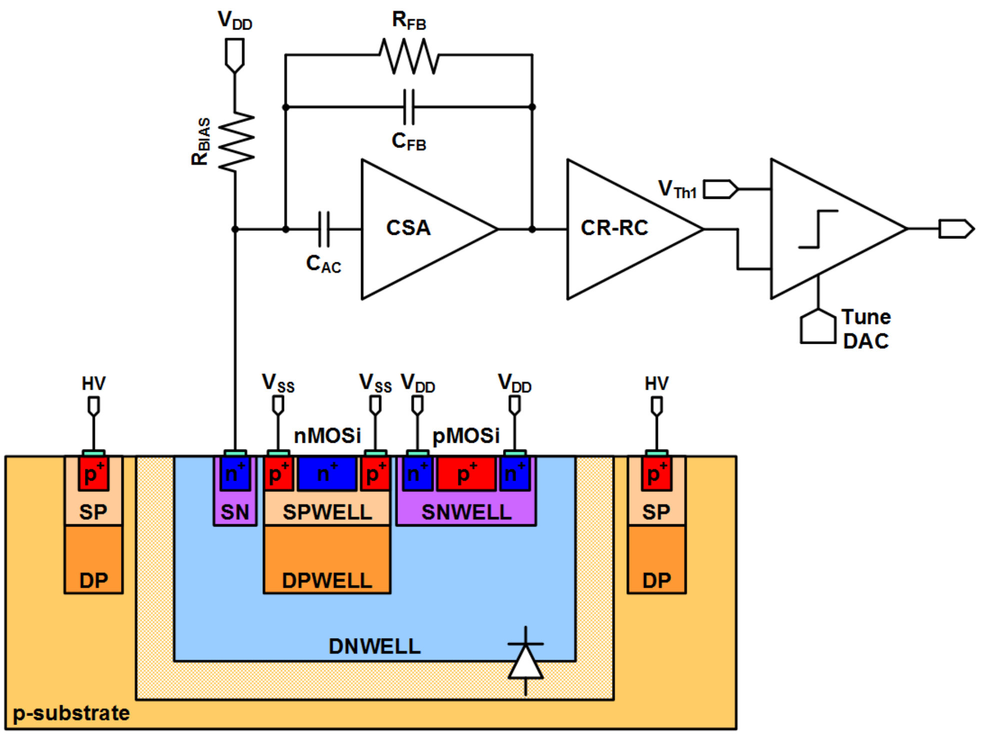


HV-CMOS SENSORS - TECHNOLOGY DETAILS

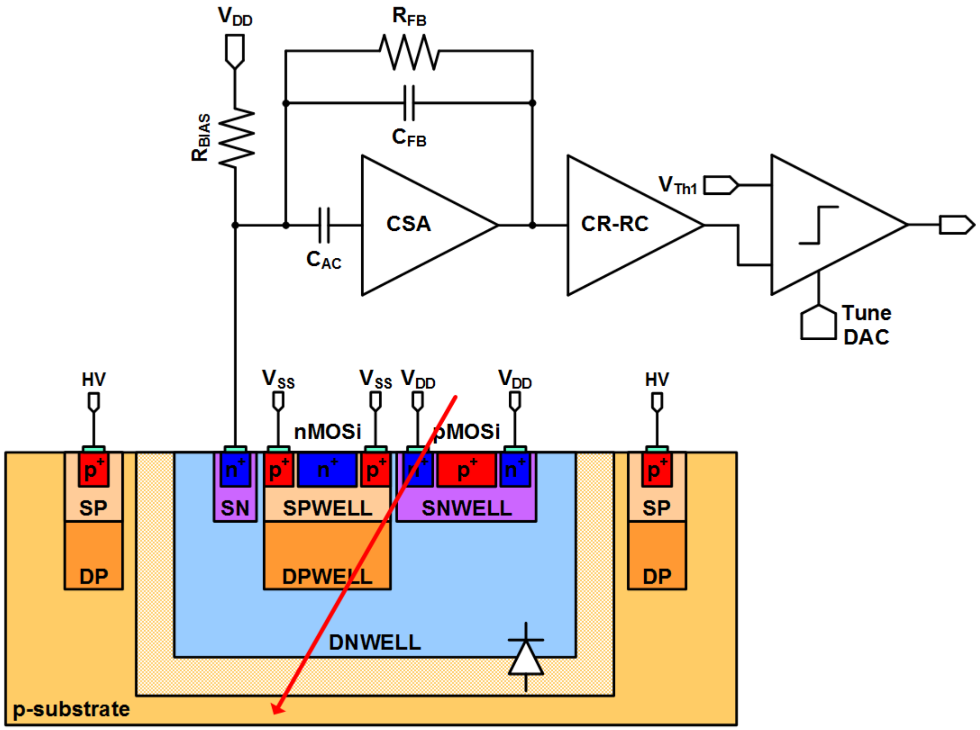


- Readout electronics:
  - embedded in the collecting electrode (DNWELL)
    - pMOS → in DNWELL (biased to V_{DD})
    - nMOS → in DPWELL (biased to V_{SS})
  - isolated from the substrate
  - low-voltage (voltage changes swing between V_{SS} and V_{DD})
  - low-power consumption

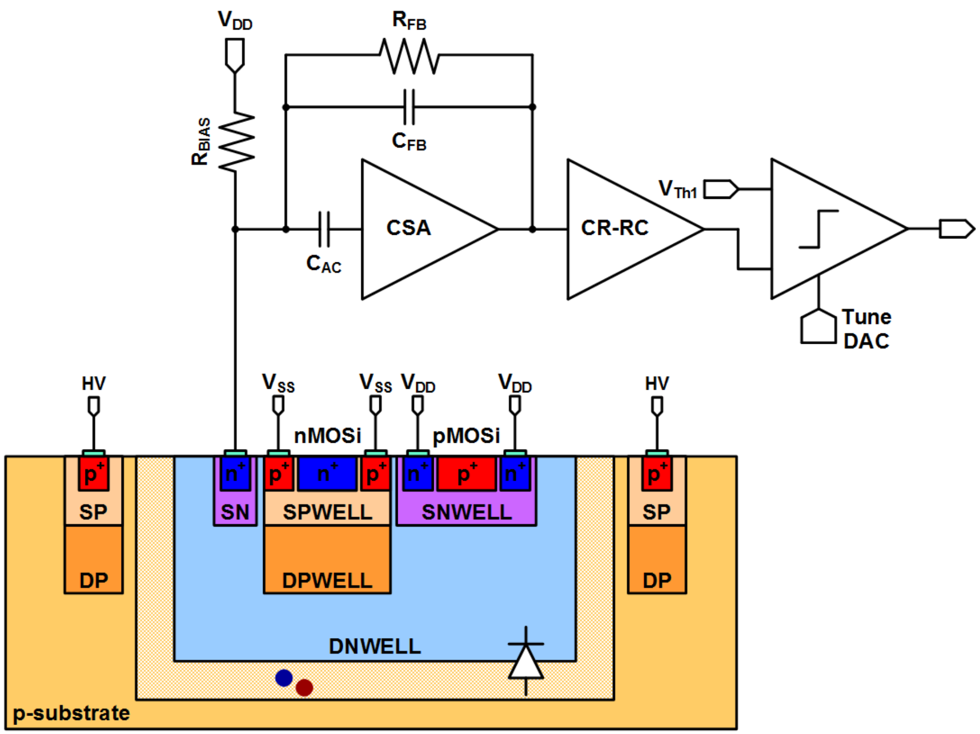
HV-CMOS SENSORS – TECHNOLOGY DETAILS



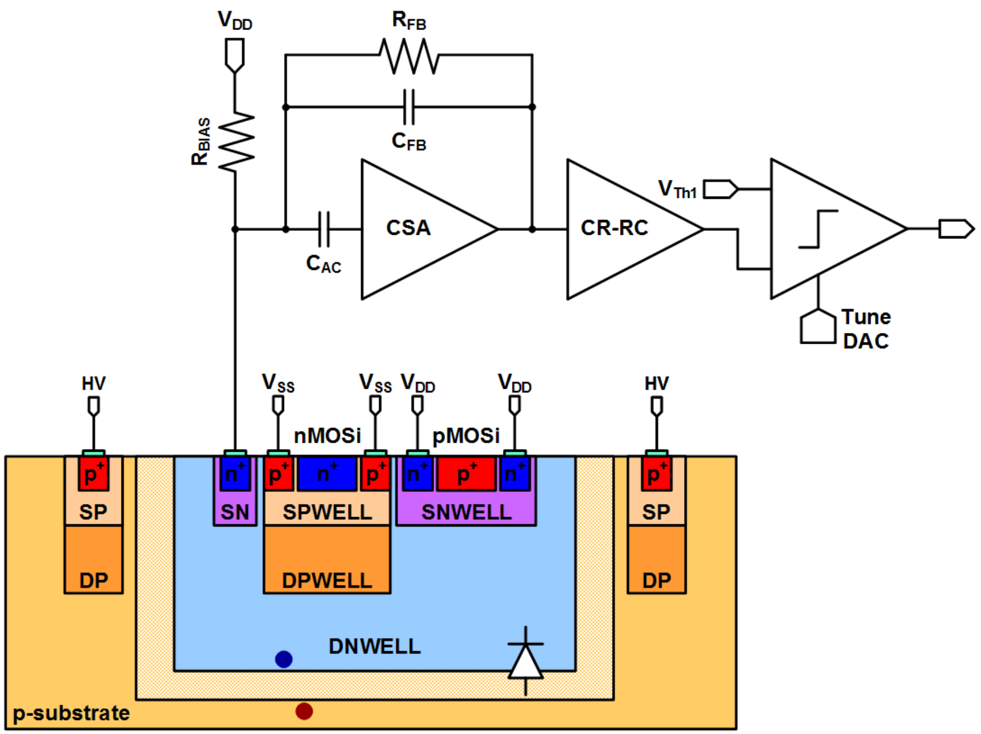
HV-CMOS SENSORS – TECHNOLOGY DETAILS



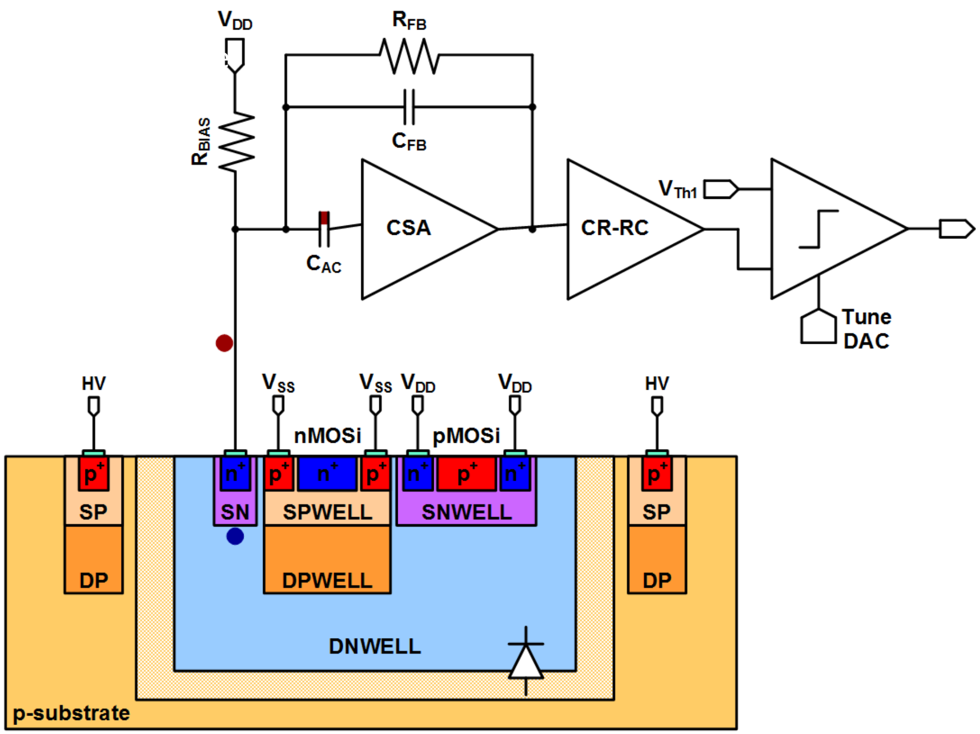
HV-CMOS SENSORS - TECHNOLOGY DETAILS



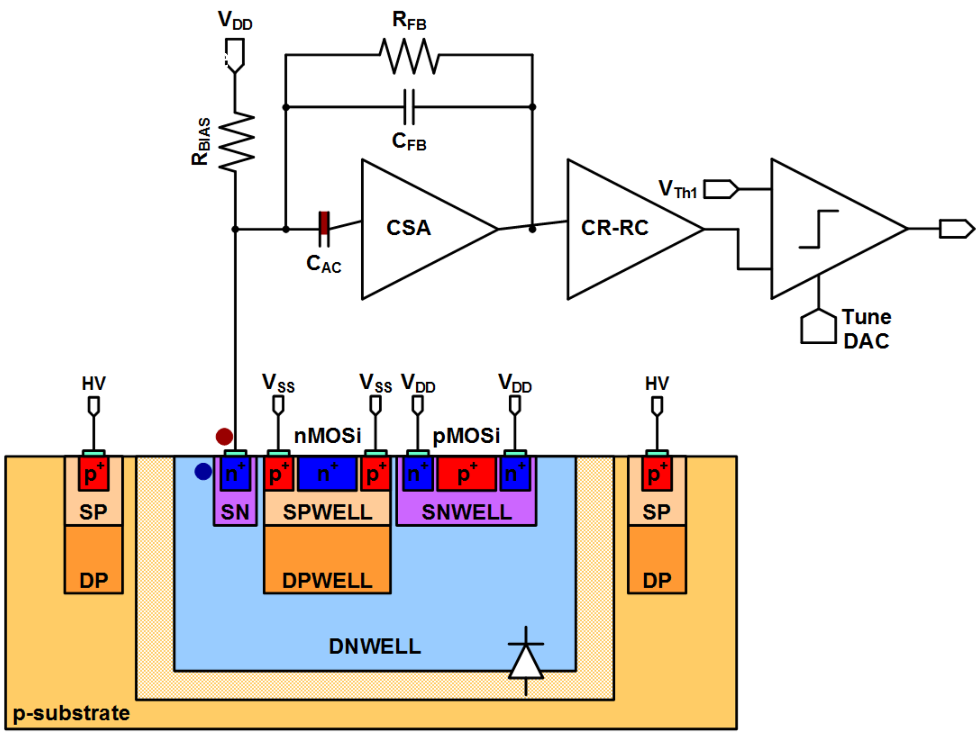
HV-CMOS SENSORS - TECHNOLOGY DETAILS



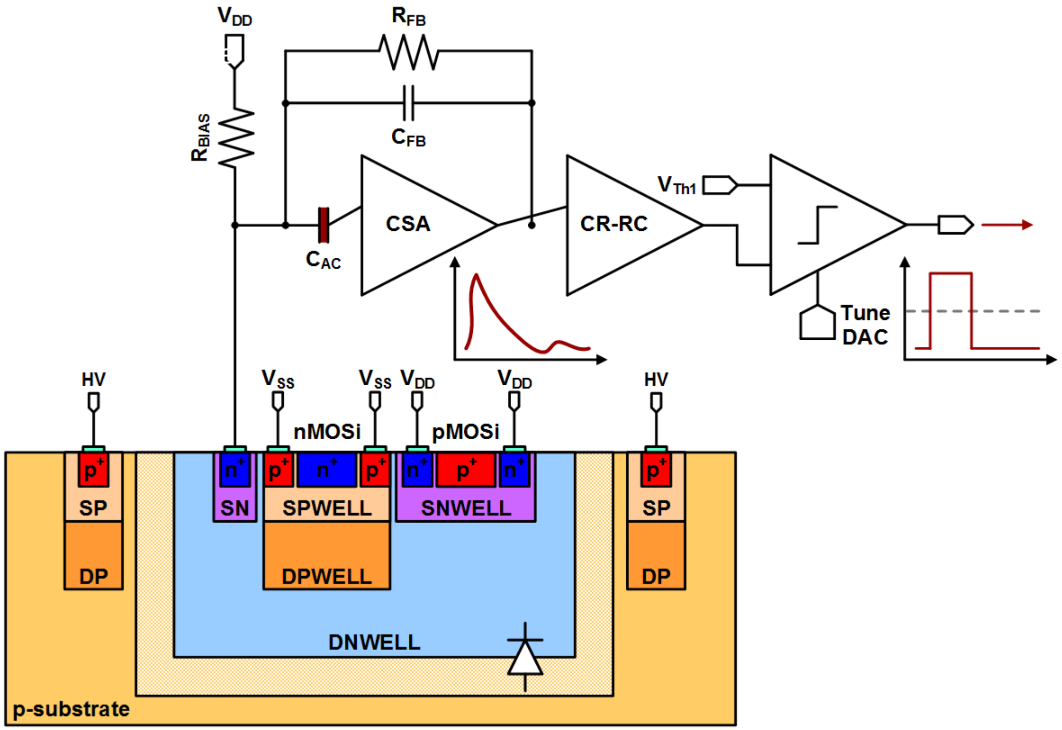
HV-CMOS SENSORS - TECHNOLOGY DETAILS



HV-CMOS SENSORS - TECHNOLOGY DETAILS



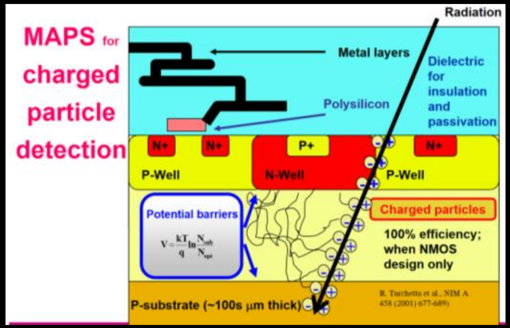
HV-CMOS SENSORS[14]- TECHNOLOGY DETAILS



14/5
7

SENSORS

- In-pixel amplification
- In-pixel processing electronics are also possible → **very strong signal at pixel output**
- **Readout and digitization electronics on the same chip** with the pixel array
- Very small pixel sizes are possible (18 μm x 18 μm) → **high granularity**
- Low leakage current + small sensor capacitance → **excellent noise performance** (~10 e^- per pixel)
- 14-20 μm thick epi layer → **high signal-to-noise ratio** (1 MIP generates ~1000 e^-)
- Epi layer is underneath the readout electronics → **100% fill-factor**
- **Back-thinning to 50 μm is possible** whilst sensor performance is unaffected
- **CMOS sensors have demonstrated excellent performance** (EUDET/AIDA telescope, STAR at RHIC-BNL)
- **Low bias voltage** → **charge collection by diffusion** → **long charge collection times (<100 ns)**
- **Limited radiation tolerance** → **<1 Mrad (TID)**, **<2·10^13^ 1 MeV n_{eq}/cm^2 (NIEL)**



SENSORS

- **MAPS** are excellent sensors with many practical advantages, but **charge collection via diffusion** makes them

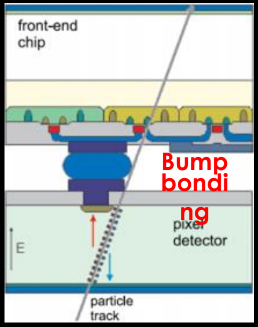
  - too slow
  - not sufficiently radiation tolerant

  for certain experiments.

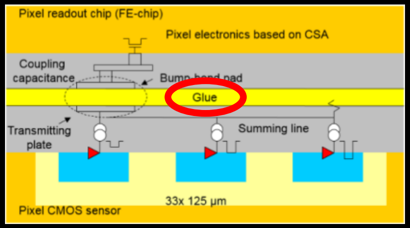
- **High Voltage-MAPS (HV-MAPS)** combine the advantages of MAPS with a "high" voltage of up to 120 V which is applied between the substrate and deep n-wells containing the transistors. This voltage leads to

  - fast charge collection via drift
  - better radiation tolerances.

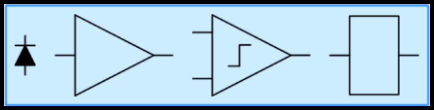
Hybrid pixel



Hybrid HV-CMOS



Fully monolithic HV-CMOS (HV-MAPS)



Diode + CSA + discrimin. + digital readout on sensor chip

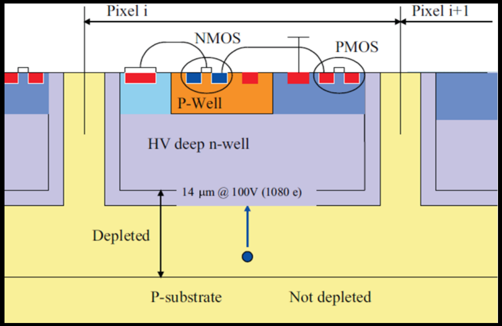
FOUNDRIES

	AMS	LFoundry	ESPROS	XFAB	TowerJazz
Feature node	180 nm/ 0.35 µm	150 nm	150 nm	180 nm	180 nm
HV	≤ 100 V/ ≤ 150 V	≤ 60 V	≤ 15 V	≤ 200 V	≤ 5 V
HR	2016/Yes	Yes	Yes	Yes	Yes
Quadruple well	No (triple)	Yes	Yes	No (BOX)	Yes
Metal layers	6/4	6	6	6	6
Backside processing	No	Yes	Yes	No	Yes
Stitching	No	Yes	No	No	Yes
TSV	Yes	No	No	No	No

- Other options are:
  - Global Foundries 130 nm, IBM 130 nm, OKI/LAPIS/KEK, ON Semiconductor 180 nm (formerly AMIS), Toshiba 130 nm, TSMC 65 nm

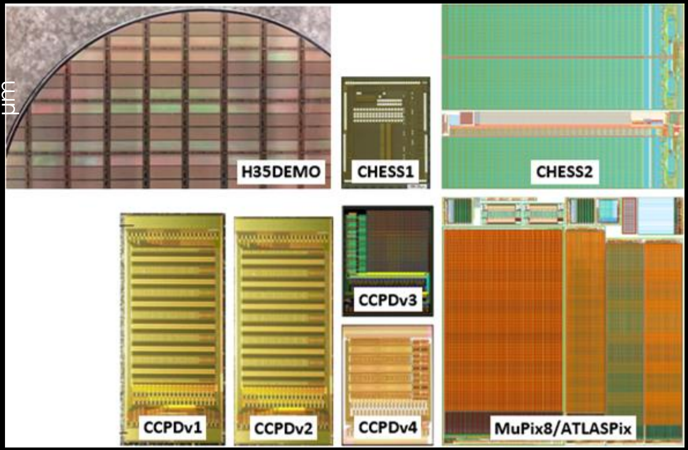
AMS

Foundry	Feature node [nm]	HV [V]	HR [Ω·cm]	Depletion region [µm]	P-N wells	Metal layers	Backside biasing	Stitching	TSV
ams	350 180	<150	20 – 1k 10 – 1k	140	Triple	4 6	No	No	Yes
LFoundry	150	<120	10 – 4k	170	Quadruple	6	Yes	Yes	No
TowerJazz	180	<6	1k – 8k	18 – 40	Quadruple	6	Yes	No	No
XFAB	180	<200	100	–	BOX layer	7	No	No	No
ESPROS	150	<20	2k	50	Quadruple	6	Yes	No	No



I. Peric, NIMA 650 pp. 158-162, 2011

ams 0.35 µm



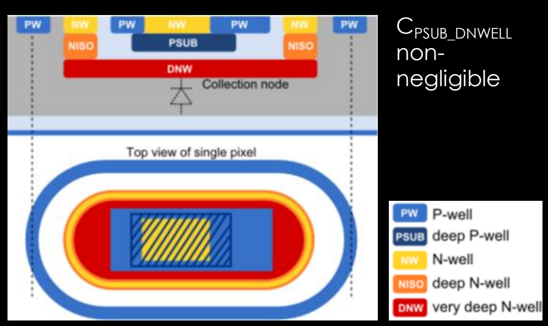
Plus:
- initial R&D
- H35CCPDv1-2
- HVStrip

Plus:
- CCPDv1-8
- CLICpix (CCPDv3)
- C3PD
- MuPix1-8 (Mu3e)

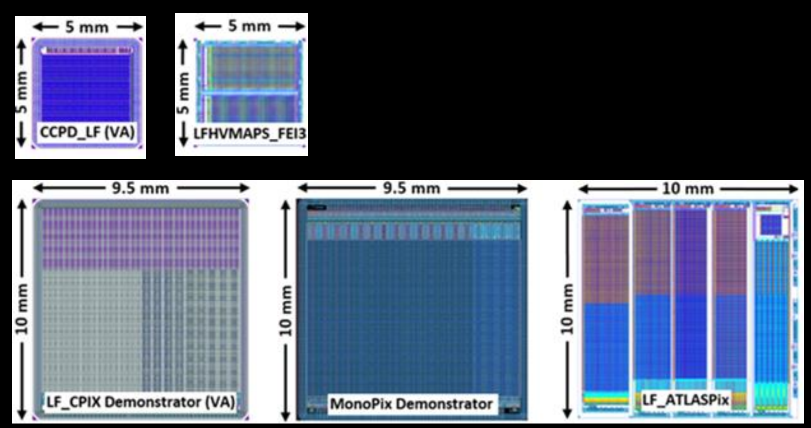
- No possibility of isolating n-wells from the collecting deep n-well. No CMOS electronics in the sensor area.

LFOUNDRY

Foundry	Feature node [nm]	HV [V]	HR [Ω·cm]	Depletion region [μm]	P-N wells	Metal layers	Backside biasing	Stitching	TSV
ams	350 180	<150	20 – 1k 10 – 1k	140	Triple	4 6	No	No	Yes
LFoundry	150	<120	10 – 4k	170	Quadruple	6	Yes	Yes	No
TowerJazz	180	<6	1k – 8k	18 – 40	Quadruple	6	Yes	No	No
XFAB	180	<200	100	–	BOX layer	7	No	No	No
ESPROS	150	<20	2k	50	Quadruple	6	Yes	No	No



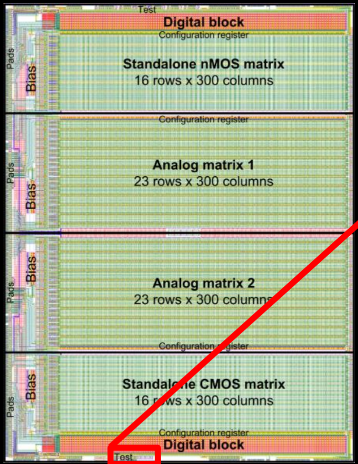
C_{PSUB_DNWELL} non-negligible



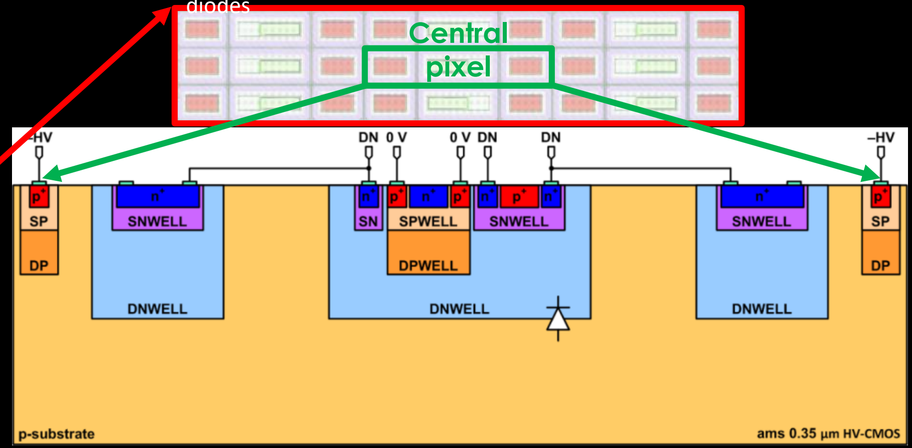
P. Rymaszewski, JINST 11 C02045, 2016

- Deep p-well (PSUB) to isolate n-wells from deep n-well (collecting electrode).
- Full CMOS electronics are possible in the sensor area.

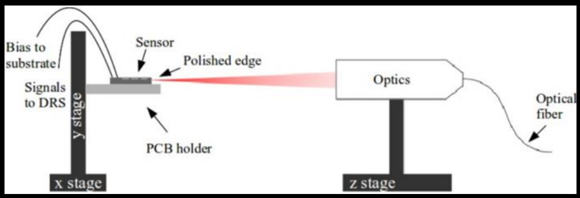
E-TCT



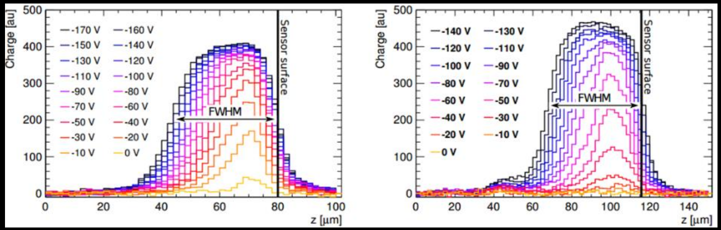
No circuitry or metal layers on top of the sensing diodes



e-TCT set-up:



Measured results:



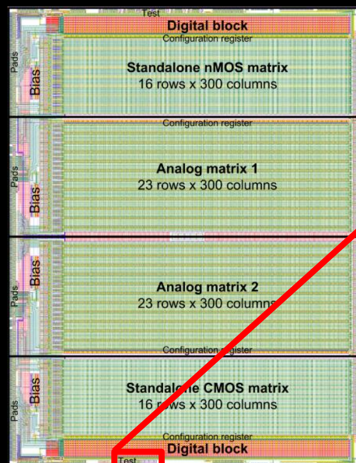
ρ=80 Ω·cm, d~35 μm @ -170 V

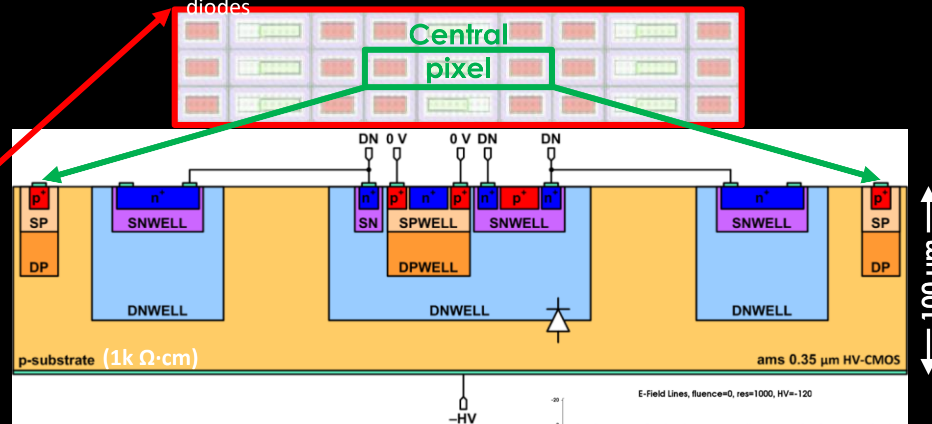
ρ=200 Ω·cm, d~45 μm @ -140 V

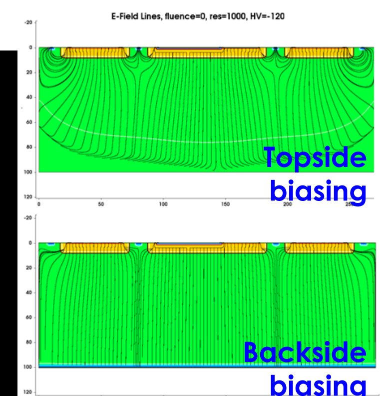
E. Cavallaro, arXiv:1611.04970v2

H35DEMO - E-TCT MEASUREMENTS

No circuitry or metal layers on top of the sensing diodes







cm

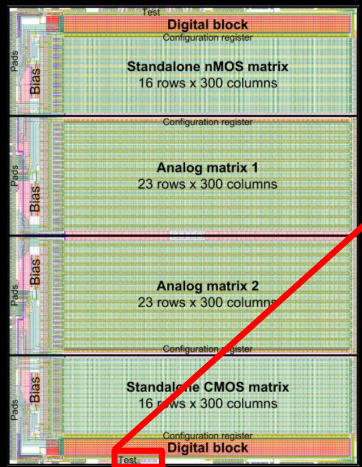
- thinning to 100 μm
- backside p⁺ implantation with boron
- thermal annealing
- backside metallization

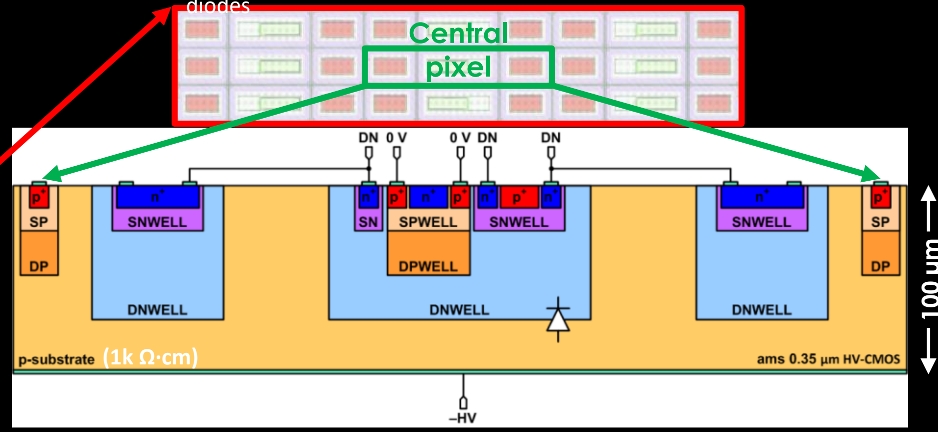
to allow backside biasing and achieve a **stronger, more uniform electric field in the sensing volume**

Higher voltage???

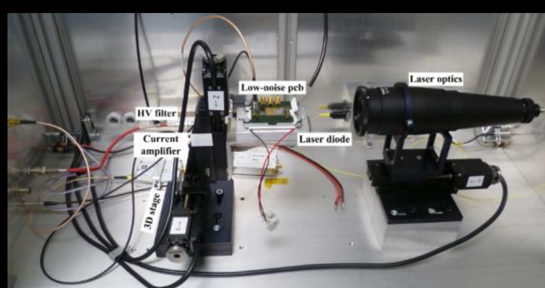
H35DEMO - E-TCT MEASUREMENTS

No circuitry or metal layers on top of the sensing diodes



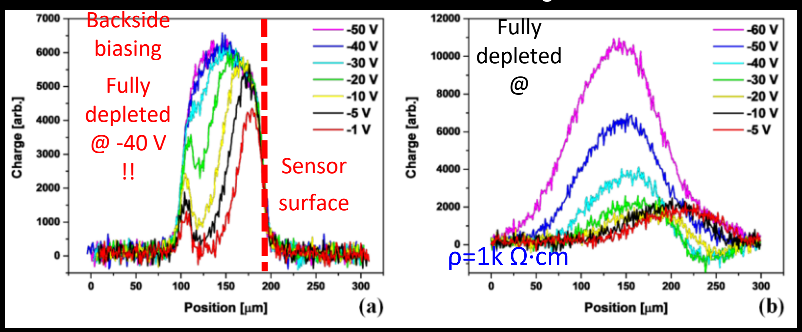


e-TCT set-up:



Measured results:

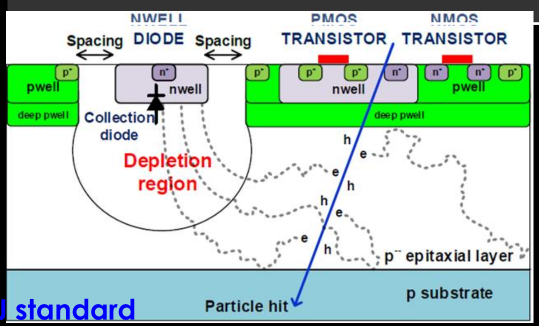
Topside biasing



ρ=1k Ω·cm, d~100 μm @ -40 V

TOWERJAZZ

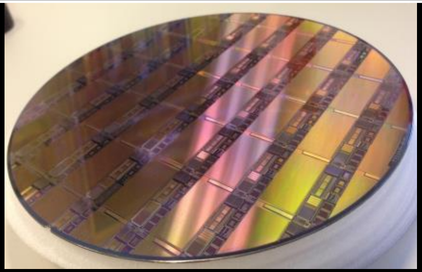
Foundry	Feature node [nm]	HV [V]	HR [Ω·cm]	Depletion region [μm]	P-N wells	Metal layers	Backside biasing	Stitching	TSV
ams	350 180	<150	20 – 1k 10 – 1k	140	Triple	4 6	No	No	Yes
LFoundry	150	<120	10 – 4k	170	Quadruple	6	Yes	Yes	No
TowerJazz	180	<6	1k – 8k	18 – 40	Quadruple	6	Yes	No	No
XFAB	180	<200	100	–	BOX layer	7	No	No	No
ESPROS	150	<20	2k	50	Quadruple	6	Yes	No	No

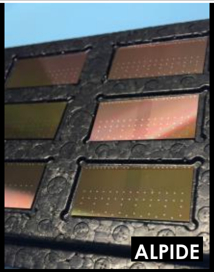


TJ standard

D. Kim et al., JINST 11 C02042, 2016

- Deep p-well to isolate n-wells from p-epi layer.
- <u>Full CMOS electronics are possible in the sensor area</u>.





<u>Plus</u>:
- MISTRAL
- ASTRAL
- CHERWELL
- Explorer
- Investigator
- MALTA
- MonoPix

- <u>Small n-well diode</u> → <u>low sensor capacitance</u> (~5 fF) → higher gain, better SNR, faster signal and potentially lower power consumption

Prepared for submission to JINST

Testbeam results of irradiated ams H18 HV-CMOS pixel sensor prototypes

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Abstract: HV-CMOS pixel sensors are a promising option for the tracker upgrade of the ATLAS experiment at the LHC, as well as for other future tracking applications in which large areas are to be instrumented with radiation-tolerant silicon pixel sensors. We present results of testbeam characterisations of the 4th generation of Capacitively Coupled Pixel Detectors (CCPDv4) produced with the ams H18 HV-CMOS process that have been irradiated with different particles (reactor neutrons and 18 MeV protons) to fluences between $1 \cdot 10^{14}$ and $5 \cdot 10^{15}$ 1-MeV- n_{eq}/cm^2. The sensors were glued to ATLAS FE-I4 pixel readout chips and measured at the CERN SPS H8 beamline using the FE-I4 beam telescope. Results for all fluences are very encouraging with all hit efficiencies being better than 97% for bias voltages of 85 V. The sample irradiated to a fluence of $1 \cdot 10^{15}$ n_{eq}/cm^2 – a relevant value for a large volume of the upgraded tracker – exhibited 99.7% average hit efficiency. The results give strong evidence for the radiation tolerance of HV-CMOS sensors and their suitability as sensors for the experimental HL-LHC upgrades and future large-area silicon-based tracking detectors in high-radiation environments.

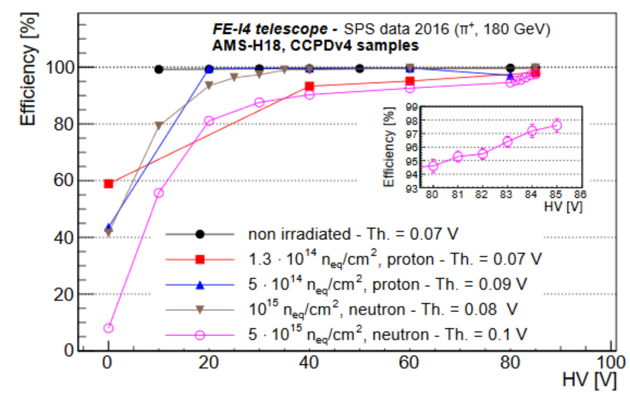


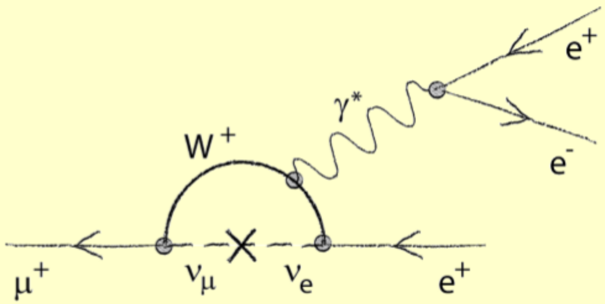
Figure 7. Average hit efficiency as a function of applied bias voltage. The insert shows the sudden increase in efficiency between 80 and 85 V, which could be attributed to charge multiplication

WHAT THIS ALL MEANS ….

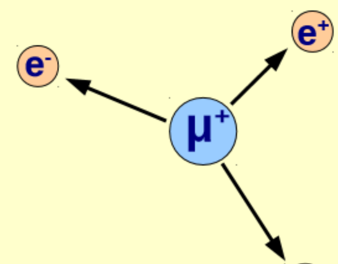
- "Guessing" you can look forwards to…
  - Monolithic* (low cost) sensor O(x) CHF/cm^2.
  - O(20) micron pixels and displaced digital periphery
  - 40 Mhz or better readout
  - Thickness to O(25um)
  - Radiation tolerance will(may) increase to O(10^{16} 1MeV n/cm^2)
  - Power dissipation < 1 W/cm^2
  - Power still looks too high for direct radiative cooling of sensor (<< 0.1W cm^2)
  - Time to ns resolution level - but not too much better. Collection O(100ps)
- Associated new low mass mechanics with cooling
  - Look at < 0.2 % per layer with cooling

NOTE

- Digital periphery is, at the moment, “dead”, in MAPs
- Need to stich and overlap OR glue/bond in a hybrid pixel type of way (a service chip)
- Can we find a way to go to 100% fill ?
- Cost related => more steps increase complexity
- BUT with big pixels(IT) and multiwells may have a chance to kill periphery…design study needed



$\mu^+ \rightarrow e^+e^+e^-$



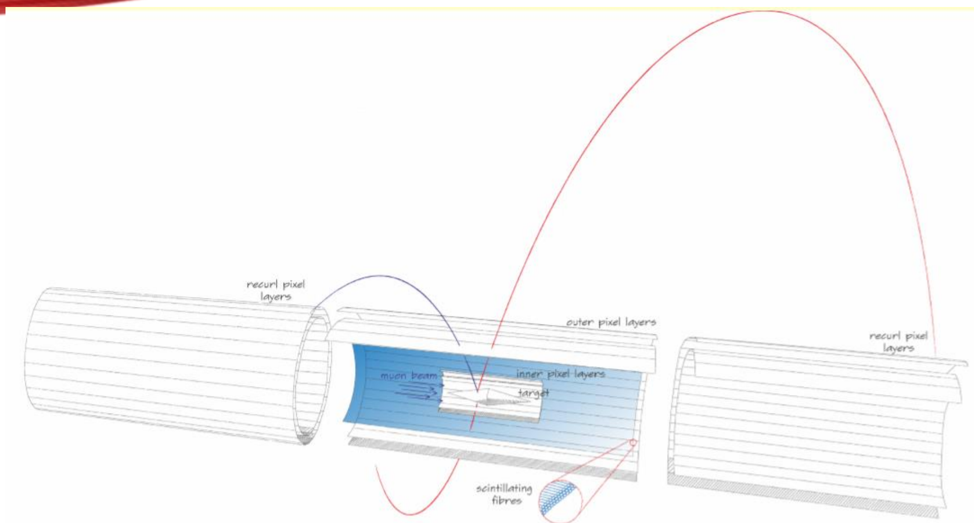
BR suppressed by $$\propto \frac{(\Delta m_\nu^2)^2}{m_W^4} \approx 10^{-50}$$

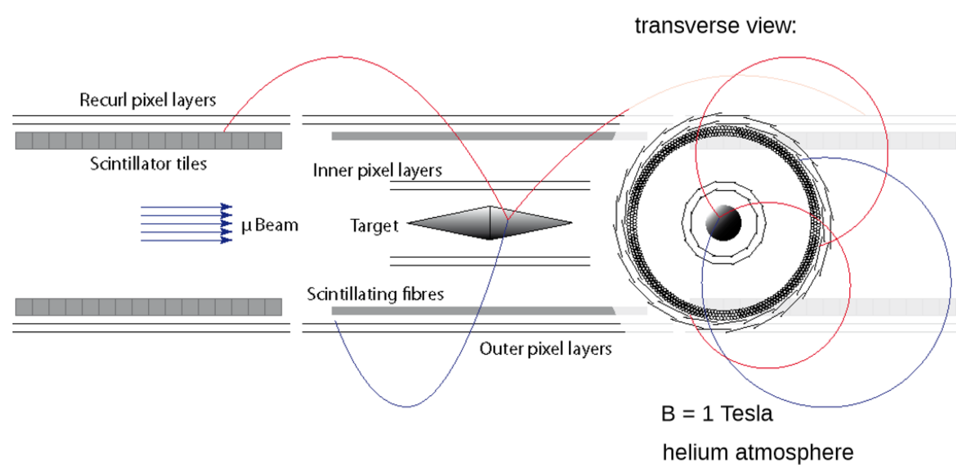
Mu3e experiment

- University of Geneva (CH)
- University Heidelberg (D)
- Karlsruhe Institute of Technology (D)
- University Mainz (D)
- Paul Scherrer Institute (CH)
- ETH Zurich (CH)
- University Zurich (CH)

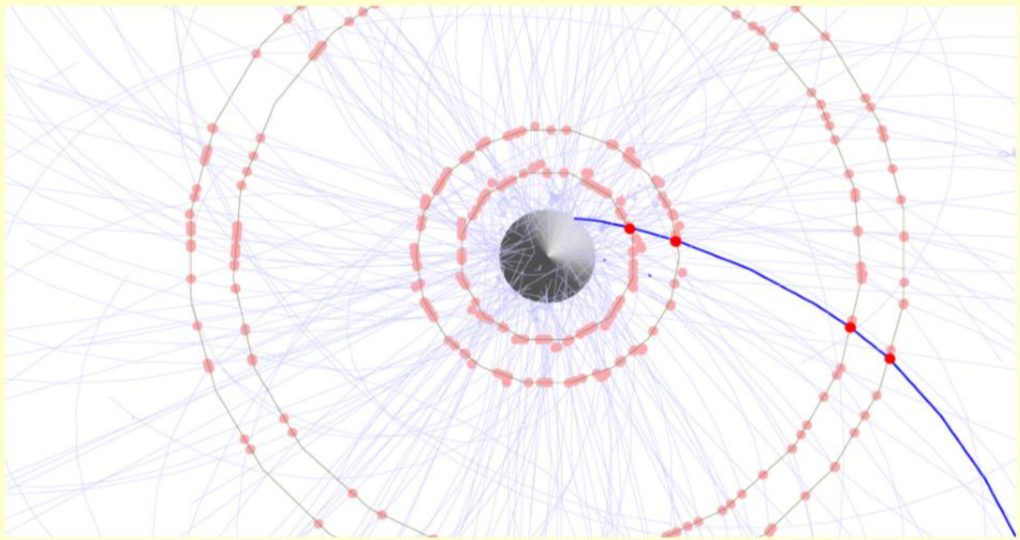
Several UK institutes interested to join
- Bristol
- Liverpool
- Oxford
- UC London

André Schöning, Heidelberg (PI) 86 CERN Detector Seminar, March 31, 201


recurl pixel layers
outer pixel layers
recurl pixel layers
muon beam
inner pixel layers
target
scintillating fibres


transverse view:
Recurl pixel layers
Scintillator tiles
Inner pixel layers
μ Beam
Target
Scintillating fibres
Outer pixel layers
B = 1 Tesla
helium atmosphere

Tracks in Pixel Detector



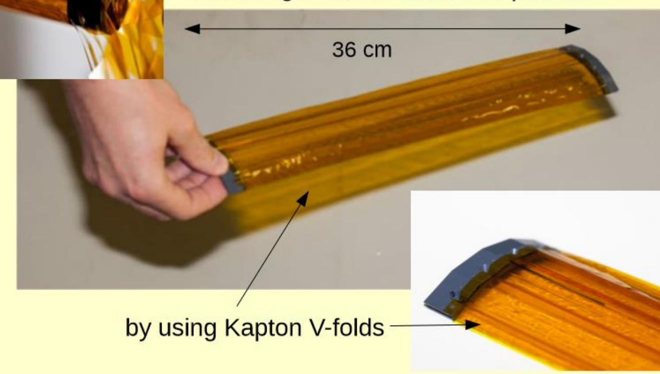
→ **additional timing detectors needed < 1ns**

André Schöning, Heidelberg (PI) 72 CERN Detector Seminar, March 31, 201

Ultra-thin mechanical mockup:

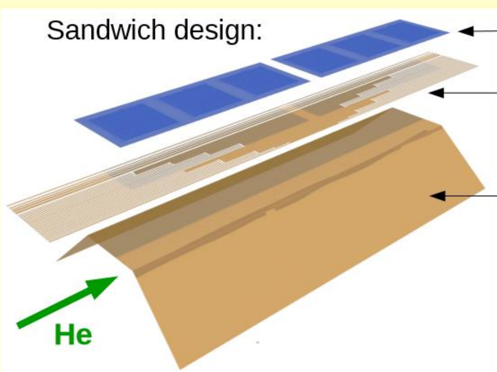
- sandwich of 25 µm Kapton®
- here 50 µm glass (instead of Si)

Even larger stable structures possible



Mu3e physics sensitivity: ~ $(X/X_0)^3$

Most challenging requirement: $X/X_0 \leq 0.1\%$



monolithic HV-CMOS sensor (50 µm)

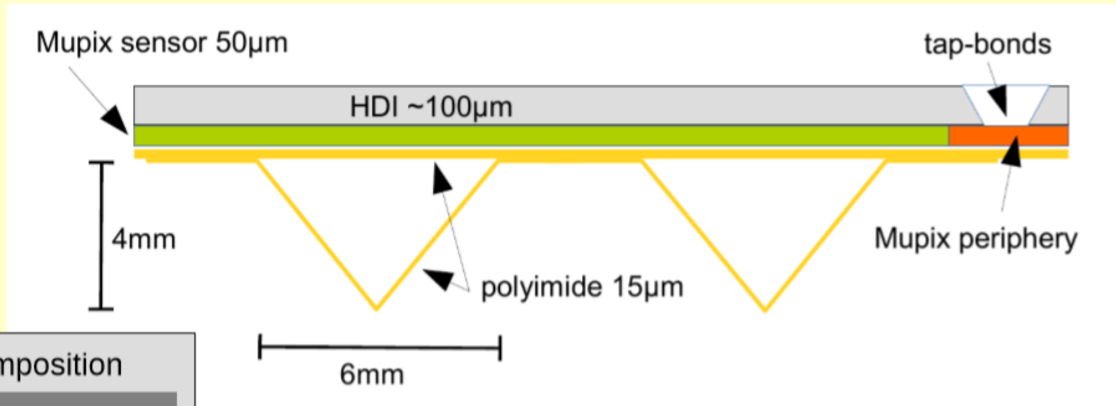
thin aluminium / kapton flexprint

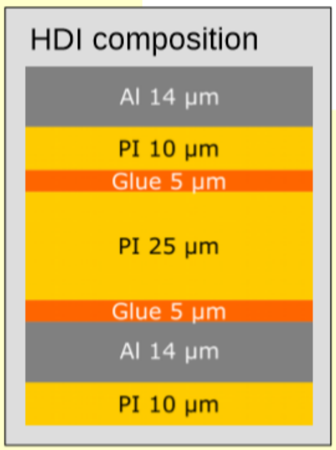
kapton support foil (25 µm)

+ gaseous helium cooling

$X \sim 0.1\%\ X_0$ per layer possible

Ultralight Pixel Ladder



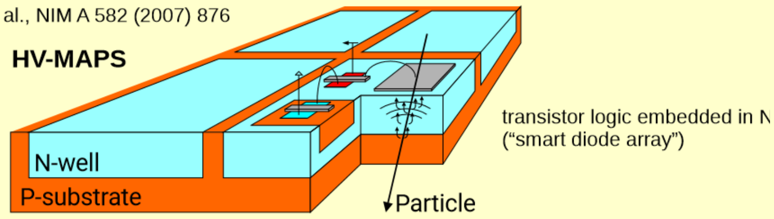


	Layer 1-2		Layer 3-4	
	thickness [μm]	X/X_0	thickness [μm]	X/X_0
MuPix Si	45	$0.48 \cdot 10^{-3}$	45	$0.48 \cdot 10^{-3}$
MuPix Al	5	$0.06 \cdot 10^{-3}$	5	$0.06 \cdot 10^{-3}$
HDI polyimide & glue	45	$0.18 \cdot 10^{-3}$	45	$0.18 \cdot 10^{-3}$
HDI Al	28	$0.31 \cdot 10^{-3}$	28	$0.31 \cdot 10^{-3}$
polyimide support	25	$0.09 \cdot 10^{-3}$	≈ 30	$0.10 \cdot 10^{-3}$
adhesives	10	$0.03 \cdot 10^{-3}$	10	$0.03 \cdot 10^{-3}$
total	158	$1.15 \cdot 10^{-3}$	163	$1.16 \cdot 10^{-3}$

module: ~ 1 per mill radiation length

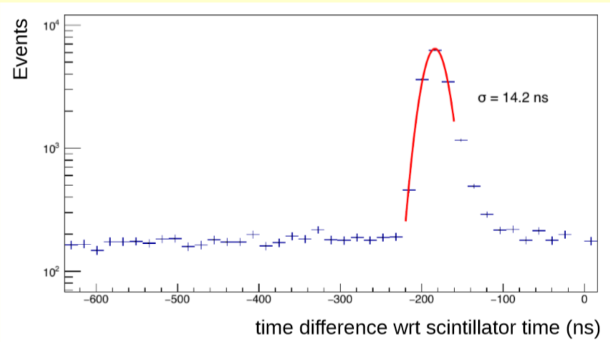
The MuPix Sensor for Mu3e

I.Peric, et al., NIM A 582 (2007) 876



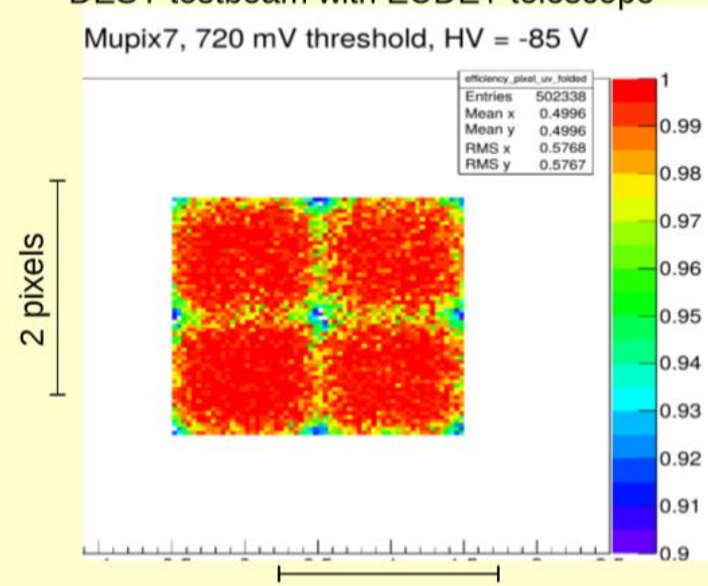
High Voltage - Monolithic Active Pixel Sensor (HV-MAPS)

- **active sensor → hit finding + digitisation + zero suppression + readou**
- high precision → pixels 80 x 80 μm^2
- low noise ~ 40 - 50e → low threshold
- small depletion region of ~ 10 μm → thin sensor ~50 μm (~ 0.0005 X_0)
- standard HV-CMOS process (60 - 90 V) → low production costs
- continuous and fast readout (serial link) → online reconstruction



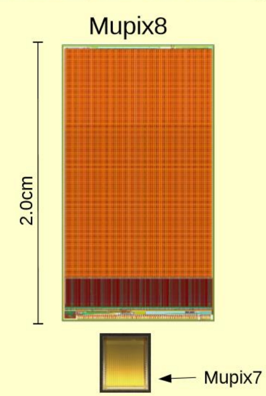
Mu3e requirement sigma (t) < 20 ns fulfilled

DESY testbeam with EUDET telescope



Mupix8 Prototype

Mupix8 submission in AMS HV-CMOS 180nm (chips expected mid April)
(Heidelberg, Karlsruhe, Mainz)



Features and improvements wrt Mupix7

- 31250 pixel of size 80 x 80 μm^2
- only 36 bond-pads per chip (+ test pads)
- four serial links a 1.25 Gbps
- two time walk correction schemes
  - 2-thresholds method
  - ToT with voltage ramp
- substrate: 80 Ωcm (before 20 Ωcm)
  - larger depletion
- current drivers for transmission lines
- some fixes and changes:
  (cross talk, state machine, no 2nd amplifier...)

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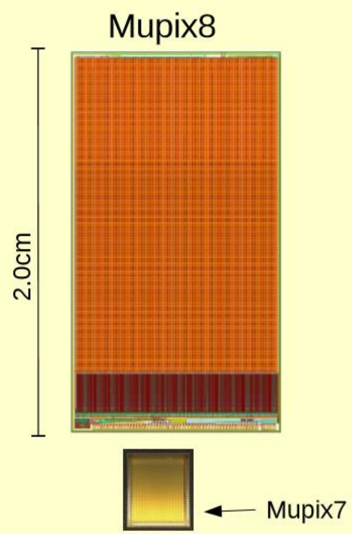

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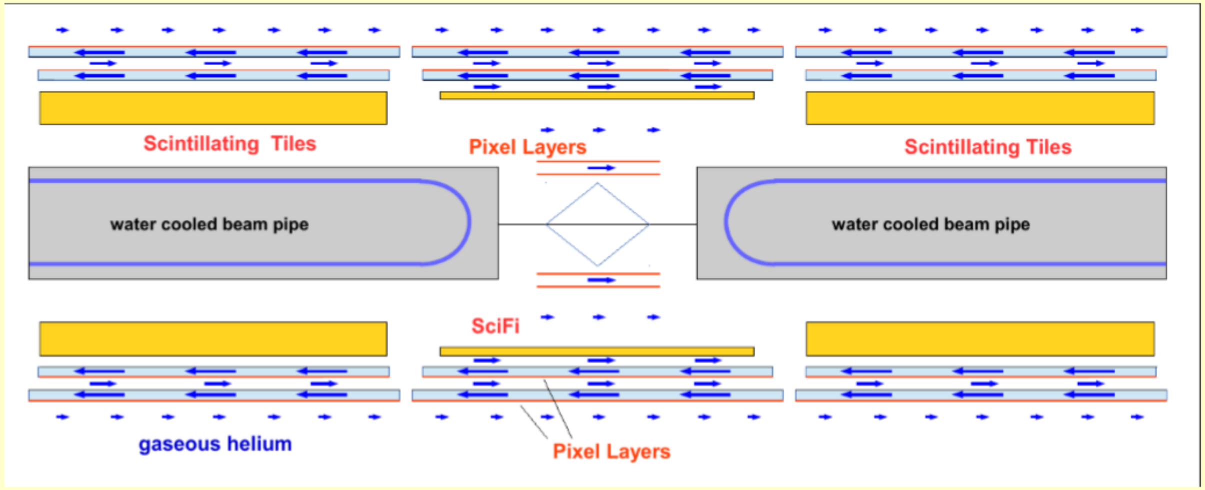
Mu3e Cooling System

Total Power Consumption: ~10 KW

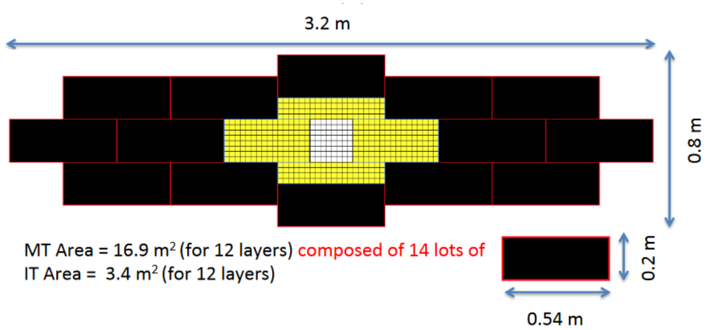
- **Water cooling** system around beam pipe: DC-DC converters, electronics (~5KW)
- Novel **Helium gas cooling** system: pixel tracker modules (~5KW)
  - He flow in V-folds (channels) up to 20 m/s
  - He flow in gaps between layers up to 5 m/s
  - global He-flow

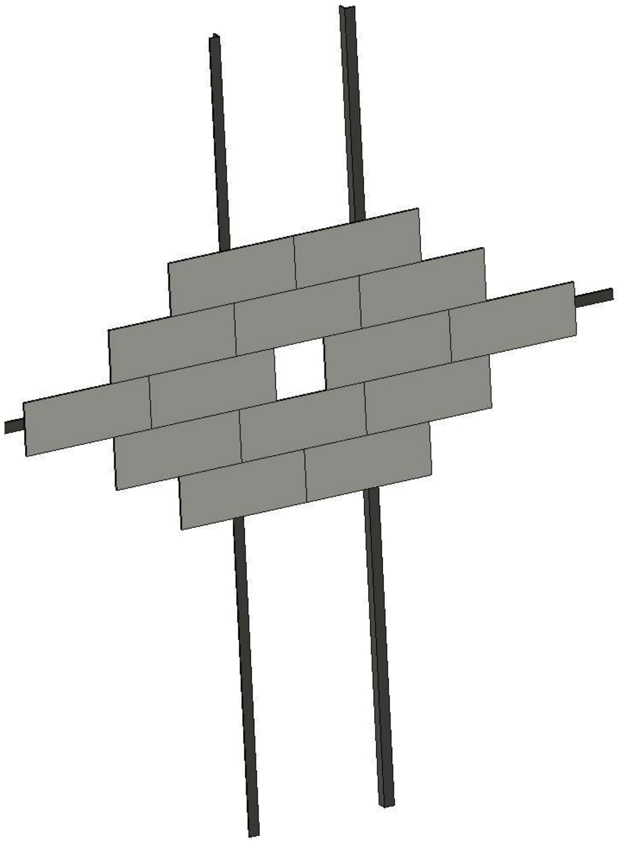


IT UPGRADE

- LHCb Upgrade
- Look at a tile that cools and supports an HVCMOS sensor
- Sensor and supplies

~0.1% X_0





IT UPGRADE

IT Occupancy plots from Greg Cizarek.

These plots are at inst. lumi 2x 10^{34}.

This was for a B sample

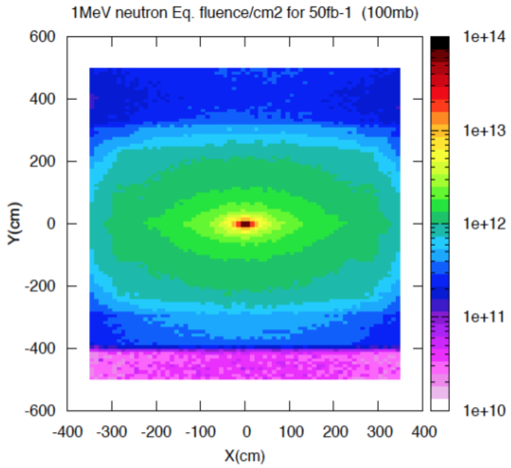


Figure 3.1: The expected 1-MeV neutron equivalent fluence per cm^2 at $z = 783$ cm after an integrated luminosity of 50 fb^{-1}.

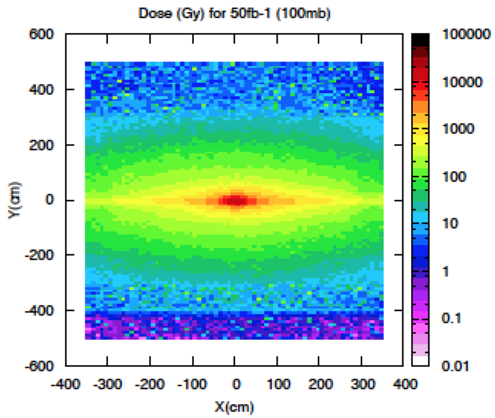


Figure 3.2: The expected dose in the $x - y$ plane at $z = 783$ cm after an integrated luminosity of 50 fb^{-1}.

IT UPGRADE

- Pixels e.g. 50 x 1000 micron (we can design this)
- ~0.05 Wcm^{-2}
- One “box” 25W (54 cm x 20 cm)
- One layer 150W
- Detector 1.8kW

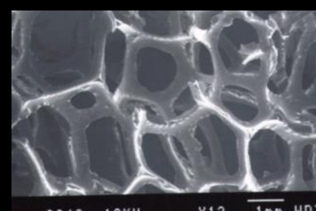
GASEOUS COOLING WITH LOW DENSITY CARBON FOAM

Tim Jones

May 2017

WHY USE AN OPEN CELL FOAM ?

- Open cell structure …
  - Breaks up flow and promotes turbulence
    - Turbulence increases the Reynolds number of the fluid flow and this increases the heat transfer coefficient, h
  - Increases the surface area
    - Provided the foam has a decent thermal conductivity, heat is conducted away from the walls of the channel and into the middle of the channel. Combined with the enhanced surface area, this improves the area available for convective heat transfer into the fluid.

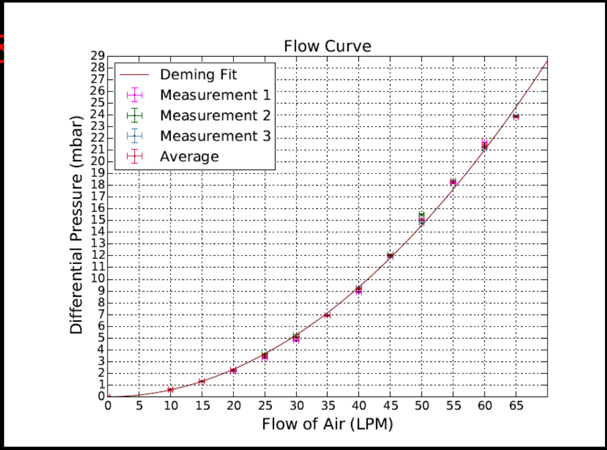


NB – these images are NOT a 130ppi foam!

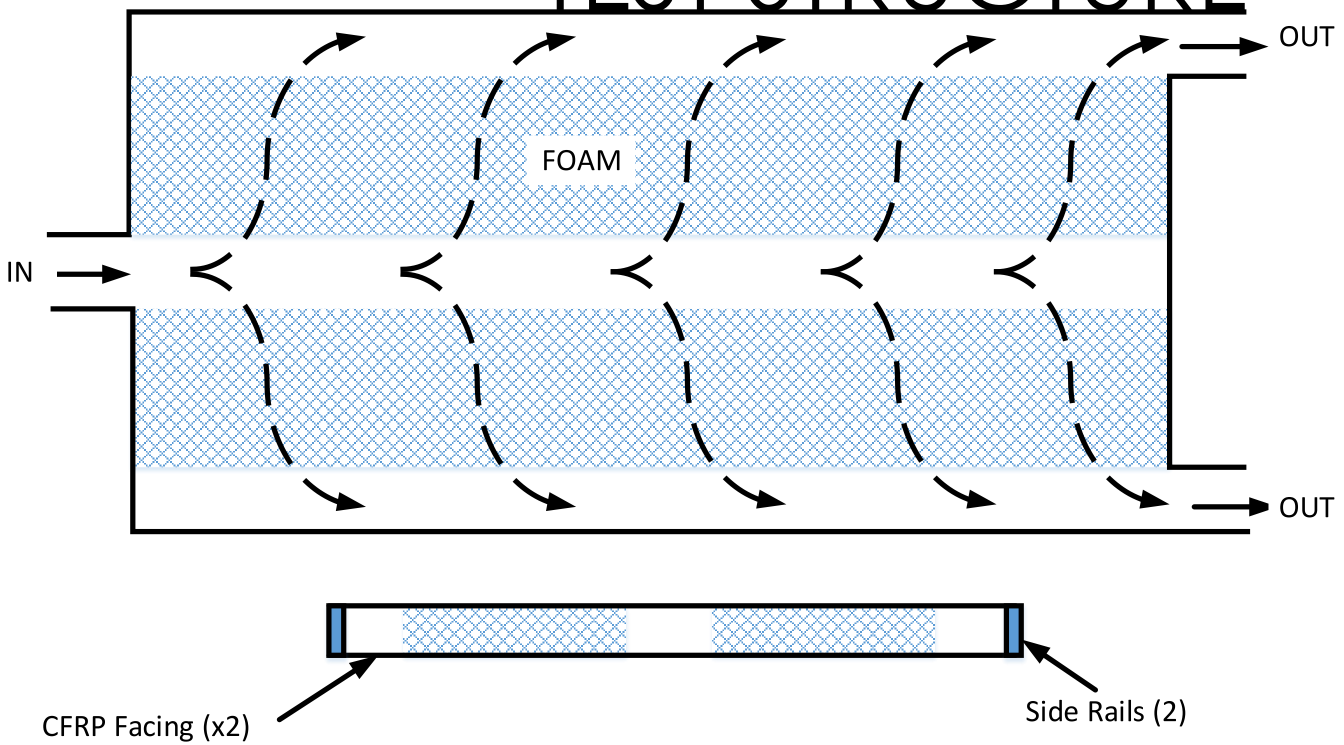
- Allcomp K9
  - K9 foam has 130 pores per inch (ppi) corresponding to a pore size of about 0.2mm
  - At a density of 0.23 g/cc, the average thermal conductivity of about 30 $W.m.k^{-1}$.

PREVIOUS STUDIES IN ATLAS

- Gas cooled stavelet (Tim Jones)
  - Studied thermal performance of a 50cm x 10cm x 0.5cm structure with 10 rectangular channels flushed with air, N_2 and helium
- Air-cooled CFoam test structure (Duco Bouter & Nigel Hessey)
  - Studied thermal performance of a test structure cooled by air passing through an open cell foam.
  - HTC ~ 370 $W.m^{-2}.K^{-1}$
- It was found that "the carbon foam solution is about 30% less radiation length and 25% less mass compared to the baseline CO_2"
- Measure at 0.05 W/cm^2 that with 50 litres per minute(!) air have only about 2°C increase in Si over gas
  - *We have built an LHCb prototype*

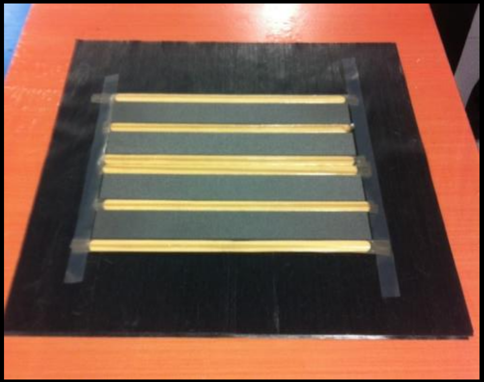


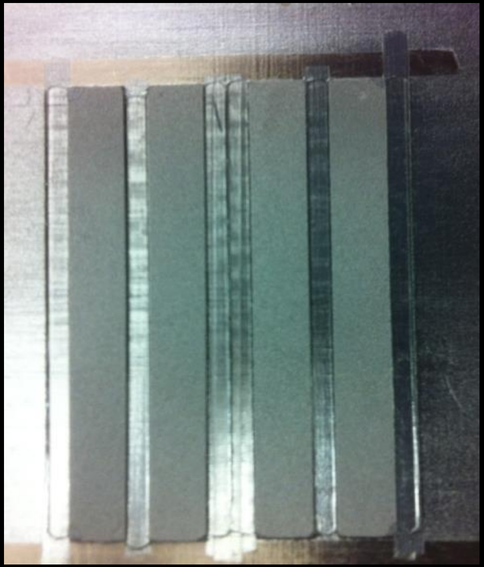
LIVERPOOL GAS-COOLED TEST STRUCTURE



CONSTRUCTION

- Co-curing
  - 3 layers (30cm x 30cm) of K13C2U/EX-1515
  - 4 bars of Allcomp K9 foam (20 x 2.5 x 0.3 cm)
  - Cure under 6 bar pressure and 121 deg C for 3 hours





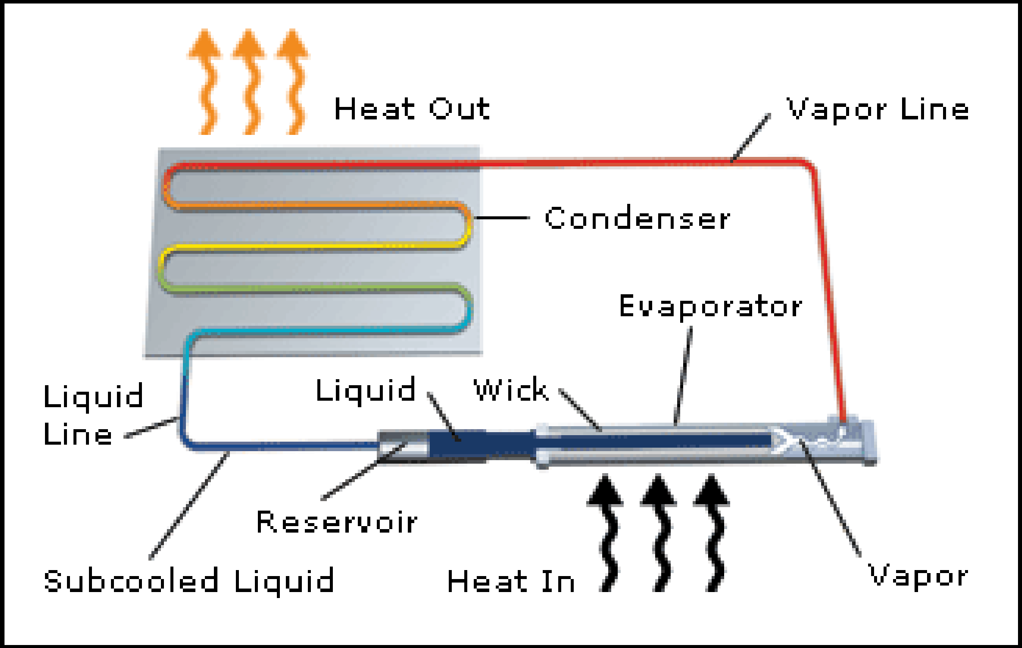
IT PROTOTYPE

- If this works m ~ $0.5 g/cm^2$
  - i.e. 1%
- Realistically (maybe!) can get down to 0.5% (thinner CF, end pieces, slightly different foam)

HEAT PIPES

From space: vacuum compatible

Considered for VELO I



- Flexible and flex fatigue resistance (tested to more than 7.5 million flex cycles)
- Resists gravity loads (9g-capable), shock, vibration, freeze and thaw
- Versatile heat load capabilities (for dissipating a few watts or many kW)
- Passive (and under partial vacuum)
- Approx 10000x conductivity of Cu.
- -250C to +1000C
- Low mass designs possible. 2 x 6 mm pipes carry O(30W)

SUMMARY: HVCMOS &TECHNOLOGIES

- Exciting new possibilities
- Rad hard and thickness, performance suitable for IT
- New/existing cooling and mechanical techniques promise possibility to build