Status of the R&D for the NUMEN experiment

D. Lo Presti

for the NUMEN Project

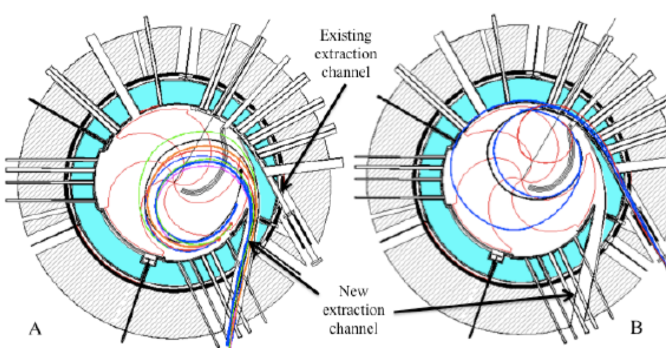
Overview

- *Upgrade of the CS and MAGNEX spectrometer*
- *New beam lines for NUMEN*
- *MAGNEX Focal Plane Detector*
- *Upgrade of Focal Plane Detector for NUMEN*
- *R&D activities*
- *Conclusions*

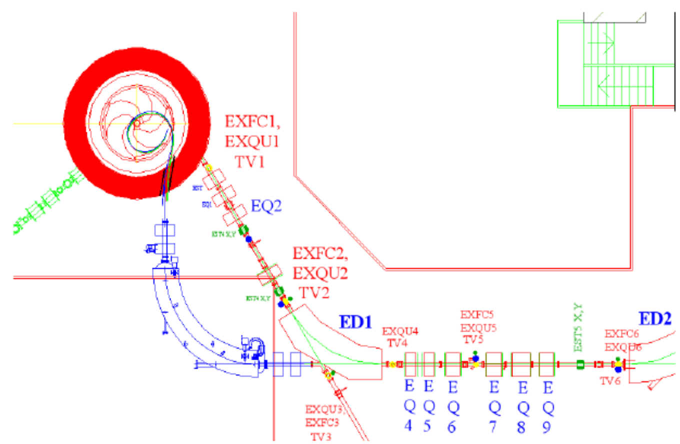
Upgrade of the CS accelerator and MAGNEX spectrometer

Motivations

- The LNS set-up is today an ideal one for the research objectives of NUMEN even at a worldwide perspective.
- However, a main limitation on the beam current delivered by the accelerator and the maximum rate accepted by the MAGNEX focal plane detector must be sensibly overcome in order to systematically provide accurate numbers to the neutrino physics community in all the studied cases.
- The upgrade of the LNS facilities in this view is part of this project.
- For a systematic study of the many “hot” cases of ββ decays an upgraded set-up, able to work with two orders of magnitude more current than the present, is thus necessary.
- The CS accelerator current (from 100 W to 5-10 kW);
- The beam transport line transmission efficiency to nearly 100%

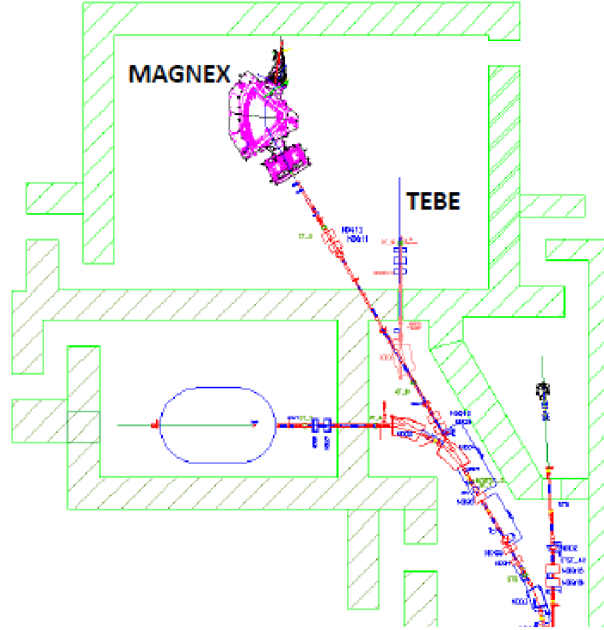


Extraction by stripping



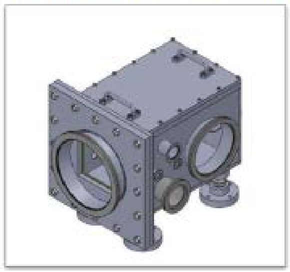
➢ (Poster 145 A. Russo)

Upgrades and new beam lines for NUMEN



- **TE**st **BE**am facility: (Poster 25 A. Russo)
  - Available of beams for short tests
  - low emittance beam line for test of tracking detectors
  - Working in parallel with MAGNEX activities

- Gas chamber (built at UNAM-Mexico) to be installed in **TE.BE.**




- Post-stripper study for the (^{20}Ne,^{20}O) double charge exchange reactions at zero degrees within the NUMEN experiment. (Poster 23 G. Santagati)
- Study and Design of the target for the NUMEN Experiment. (Poster 14 F. Pinna)
- New power supplies for the MAGNEX spectrometer (QD) to increase magnetic rigidity under NUMEN conditions
- Design of Beam Dump in MAGNEX hall
- …

MAGNEX Focal Plane Detector (FPD)

M.Cavallaro et al. EPJ A 48: 59 (2012)

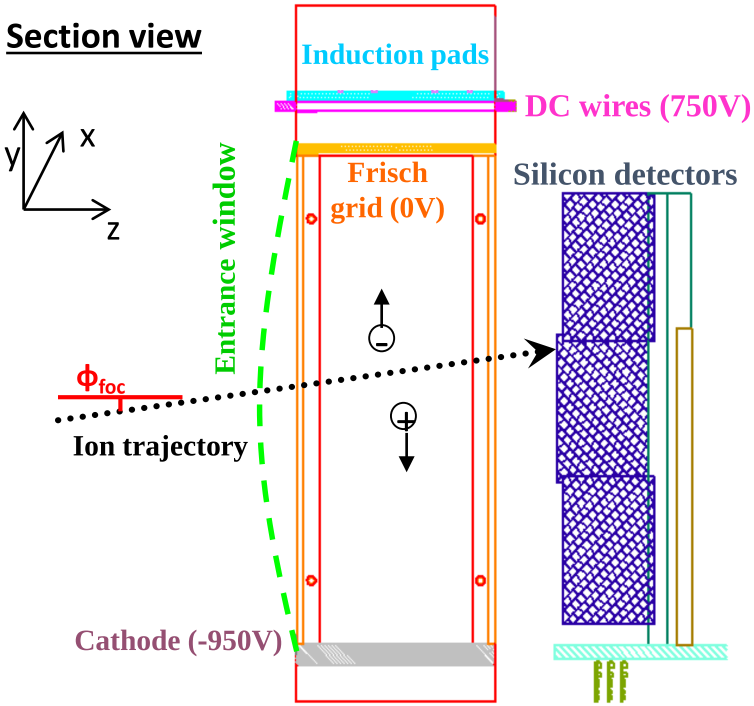
D.Carbone et al. EPJ A 48: 60 (2012)

Two tasks to accomplish:

1) High resolution measurements at the focal plane of the phase space parameters ($X_{foc}, Y_{foc}, \theta_{foc}, \phi_{foc}$)
2) Identification of the reaction ejectiles (Z,A) – crucial aspect for heavy ions

- **Gas-filled hybrid detector**
  Drift Chamber 1360mmx200mmx96mm,
  Pure isobutane pressure range: 10-100 mbar;
  600-1200 Volt, wires 20 micron
- **Wall Si** 500 and 1000μm - 20 columns x 3 rows

Section view



Ion Identification

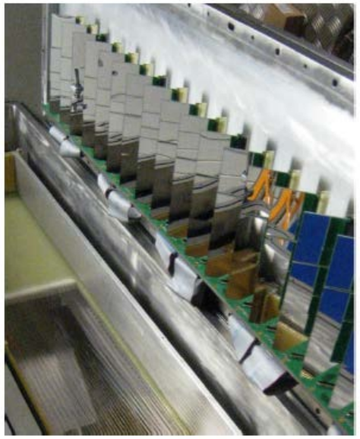
60 Silicon Detectors -> E_{res}

6 Proportional Wires -> ΔE

Ray Reconstruction

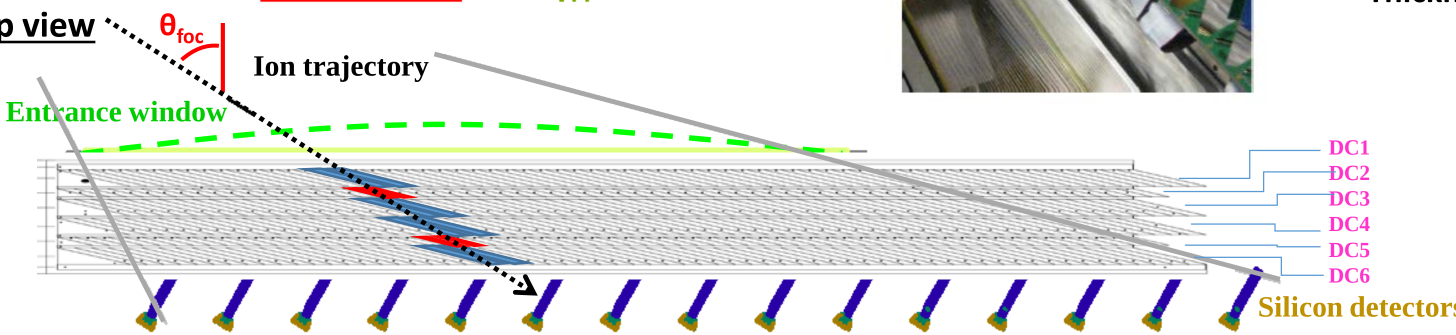
6 Induction Strip -> $X_1, X_2, X_3, X_4, X_5, X_6$ -> X_{foc}, θ_{foc}

6 Drift Chambers (DC) -> $Y_1, Y_2, Y_3, Y_4, Y_5, Y_6$ -> Y_{foc}, ϕ_{foc}



PID Wall of 60 Silicon detectors
7 X 5 cm² each
Covered area 100 X 20 cm²
Thickness 500 – 1000 μm

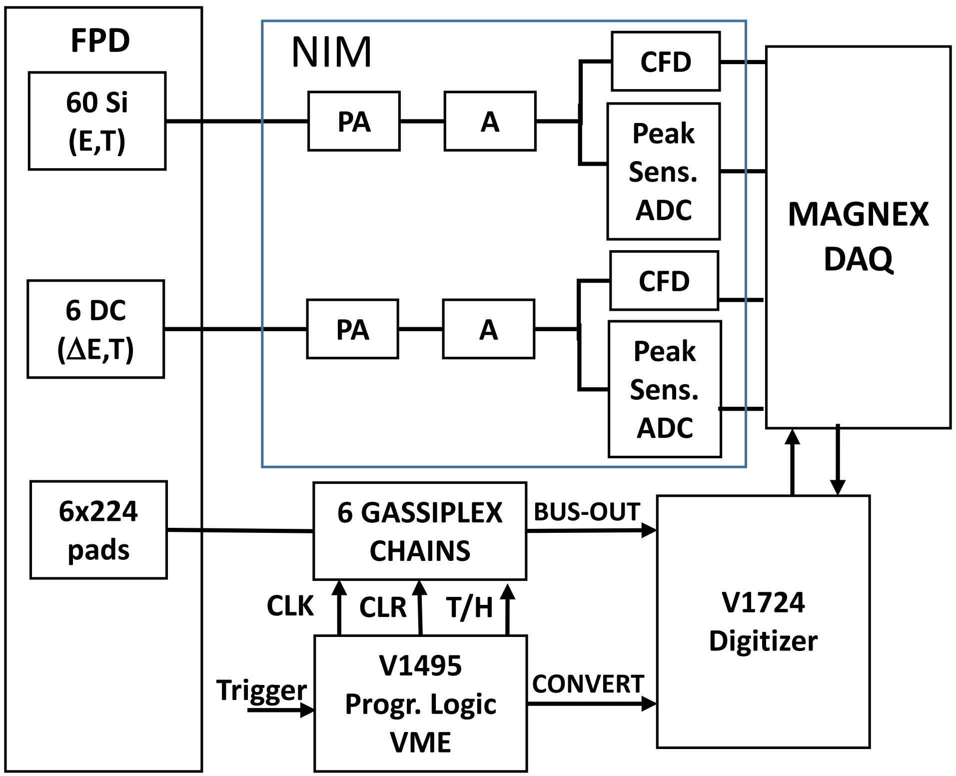
Top view



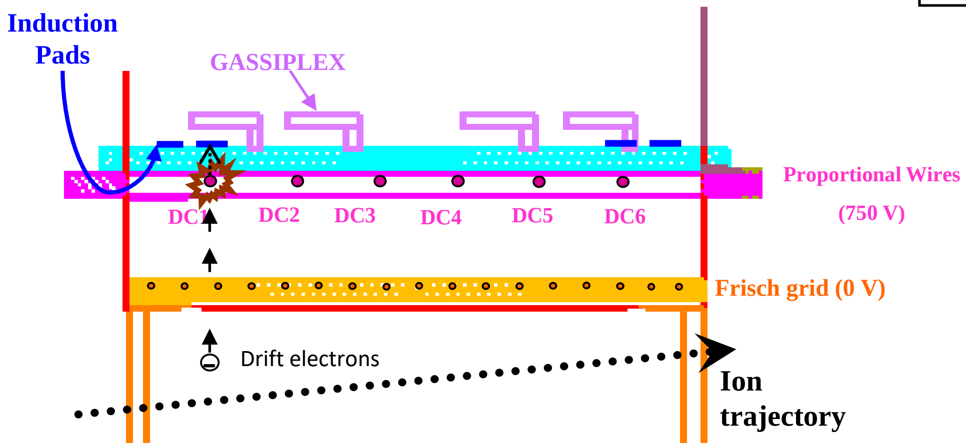
MAGNEX FPD Front-end and Read-Out (FE-RO) Electronics

- **Pads** read-out by **GASSIPLEX** chip (16 channel) in gas to reduce vacuum connectors.
- Each channel features a charge-sensitive amplifier, a switchable filter, a shaping amplifier and a track and hold circuit.
- Sequential analog output transfer -> 4 daisy-chained chips.
- **DC** signal pre-amplified and multiplexed at trigger.
- Digitization by **CAEN V1724** module.
- Analog signal are amplified and sampled by 14 bit 100 MS/s ADC.
- Digitized values transferred when over threshold.
- A **CAEN V1495 VME** programmable logic, externally triggered by a proper trigger signal from silicon and DC detectors (TRIGGER), controls the GASSIPLEX chips and ADC in order to perform the readout operations.
- Software pedestal calibration and data alignment.
- Influence of Front-End power dissipation on the gas.

MAGNEX readout schematic of the FPD.



Overall dead time (about 300 μs)



Upgrade of the Focal Plane Detector for NUMEN

Multiwire gas tracker and ΔE stage → Limited to 1-2 kHz

Wall of 60 Silicon detectors → Double-hit probability at 500 kHz > 30 %
Higher granularity needed
Radiation Hardness critical:
10^{14} ions/cm^2 in ten years of activity
Si detector dead @ 10^9 implanted ions/cm^2

Upgrade of detector and Electronics: (Full Custom Development)

Multiwire gas tracker ------ Gas Tracker based on micro-pattern (No ΔE)
GEM/THGEM (Talk Marco CORTESI Sat 10:30)

7x5 cm^2 silicon pad wall ------ SiC Telescope wall (ΔE+E)
Higher granularity and radiation hard

500 kHz

GASSIPLEX front-end + CAEN Digitizers ------ VMM ASIC (front-end + digitizer)
System on Module (SOM) for fast read-out
Use of the same FE-RO chain for all the detectors

Redesigned Segmented Anode ------ Digital Tracking + Time + ΔE (VMM)
1500 channel Tracker+ 2000 channel PID wall

- Gamma calorimeter: study and scintillator read-out test - IFUSP – San Paolo to separate DCE cascade gamma rays (Talk J.R.B. De Oliveira Thu 15:30)

Upgrade of detector: Backup R&D

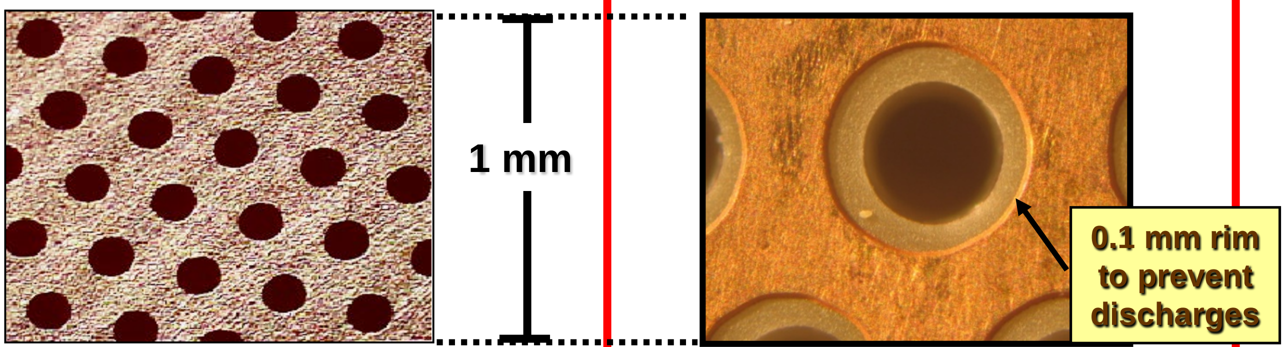
- Scintillating Gas + SiPM based Tracker (Poster 7 G. Gallo)
- Phoswitch based PID wall

Thick-Gas Electron Multiplier (THGEM)

Manufactured by standard PCB techniques of precise drilling in G-10/FR-4 (and other materials) and Cu etching → **Simple & Robust**

STANDARD GEM
10^3 GAIN IN SINGLE GEM

THGEM
10^5 gain in single-THGEM



THGEM geometry:
-) Thickness = 0.6 mm
-) Hole Ø = 0.5 mm
-) Hole Pitch = 1 mm

- **Effective single-electron detection**
- **High gas gain ~10^5 (>10^6) @ single (double) THGEM**
- **Few-ns RMS time resolution**
- **Sub-mm position resolution**
- **MHz/mm^2 rate capability**
- **Cryogenic operation: OK**
- **Gas: molecular and noble gases**
- **Pressure: 1mbar - few bar**
- **Reduced ion feedback**
- **No need for operation in clean room**

L. Periale et al., NIM A478 (2002) 377
P. Jeanneret, PhD thesis, Neuchatel U., 2001
P.S. Barbeau et al, IEEE NS50 (2003) 1285
R. Chechik et al., NIMA 535 (2004) 303

Dr. Marco CORTESI on **21 Oct 2017**
from **10:30** to **11:00**

PID requirements for NUMEN

Target
- ✓ p-n junctions
- ✓ Schottky diodes

- ✓ 1x1 cm² ΔE-E telescope
- ✓ thickness of ΔE stage 100 μm
- ✓ thickness of E stage 500-1000 μm

- Wide bandgap (3.3eV)

⇒ It has much lower leakage current than silicon

- Signal (**for MIP !**):

Diamond	36 e/μm
SiC	51 e/μm
Si	89 e/μm

⇒ It has more charge than diamond Si/SiC≈2

- Higher displacement than threshold silicon

⇒ radiation harder than silicon

SiC detectors

Tetrahedron of Carbon and Silicon atoms with strong bonds in the crystal lattice.

- Very hard and strong material!
- High degree of segmentation to avoid double hit events

(Poster 27 G. Litrico)

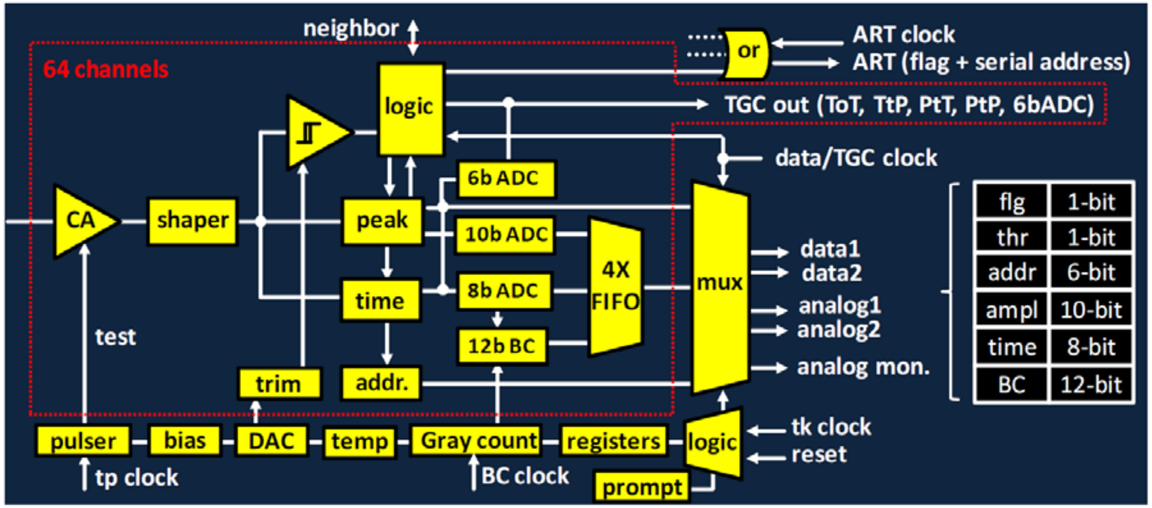
- The Schottky diodes are fabricated by epitaxy onto high-purity 4H–SiC n-type substrate.
- Challenges in the growth of bulk SiC: to grow large single crystals in large quantities is a problem (Defects in SiC)

SiCILIA

Silicon **C**arbide Detectors

- **Technological Challenge!**

FRONT-END Electronics
VMM chip - Brookhaven National Laboratories



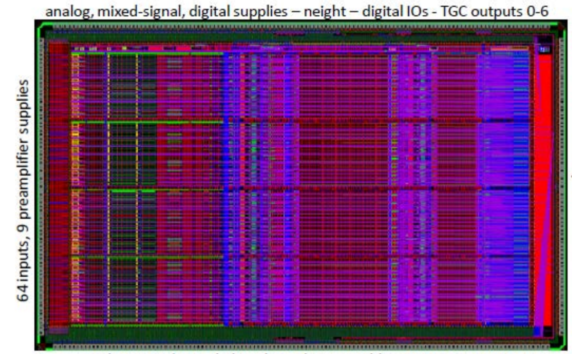
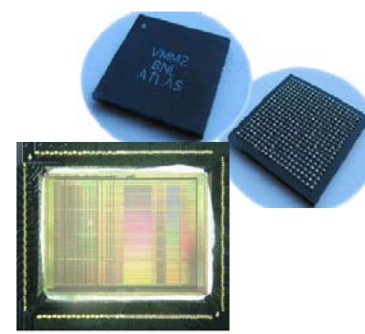


Fig. 2 – Physical layout of VMM2, size 13.5×8.4 mm² pad count 392.

130nm 1.2V 8-metal
CMOS technology from IBM

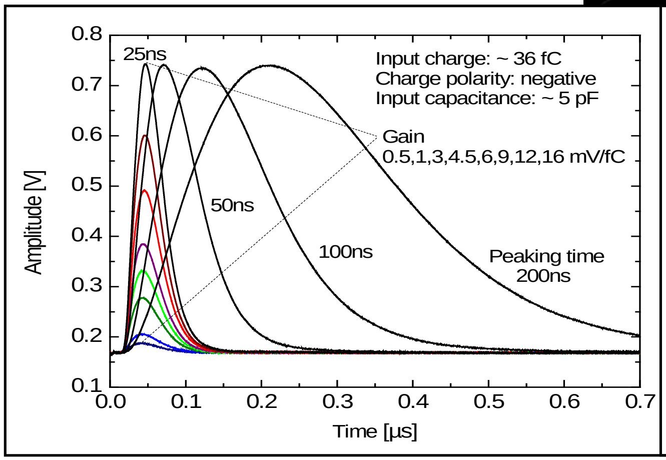
- **<u>64 linear front-end channels</u>:**
- low-noise charge amplifier (CA) with adaptive feedback;
- test capacitor and pulse generator for calibration;
- adjustable polarity;
- optimized for a capacitance of 200pF and a peaking time of 25 ns.
- third-order shaper (DDF) - <u>adjustable peaking time in four values (25, 50, 100, and 200 ns)</u>;
- Stabilized band-gap referenced baseline;
- <u>Gain adjustable in eight values (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC).</u>
- Many mode of operation, selected “<u>continuous digital</u>”:
  - **<u>38 bit generated for each event read-out @ about 200 MHz</u>;**
  - Id channel-peak amplitude (10b) - time stamp (10b);
  - 4-event deep de-randomizing FIFO per channel, read-out token ring;
  - 8 LVDS digital channel required for the read-out and control of the chip;
- <u>Power dissipation 4 mW per channel</u>.

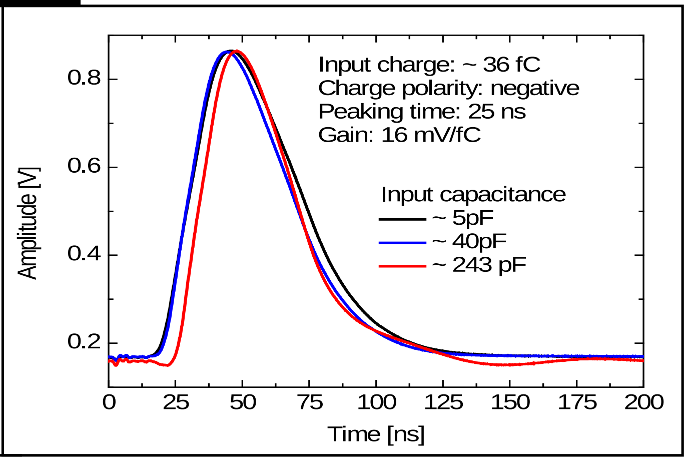


(Poster 19 D. Bongiovanni)

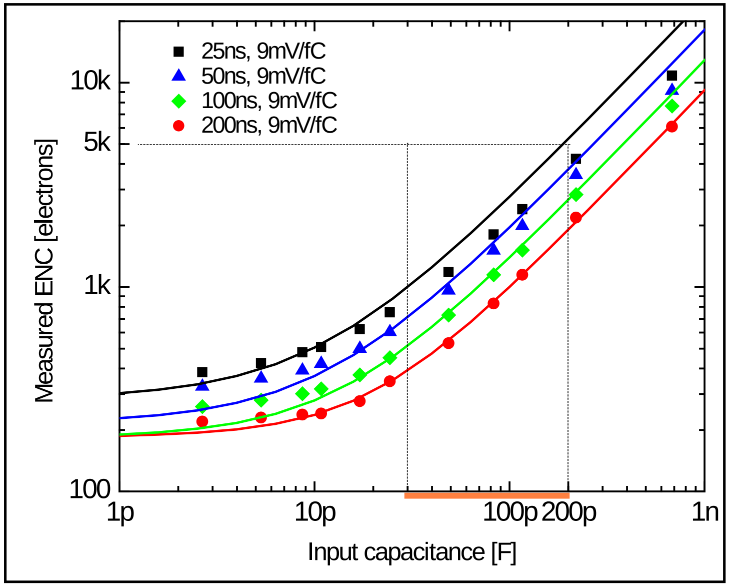
VMM Measured Pulse Response

- Suitable for different detector capacitances
- Wide range of measurement parameters
- Test pulse pattern embedded

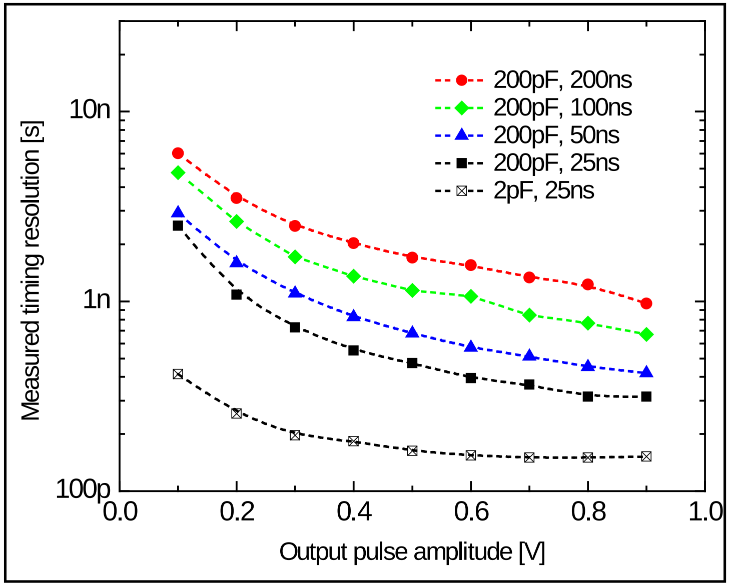




charge resolution



timing resolution

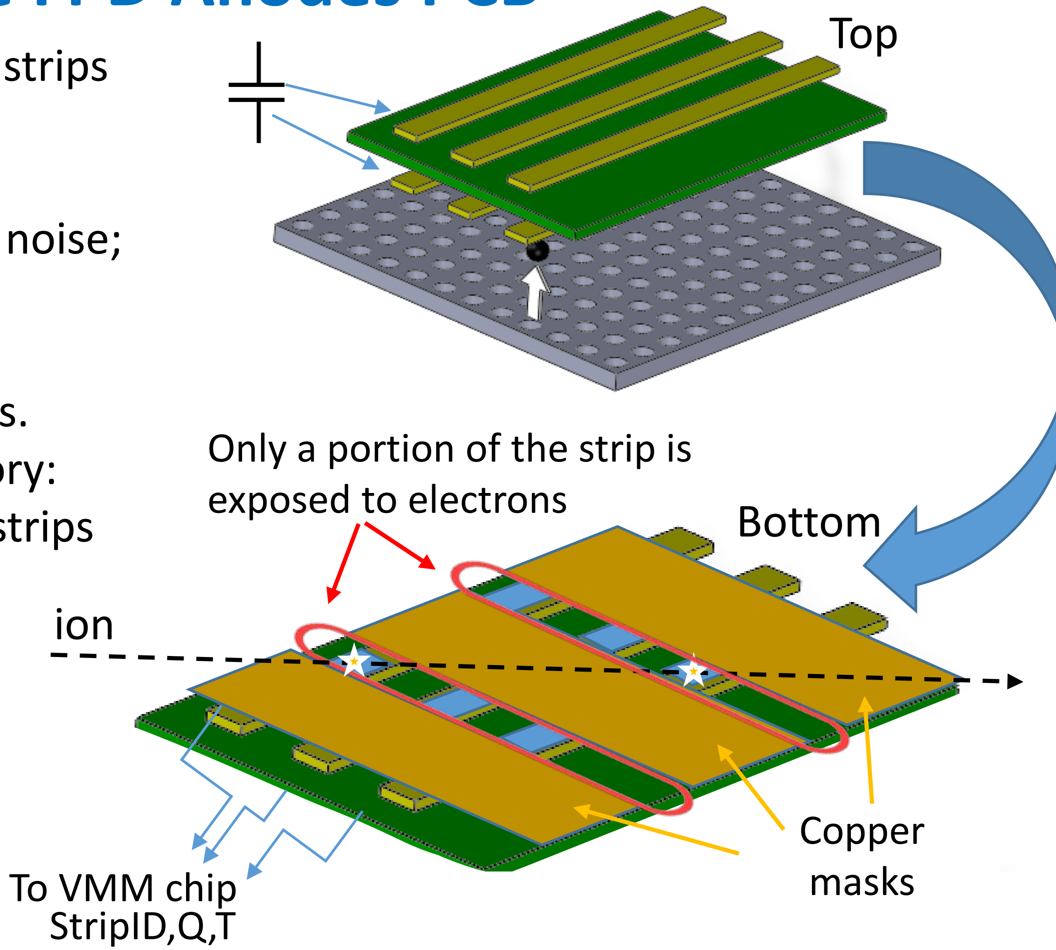


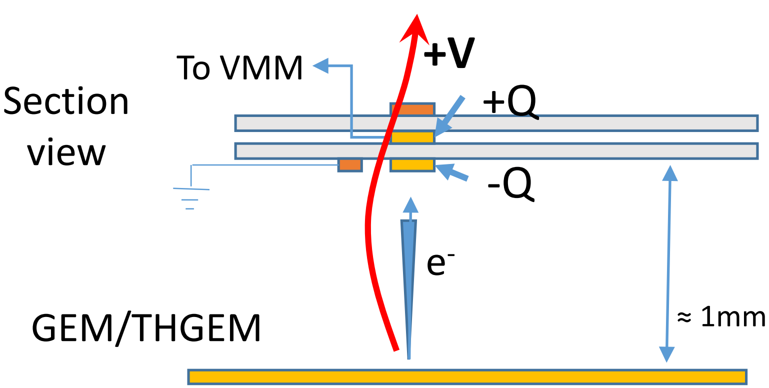
G. De Geronimo, in “Medical Imaging” by Iniewski

(Poster 19 D. Bongiovanni)

Design of the FPD Anodes PCB

- Two plane of 1500 capacitive-coupled strips (750 μm strip pitch)channels: time (<ns) and charge (8 bit)
- Low capacitance for high rate and low noise;
- Read-out by VMM;
- Modular (standard PCB technologies);
- Possible integration with THGEM in gas.
- Tracking by samples of the ion trajectory: 5 trenches orthogonal to the bottom strips

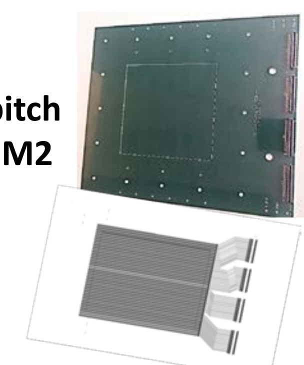




<u>**Poster 19 D. Bongiovanni**</u>

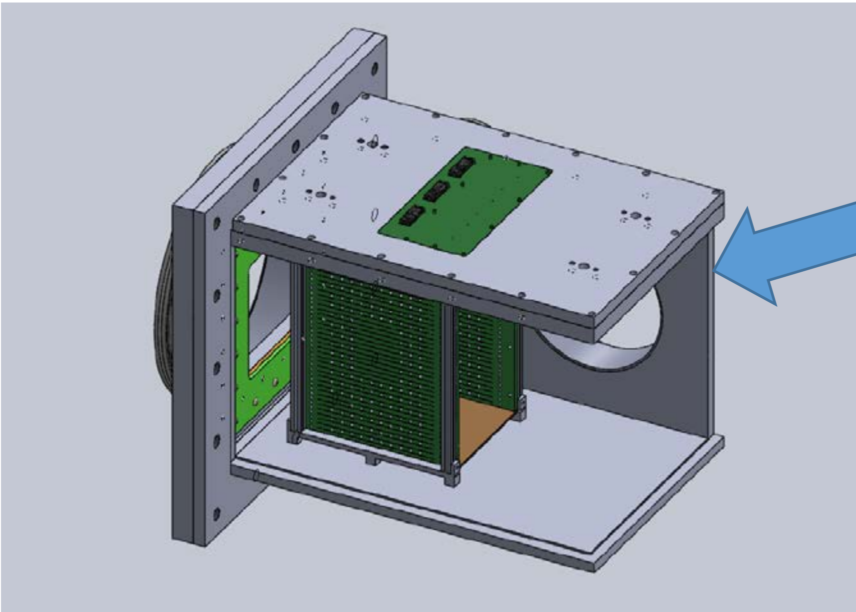
1° prototype 256 strip 500μm pitch

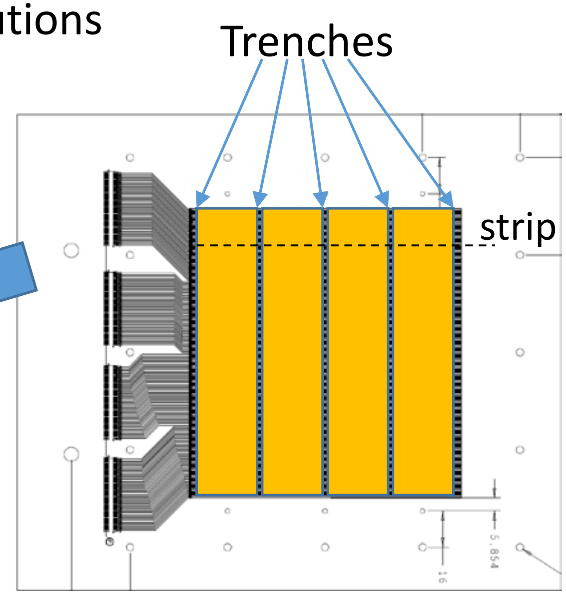
- **Tested in connection to VMM2 by internal pulser;**
- **Negligible cross-talk.**



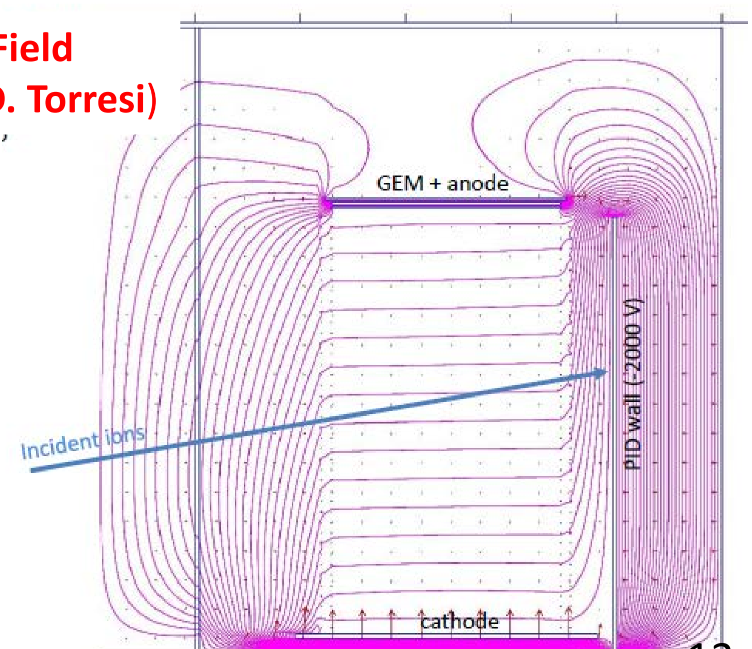
New Tracker prototype

Test Beam (**Te.Be.**) platform for the test of new solutions





Electric Field Simulation (D. Torresi)



- Choice of technologies scalable to full size detector;
- Minimization of FE-RO Electronics;
- No need for vacuum connector;
- Read-out Electronics in air;
- Minimization of Vacuum pollution;
- Optimization of the electric field;
- Easy of maintenance.

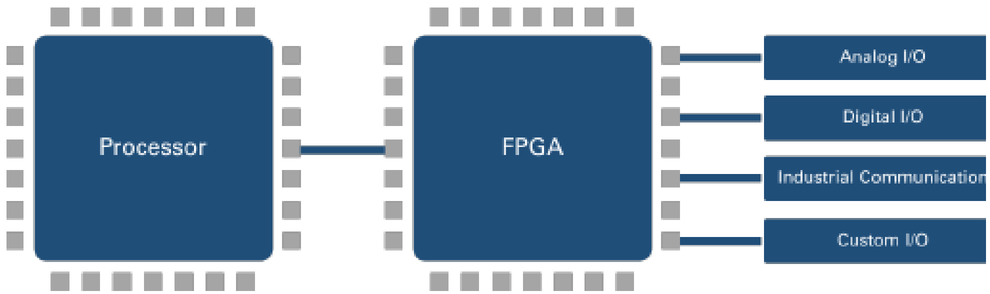
Poster 20 D. Bonanno

Poster 19 D. Bongiovanni

Read-out Electronics – System On Module

Read-out of VMMx chips will be performed by a SOM based board, custom designed for the experimental demands:

- Low Power;
- Radiation Tolerance;
- Low Cost;
- Re-configurability;



Processor SoC

Xilinx Zynq-7020
667 MH Dual-Core ARM Cortex-A9
Artix-7 FPGA Fabric

Size and Power

50.8mm x 78.2mm (2 in. X 3 in.)
Typical Power: 3 W to 5 W

Memory

Nonvolatile: 512 MB
DRAM: 512 MB

Operating Temperature

-40 °C to 85 °C Local Ambient

Re-programmable Intelligence on board for:

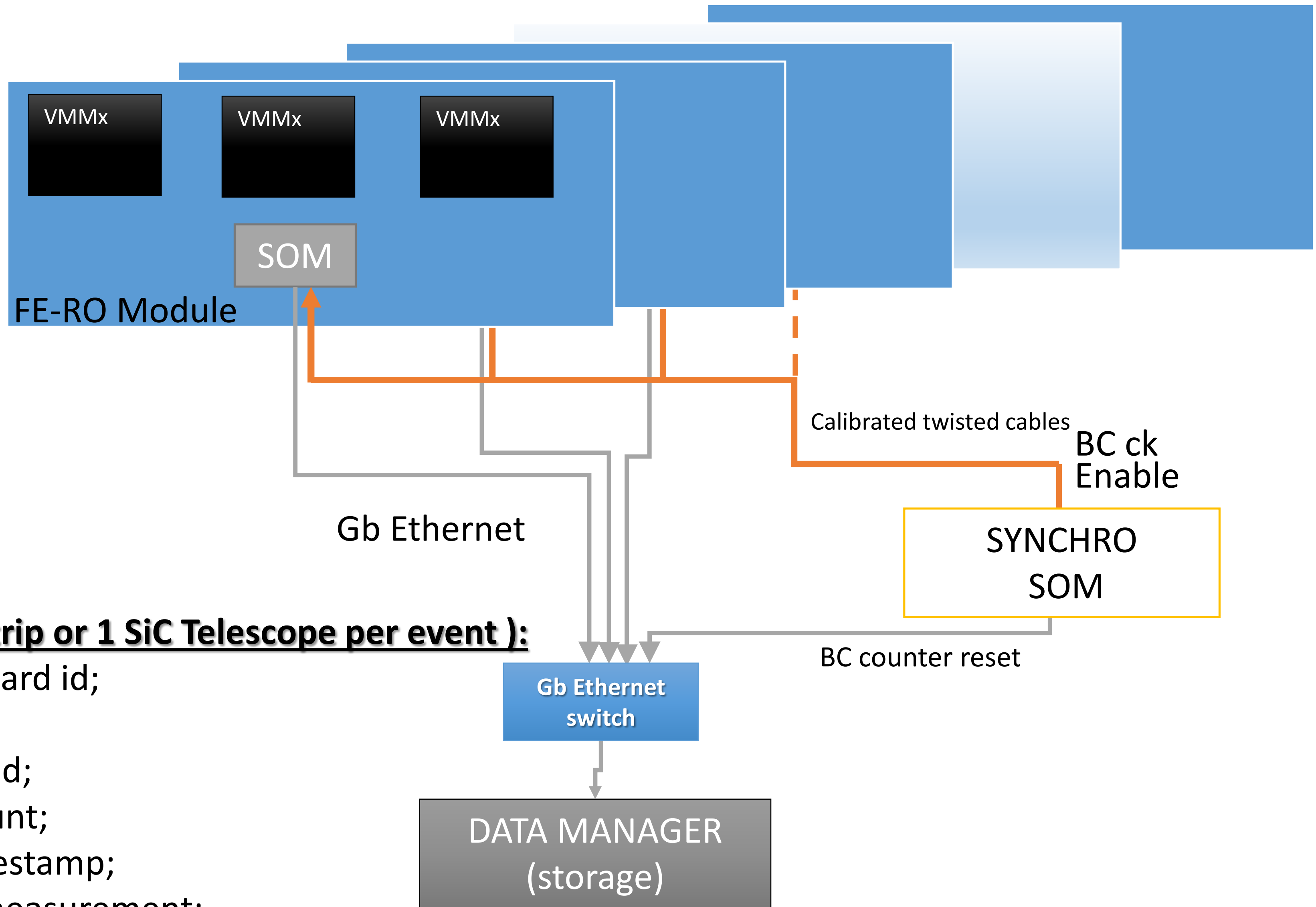
- composite trigger strategies;
- Slow control;
- Calibration;
- Overall synchronization;
- Gigabit Ethernet to maximize data throughput.

Poster 20 D. Bonanno

Dedicated Processor I/O
- Gigabit Ethernet
- USB Host
- USB Host/Device
- SDHC
- Serial TX/RX (console out)

FPGA I/O
- 16 SE fixed at 3.3V
- 144 SE/72 diff pairs with IO level selection
  - 3 Banks with user supplied voltage
- Configurable Peripherals: Gigabit Ethernet, RS232 x3, RS485 x2, CAN x2

FE-RO + DAQ Architecture



1 event
(Tracker 1 strip or 1 SiC Telescope per event):

- FE-RO Board id;
- Chip id;
- Channel id;
- BC ck count;
- Fine Timestamp;
- Charge measurement;

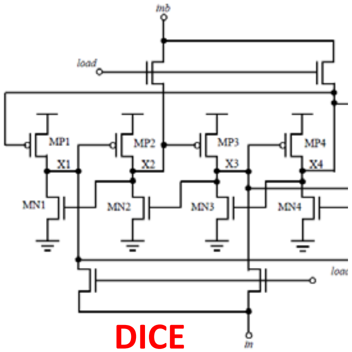
Poster 20 D. Bonanno

FE-RO Radiation Tolerance

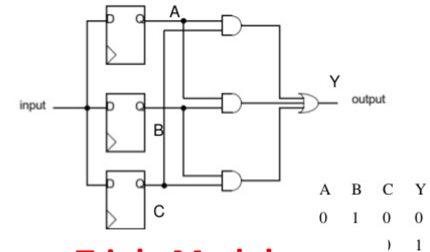
1. VMM Radiation Tolerance and SEU

To mitigate the SEU effects in the VMM storage elements two different techniques are used:

1. **Dual Interlocked Cells (DICE) for the protection of the configuration register;**
2. **The more common Triple Modular Redundancy (TMR) for the state machines and possibly the BCID register.**



DICE



Triple Modular Redundancy (TMR)

The first version of the VMM was tested in the NSCR Demokritos Tandem accelerator by ATLAS collaboration.
The VMM1 was irradiated in the area of the configuration registers for 44 h *n* of energy range 18-22 MeV achieving an integrated *n* flux of 3.1×10^{11} *n* cm^{-2}.
The measured cross-section found to be $(4.1\pm7) \times 10^{-14}$ cm^2/bit.
This shows a probability of 60 SEU/y/VMM2 for the NSW expected *n* flux.
Deep sub-micron technologies are known to be immune to much higher TID doses because of increasingly thinner oxide layers which can trap smaller amounts of charge.
Although not expected to be a problem, the VMM3 will be tested for TID tolerance in the ^{60}Co source irradiation facility at BNL.

2. SOM Radiation Tolerance and SEU

No Data available for SOM by National Instruments. First measurements in November 2017 at São Paulo.

ITER (International Thermonuclear Experimental Reactor) Guidelines

Expected Gamma Radiation Effects

- For the system and individual components, at what dose level is there;
- Degradation in analog signal performance;
- Partial and/or temporary functional failures;
- Permanent failure

Expected Neutron Radiation Effects

- Corrupt data in the SRAM or other memory of a CPU or ADC board;
- Hang-up of the CPU or ADC board requiring a reboot;
- Corrupt configurations in FPGA or other programmable devices requiring reconfiguration to continue operation;
- Permanent failure.

Conclusions

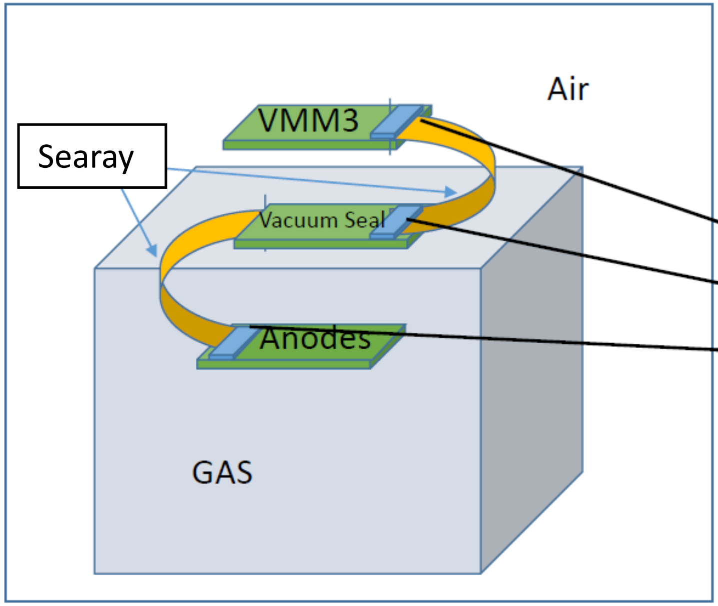
- Leading R&D:
  - Construction of the FPD prototype (end of 2017):
    - 3 VMM3 FE-RO Module final design (Poster 19 D. Bongiovanni)(Poster 20 D. Bonanno)
  - Validation of the FPD tracker design @TE.BE.:
    - Pitch, capacitance and interconnections;
    - (Vacuum sealing,…)
    - GEM/THGEM (Talk M. Cortesi Saturday 10:30)
    - Electric Field simulation and optimization
    - SiC PID wall - SICILIA (Poster 27 G. Litrico)
  - New Beam lines for NUMEN experiments at INFN-LNS (Poster 25 A. Russo)
  - Post-stripper study for the (^{20}Ne,^{20}O) double charge exchange reactions at zero degrees within the NUMEN experiment (Poster 23 G. Santagati)
  - Overview on the Study and Design of the target for the NUMEN Experiment (Poster 14 F. Pinna)
- Gamma Wall spectrometer development (Talk J.R.B. De Oliveira Thursday 15:30)
- Test of radiation tolerance for FE-RO electronics (Nov. 2017)
- Backup R&D in progress:
    - Optical Tracking FPD (Poster 7 G. Gallo)
    - Phoswitch PID

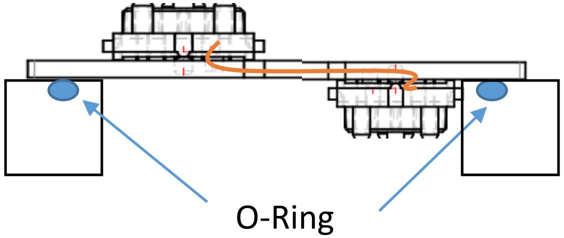
Thank you

Contacts
Domenico.lopresti@ct.infn.it
Skype: Domenico.Lo.Presti

Scheme of connections

- No need for vacuum connectors;
- Ease of installation;
- Same solution for all the FPD detectors;

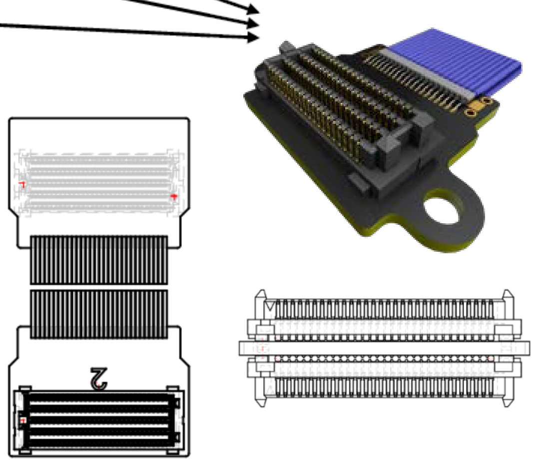




0.80 mm SAMTEC SEARAY™ High-Speed/High-Density Array Micro Coax Cable Assembly

Features

- 0.80 mm (.0315") pitch
- Eight and ten rows
- 50 ohm single-ended signal routing
- 34 AWG micro ribbon coax cable
- Available up to 300 positions



FE-RO Architecture: some numbers

- ***FE-RO Module***:
  - *3 VMMx chip -> 1 SOM*
  - *192 input -> 1 Gb/s Ethernet*
  - *If 0.75 mm pad -> 1.44 MHz max event rate per Module;*
  - *38 bit/event+ 5 bit (id chip and id Module) *number of strips involved * number of layers= 43 bit/event*3*5=645 bit*

    (plus id chip and id Module);
  - *Max Data Throughput = 0.929 Gb/s per Module;*
- ***Timing strategy***
  - *Synchro SOM:*
    - *BC clock to all Modules = 10 MHz;*
    - *Enable all Modules;*
  - *Each Module (SOM):*
    - *counts BC clock edges up to 4096 = 409.6 μs;*
  - *Each VMMx chip measures time from peak to next BC edge @ 488 ps resolution.*