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for the **FAZIA collaboration**

FAZIA electronics: from detectors to acquisition

GDS topical meeting
LNL, January 26th, 2017

Outlook

- Brief history of FAZIA
- FAZIA modular design
- Front-end electronics and block cards.
- Event building electronics
- Coupling with other detectors
- Acquisition and slow control
- Summary and Conclusions

Fazia project

The aim of the project

- Build a 4π **array** for charged particles.
- High **granularity** and good **energy resolution**.
- A **and** Z **identification** over the widest possible range.

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History of FAZIA

2007-16 **Prototypal telescope** tests were performed to design and build **FAZIA blocks**

2014 1 block (16 telescopes) successfully tested at *Laboratori Nazionali del Sud* (LNS) of INFN

2015-16 4 FAZIA blocks measured at LNS for two **physics-centered** experimental campaigns

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Present and future of FAZIA

2017 Two more **physics-centered** experiments are planned at LNS

2018 12 FAZIA blocks will be brought to GANIL and **coupled to INDRA**

20?? Adapted FAZIA blocks may be coupled with a gas detector to measure with **SPES beams**

Fazia project

Publications

- S. Barlini *et al*, Nucl. Instr. and Meth. A 600 (644–650), 2009
- L. Bardelli *et al*, Nucl. Instr. and Meth. A 654 (272–278), 2011
- S. Carboni *et al*, Nucl. Instr. and Meth. A 664 (251–263), 2012
- N. Le Neindre *et al*, Nucl. Instr. and Meth. A 701 (145–152), 2013
- S. Barlini *et al*, Nucl. Instr. and Meth. A 707 (89–98), 2013
- S. Barlini *et al*, Phys. Rev. C 87 (054607), 2013
- S. Piantelli *et al*, Phys. Rev. C 88 (064607), 2013
- R. Bougault *et al*, Eur. Phys. Jour. A 50 (47), 2014
- G. Pasquali *et al*, Eur. Phys. Jour. A 50 (86), 2014
- G. Pastore *et al*, submitted to NIM A, 2016

The FAZIA telescope

The telescope stages

1. 300 µm reverse-mounted Si detector;
2. 500 µm reverse-mounted Si detector;
3. 10 cm CsI(Tl) cristal read by a photodiode.

To achieve the best possible energy resolution and A and Z identification Si detectors come from a nTD ingot cut at random angle to avoid channeling effects.

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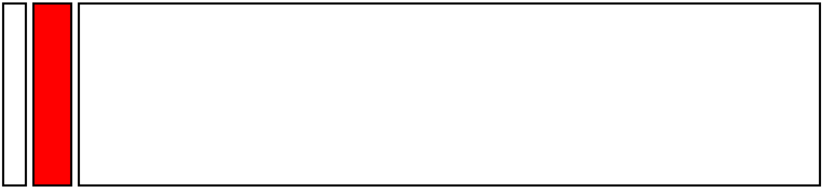

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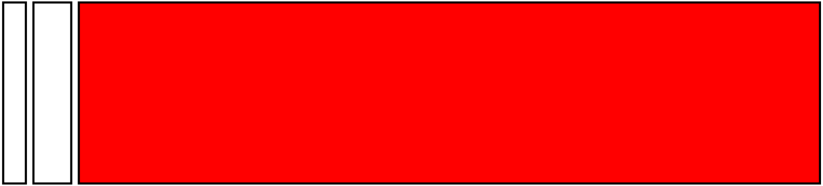
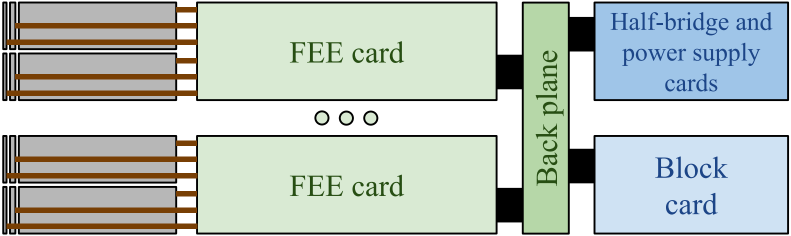


The FAZIA block

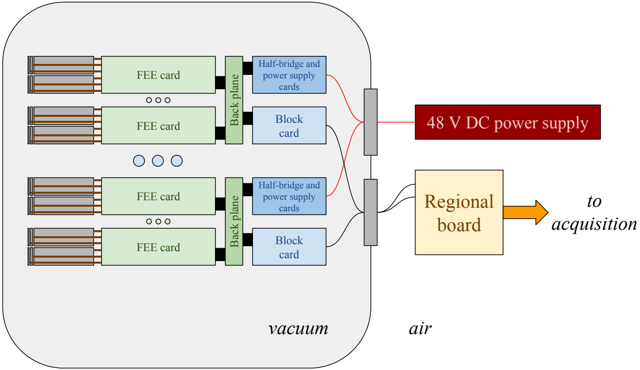
2 telescopes are connected to a FEE card.

The FAZIA block



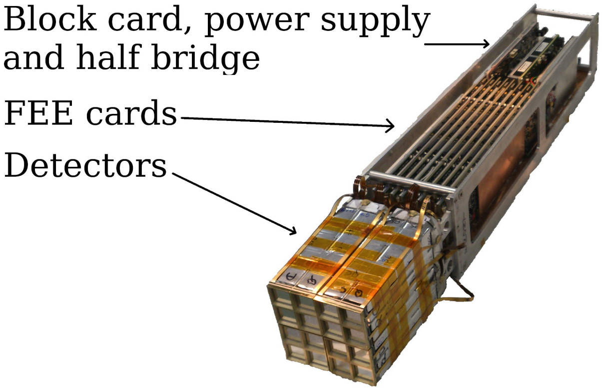
8 FEE cards are connected to a block card via a back plane.

The FAZIA block



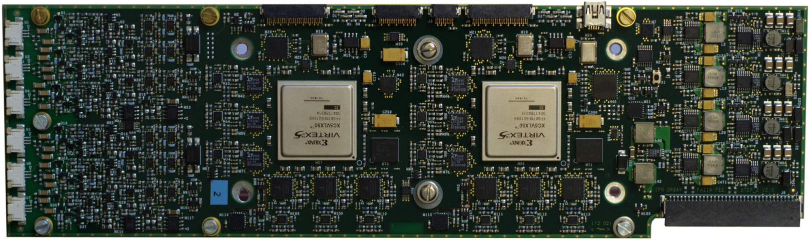
up to 36 block cards are connected to a regional board via a full duplex 3 Gb/s *optical link*

The FAZIA block



Block is mounted on a copper base in which water flows to provide cooling

Front-end electronics



FEE card

- Designed at IPN, Orsay
- 2 FAZIA telescopes per card
- Programmable logic performs on-line analysis of sampled data
  - VHDL code has been mainly written by P. Edelbruck
- FEE supplies also the Si detectors bias voltages

Front-end electronics

Detector connectors

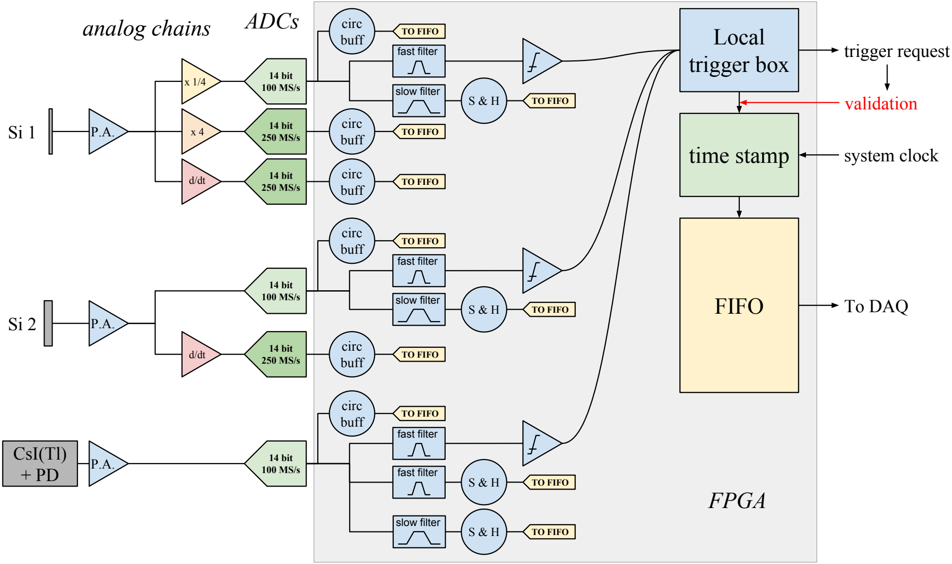
- Detectors are connected using kapton cables
- Silicon side kapton connection:
  - **ultra-sonic μbonding**
  - **conductive glue**

Front-end electronics

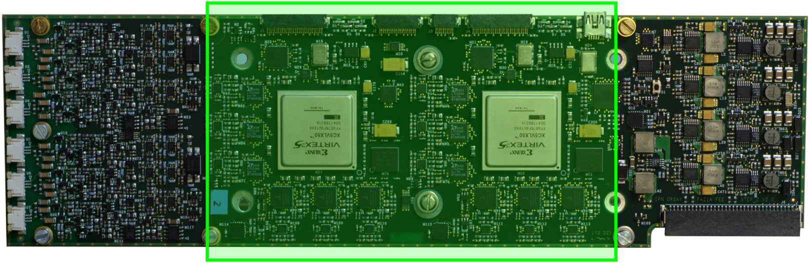
Analog chain (for each telescope)

- 3 fixed gain charge pre-amplifiers (8 V out dynamic range)
- High range signals are **attenuated** by a factor 4
- Low range signals are **amplified** by a factor 4
- Current signal by **analog differentiation** of charge signals

Front-end electronics



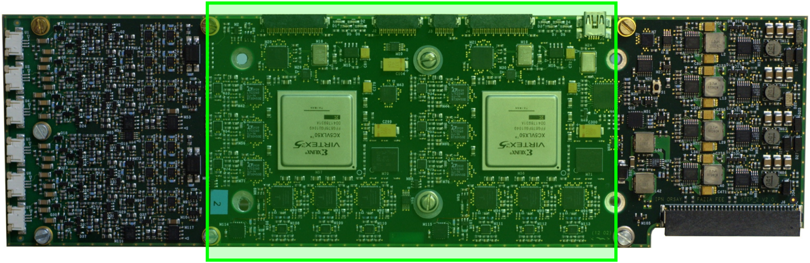
Front-end electronics



6 sampling ADCs per telescope

Si 1	14 bit, 100 MHz	4 GeV full-scale charge signal	**QH1**
	14 bit, 250 MHz	250 MeV full-scale charge signal	**QL1**
	14 bit, 250 MHz	current signal	**I1**
Si 2	14 bit, 100 MHz	4 GeV full-scale charge signal	**Q2**
	14 bit, 250 MHz	current signal	**I2**
CsI(Tl)	14 bit, 100 MHz	4 GeV Si-equiv. f.s. charge signal	**Q3**

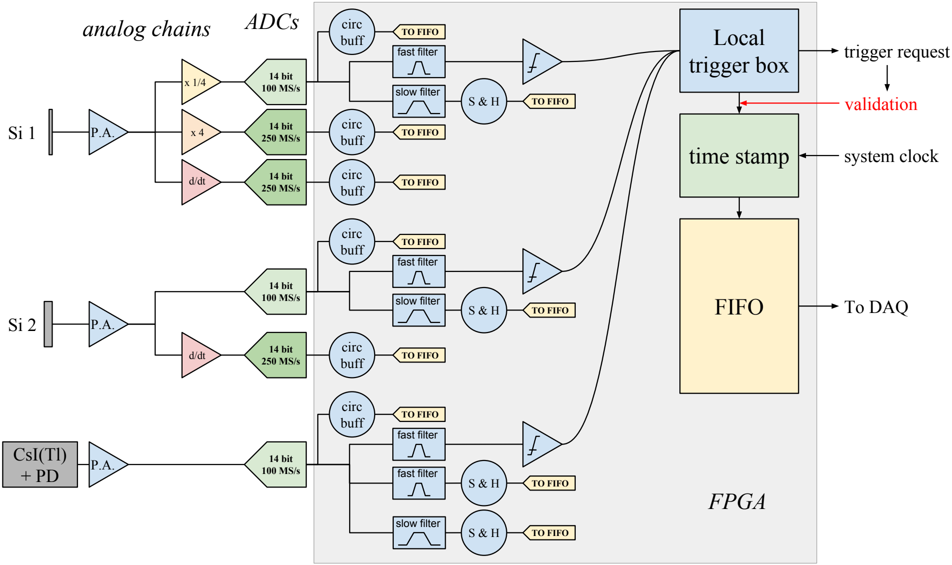
Front-end electronics



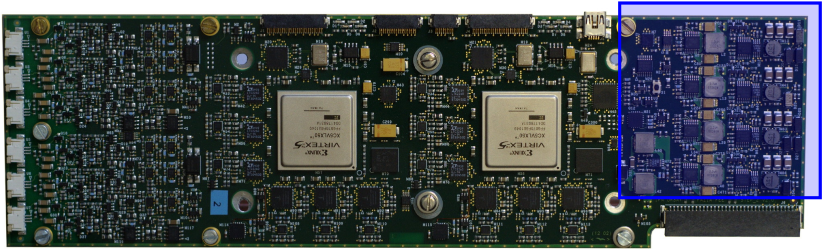
Xilinx Virtex-5 FPGAs

- Each FPGA process signals from one telescope
    - signals stored in **circular buffers** (up to **8192 samples**)
- On-board **real-time** trapezoidal shaping and **PSA**
    - fast shaped signals to leading-edge discriminators
    - maximum of slow shaped signals to acquisition
    - no pole-zero correction

Front-end electronics



Front-end electronics



HV generation

- DC/DC converters produce the Si detectors **bias voltages**:
  - 0–300 V for Si1 (140 V depletion voltage)
  - 0–400 V for Si2 (290 V depletion voltage)
- CsI(TI) photodiode bias voltage from the Power Supply card:
  - **optocoupler switch** on FEE card.

Front-end electronics

Back plane connector

- Power supply and CsI(TI) HV from power supply card
- Equalized 25 MHz **clock distribution** between FEE cards
- Star connection between FEE cards and block card:
  - FEE to BC: 2x400 Mb/s links (⇒ **800 Mb/s**)
  - BC to FEE: 1x400 Mb/s link
- Slow control communication

Half bridge and power supply

Half Bridge

- Designed at INFN – Napoli
- High power voltage conversion from 48 V DC input:
  - 22 V (14 A) DC
  - 5.5 V (70 A) DC

Power Supply

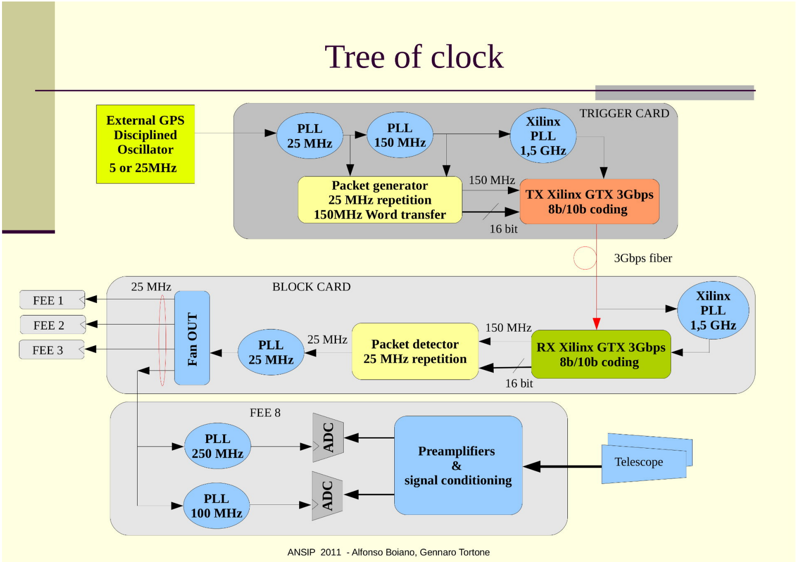
- Designed at INFN – Napoli
- Converts 22 V to 13 V, -9 V, ± 5 V and CsI(Tl) HV
- PIC monitors produced voltages together with 5.5 V from h-b
  - power on/power off
  - under/over voltage protection
  - voltage/current limits

Block Card

Block card

- Designed at INFN – Napoli
- Takes data from FEE cards via the back plane and builds up part of the event record
  - event counter consistency check
- Features a **3 Gb/s** optical link to regional board
  - 16-bit 8b/10b GTX transceiver
  - fixed latency transmission protocol
  - every 40 ns trigger multiplicity information is transmitted
- 25 MHz clock from fibre-recovered clock
  - PLL for **jitter cleaning**

Block Card



courtesy of A. Boiano, INFN – Napoli

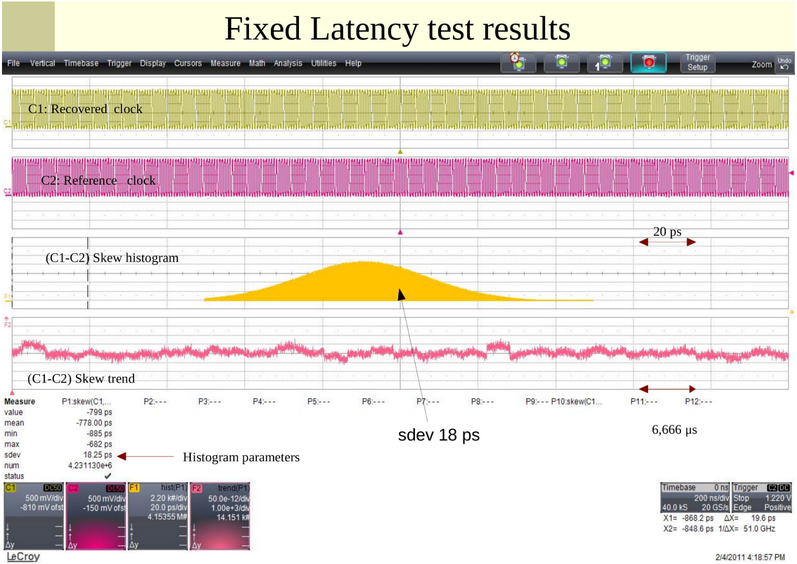
Cross syncronization

Sampling clock syncronization

- **Fixed latency** transmission[a]:
  - all ADC clocks have the same phase ($\sim$ 20 ps skew)
  - digitized signals don't have the 1 clock indetermination typical of asyncronous systems

[a] R. Giordano *et al*, IEEE Trans. on Nucl. Science 58 (194), 2011

Cross syncronization



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Cross syncronization

Sampling clock syncronization

- **Fixed latency** transmission[a]:
  - all ADC clocks have the same phase ($\sim 20\,\mathrm{ps}$ skew)
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- Common periodic **reference signal sampling**[b]:
  - additional cross-syncronization technique
  - improves time resolution up to $\sim 10\,\mathrm{ps}$

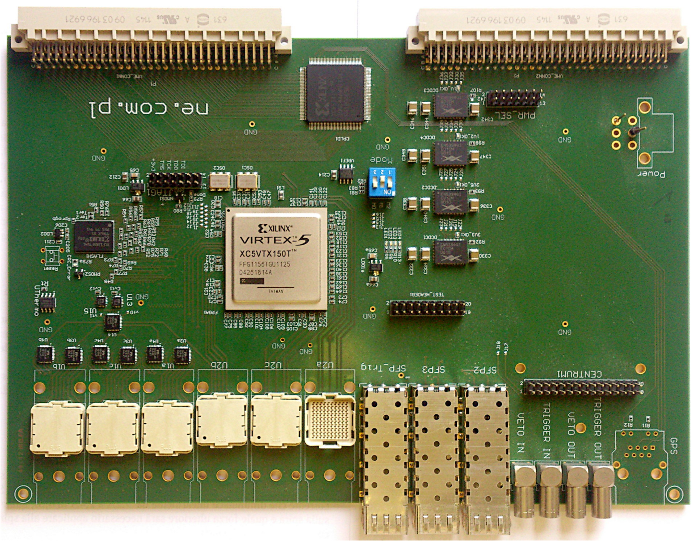
[a] R. Giordano *et al*, IEEE Trans. on Nucl. Science 58 (194), 2011
[b] L. Bardelli *et al*, Nucl. Instr. and Meth. A 572 (882), 2007

Regional board

Regional Board

- Designed at Jagiellonian University, Krakow
- Features a Xilinx Virtex-5 FPGA
  - VHDL code has been written mainly at INFN – Napoli
- **36x** 3 Gb/s bi-directional optical links
  - to/from FAZIA blocks
  - fixed latency protocol
- 2x 1 Gb/s optical ethernet links (1000Base-SX)
  - now only 1 is used ⇒ room for transmission speed increase
  - **UDP protocol** for low-latency transfer
- Possibility to connect GANIL **CENTRUM** module

Regional board



Regional board

Regional Board tasks

- **Trigger board**:
  - multiple majority logic for trigger validation
  - trigger scaling by a settable factor
  - master/slave trigger operation (for coupling)
- **Event building** from data coming from all the blocks
  - it may add the CENTRUM timestamp to each event
- **Transmission** of acquired data to servers
  - maximum speed achieved: $\sim 80\,\mathrm{MB/s}$ ($\sim 640\,\mathrm{Mb/s}$)
- **Slow control** management of all the electronics
  - data transmission and slow control use the same optical fibre

Coupling with other apparatuses

FAZIA—INDRA and FAZIA—gas coupling

FAZIA modularity makes coupling easy:

- CENTRUM[1] modules could be used for coupling
- FAZIA—INDRA coupling is in progress!

[1] developed at GANIL, Caen

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Trigger

- Asynchronous mode
- Master/slave
  (common dead time)

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CENTRUM operation

1. **Validation received** from one or both detectors
2. **Timestamp given** to both detectors

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Coupling with other apparatuses

FAZIA—INDRA and FAZIA—gas coupling

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- CENTRUM[1] modules could be used for coupling
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- data merging using NARVAL[2]

Trigger

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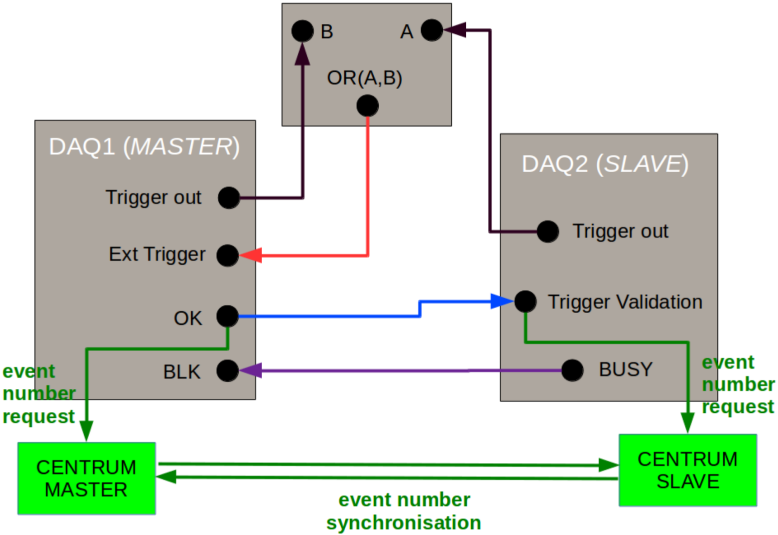
- Master/slave (common dead time)

CENTRUM operation

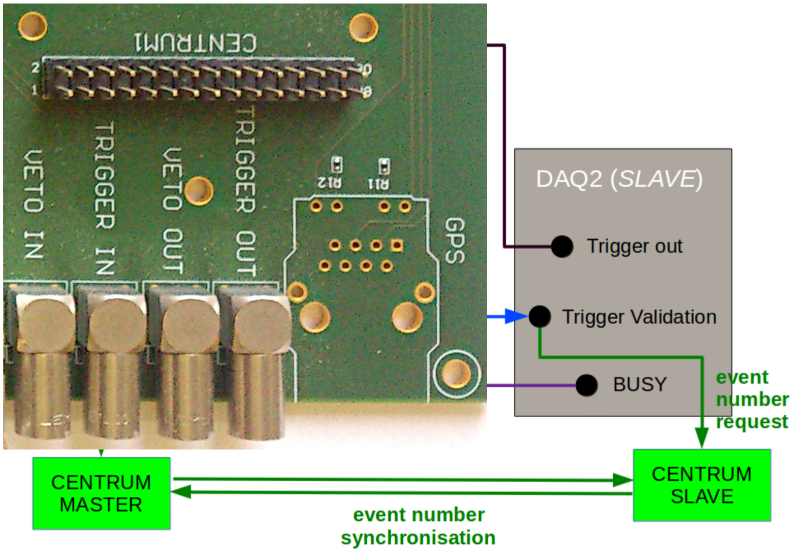
1. **Validation received** from one or both detectors
2. **Timestamp given** to both detectors

[1] developed at GANIL, Caen
[2] developed at IPN, Orsay

Common dead time coupling



Common dead time coupling



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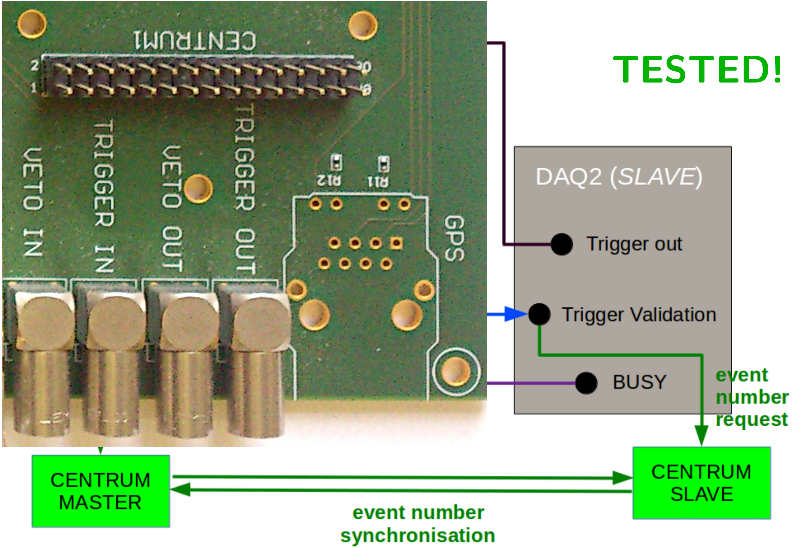
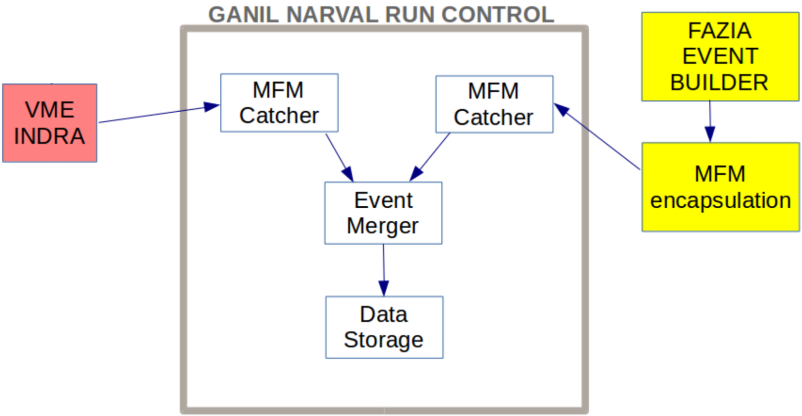


Data merging with NARVAL



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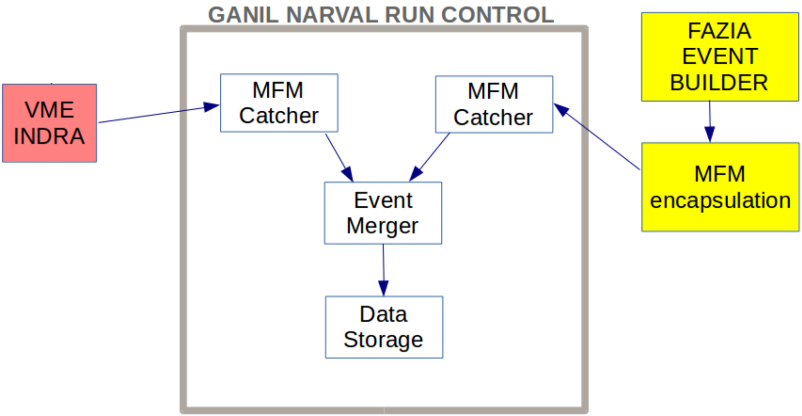


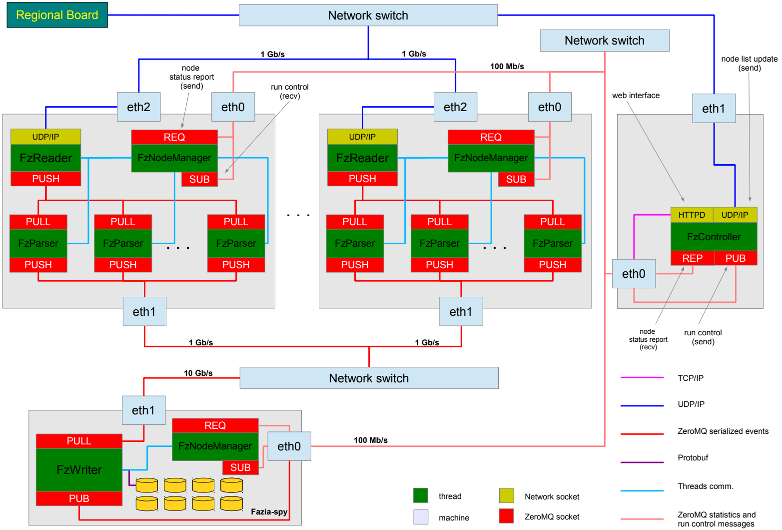
(Not yet tested...)

Acquisition and monitoring

Acquisition system

- Developed at INFN – Napoli
- Finite State Machine logic
- Multi-thread and **multi-machine**
  - controller sends machine IP addresses to regional board
  - regional board stores IP addresses inside a list
  - each event is sent to a different PC of the list sequentially
- Data merged and written to a data server.
- Monitoring software receives **live data** from the acquisition
- Data transfer between machines via **ZeroMQ** protocol
- NARVAL frame encapsulation implemented

Acquisition and monitoring



courtesy of G. Tortone, INFN – Napoli

Slow Control

Slow Control is used to read and/or change:

- Trigger operation mode (master/slave) for coupling
- Detector bias voltages and leakage currents
- Trigger and acquisition **thresholds**
- Number of **acquired samples** of signal and **pre-trigger length**
- Trapezoidal shaper characteristics (**rise time** and **flat top**)
- Many other FEE card, block card, power supply and regional board parameters

Slow Control

Slow Control operation:

- Any PC can send Slow Control commands as UDP packets
- Request for regional board:
  - RB executes the request and replies to PC
- Request for block card, power supply of FEE card:
  - RB forwards the request to all the blocks
  - RB waits for the answer, then forwards it to the PC
- Regional Board replies to **the same PC** that sent the request
- Fazia GUI[a] is a graphical tool to send Slow Control commands

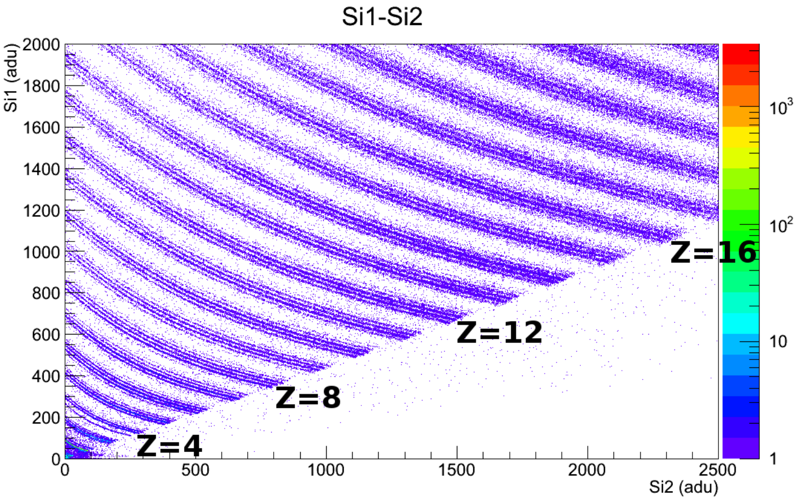
[a] developed at GANIL and INFN – Firenze

Slow Control

Summary and conclusions

- FAZIA implements **compact electronics** that permit to do on-line analysis just next the detectors
  - minimization of signal distortion
  - data reduction at the source
- Very fast and **low latency** data transfer
- Possibility to perform precise **time measurements** thanks to block cross-syncronization
  - E vs ToF to identify particles **stopped** in the first Si-layer
  - possibility to measure with **low-energy** beams
- Possibility to couple FAZIA with other apparatuses via CENTRUM and NARVAL
- Despite its compact design, energy resolution and quality of Z and A identification of FAZIA block is **comparable or better** than prototypal FAZIA telescopes.

identification capabilities



FAZIA collaboration

Thanks for your attention