New generation Pixel Readout ASICin 65nm CMOS for Extreme Rates at HL-LHC :

INFN/CHIPIX65 contributions to RD53: recent results and perspectives

L. Demaria, INFN / Torino

On behalf of CHIPIX65 collaboration

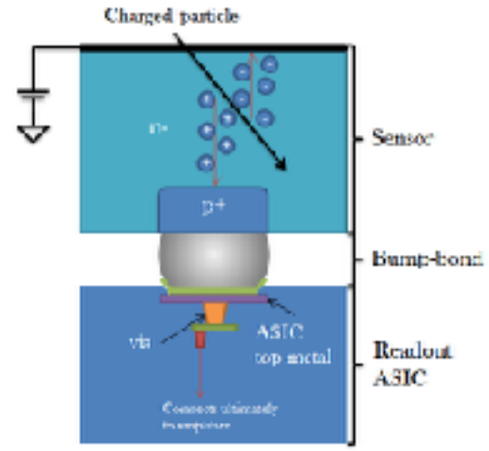
Pixel Detector at HL_LHC

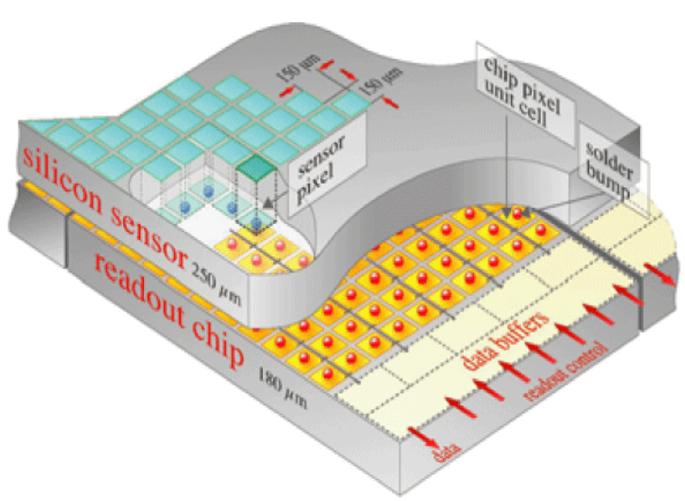
Requirements from HL_LHC experiments

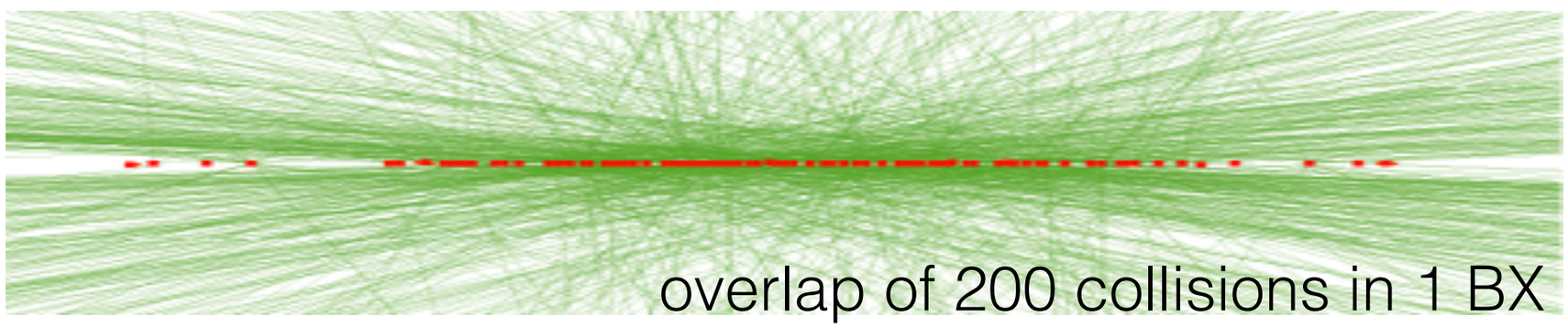
Small pixels: 50x50um^2 x 6
Large chips: 2cm x 2cm (~1 billion transistors)
Pixel Hit rates: up to 3 GHz/cm^2 (200 P.U.) Phase-1: 600MHz/cm^2
Radiation: 1Grad, 10^{16} n/cm^2 (unprecedented)

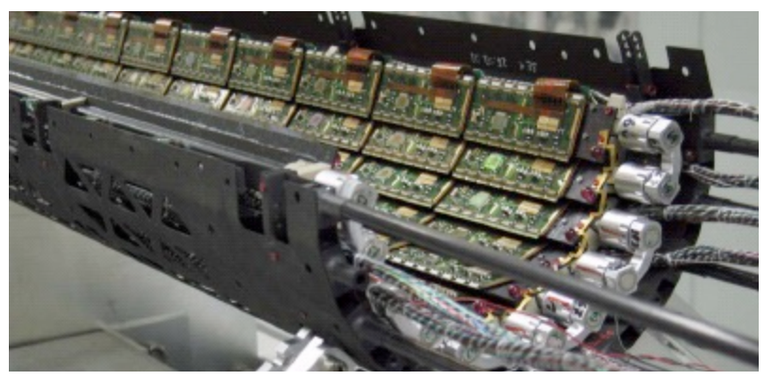
Trigger: up to 1MHz with 12.8us latency
(~100x buffering and readout)
Low power - Low mass systems

Data readout : up to 4-5 Gbs/s









CHIPIX65

Web-site: http://chipix65.to.infn.it

CALL Project CSN5 approved in October 2013

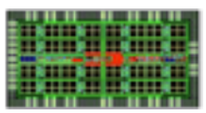
Development of an innovative **CHIP** for a **PIX**el detector, using a CMOS **65**nm technology for the first time in HEP community, for experiments with extreme particle rates and radiation at future High Energy Physics colliders.

Principal Investigator : Natale Demaria - INFN/Torino

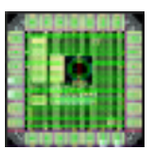
Institutes:

Bari, Lecce, Milano, Padova, Pavia, Perugia, Pisa, Torino

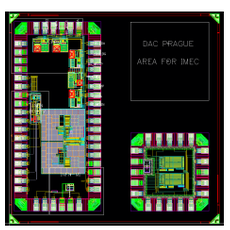
People (~40 of which 50% ASIC designers; 12.4 FTE)



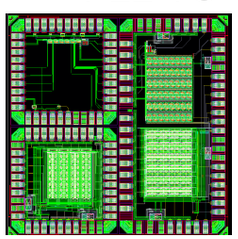
DCDC-Le



PLL-TO



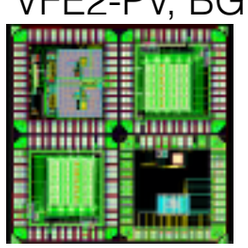
BG, DAC-Ba



VFE1-Pv

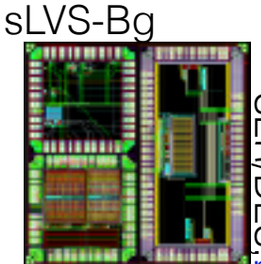
VFE1-TO

VFE2-PV, BG



VFE2-TO

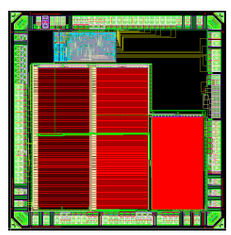
sLVS-Bg



DualRail

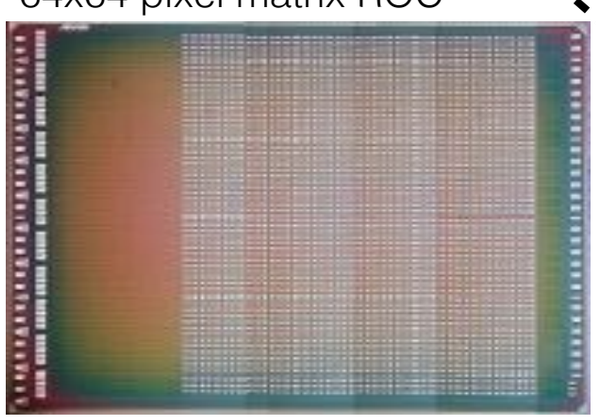
sLVS-Pi, ADC, SER/DES

SRAM-Mi



Submissions made in CMOS 65nm

64x64 pixel matrix ROC



Work Packages:

Radiation Hardness – A.Paccagnella (Padova)
Digital Electronics – R.Beccherle (Pisa)
Analog Electronics - A.Rivetti (Torino)
Chip Integration - V.Re (Pavia/Bergamo), V.Liberali (Milano)

Papers / talks / thesis

- 27 talks at International conferences
- 3 degree theses, 3 PhD thesis
- 26 papers on international journals

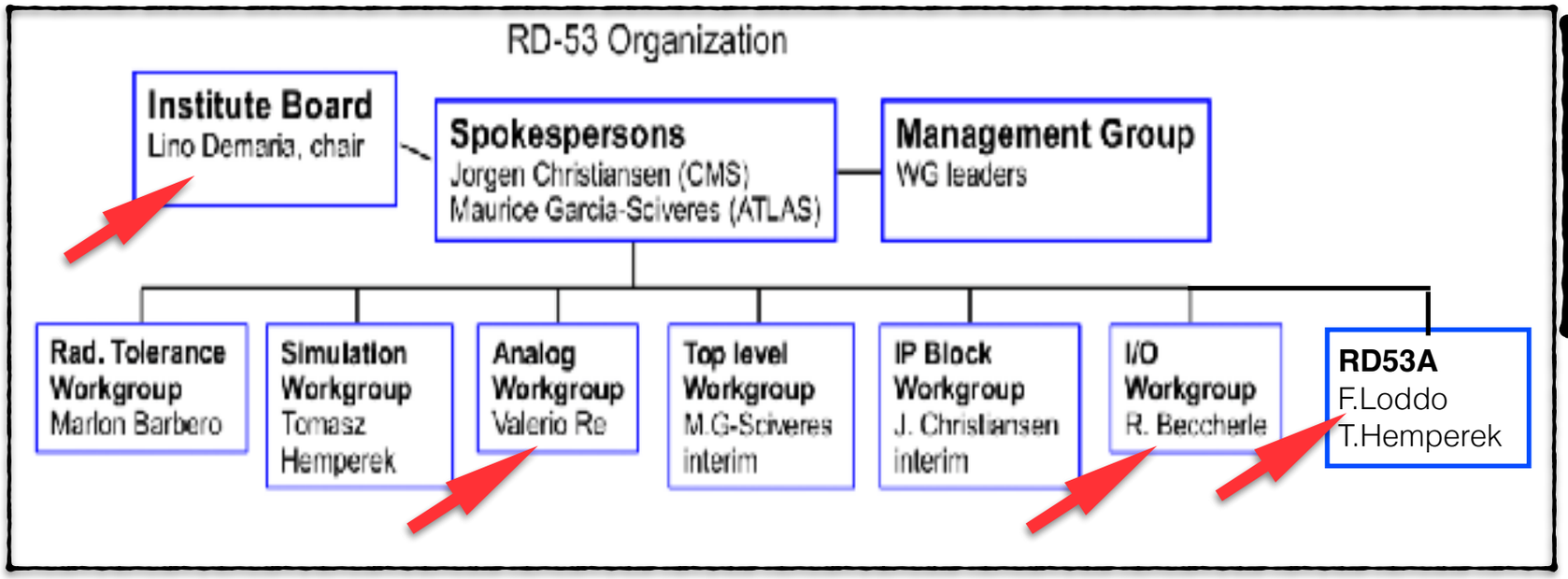
CHIPIX65 Project

Institutes:

Bari, Lecce, Milano, Padova, Pavia, Perugia, Pisa, Torino

People (44 of which 50% ASIC designers)**:**

N.Demaria, G.Dellacasa, G.Mazza, A.Rivetti, M.D.Da Rocha Rolo, E.Monteil, L.Pacher, F.Ciciriello, F.Corsi, C.Marzocca, G.De Robertis, F.Loddo, C.Tamma, M.Bagatin, D.Bisello, S.Gerardin, S.Mattiazzo, L.Ding, P.Giubilato, A.Paccagnella, F.De Canio, L.Gaioni, M.Manghisoni, V.Re, G.Traversi, E.Riceputi, L.Ratti, C.Vacchi, R.Beccherle, G.Magazzu, M.Minuti, F.Morsani, F.Palla, V.Liberali , S.Shojaii, A.Stabile , G.M.Bilei , M.Menichelli , S.Marconi, D.Passeri, P.Placidi, S.D'Amico, C.Veri, A.Donno.



	Country	Town	Institute	Inst. Representative
1	Czech Republic	Prague	FNSPE-CTU/IP-ASCR	Miroslav Havranek
2	France	Marseille	CPPM	Alexandre Rozanov
3	France	Paris	LPNHE	Giovanni Calderini
4	Germany	Bonn	Bonn University	Hans Krüger
5	Italy	Bari	INFN and Politecnico	Flavio Loddo
6	Italy	Milano	INFN and University	Valentino Liberali
7	Italy	Padova	INFN and Politecnico	Alessandro Paccagnella
8	Italy	Pavia	INFN and University	Valerio Re
9	Italy	Perugia	INFN and University	Gian Mario Bilei
10	Italy	Pisa	INFN and University	Fabrizio Palla
11	Italy	Torino	INFN and University	Natale Demaria
12	Netherlands	Amsterdam	NIKHEF	Nigel Hessey
13	Spain	Sevilla	Sevilla University	Rogelio Palomo
14	Switzerland	Geneva	CERN	Jorgen Christiansen
15	UK	Didcot	Sc.&Tech Facilities Council	Mark Prydderch
16	USA	Chicago	Fermilab	David Christian
17	USA	Berkeley	University of California	Beate Heinemann
18	USA	Albuquerque	Univ of New Mexico	Sally Seidel
19	USA	Santa Cruz	U.C. Santa Cruz	Alex Grillo

Institutes:
8 CMS, 2 CMS/ATLAS, 9 ATLAS

RD53 Collaboration
is a real and effective synergy
among CMS-ATLAS communities
with a specific and focused goal
with a real main deliverable:
a **LARGE scale FRONT-END ASIC prototype for Pixel-Phase 2 detectors**

Personal comment:
quite unique experience
challenging when going to decision
EXCELLENT melting pot !

INFN: 7 groups,
30% of RD53 members

Web-site: http://rd53.web.cern.ch/rd53/

Ingredients and strategy defined in RD53

A. Development of Building blocks
   - IP-Block
   - Analog Very Front Ends

B. Development of Digital Architecture

C. Verification environment

D. Complex Chip Integration : modern tools to secure a successful ASIC submission

E. Radiation characterization: try mitigation strategy

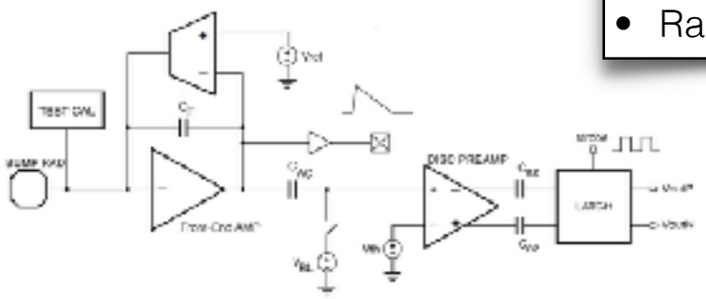
Small DEMONSTRATORs : 64x64 pixel matrix
- FE65P2
- CHIPIX65-FE0

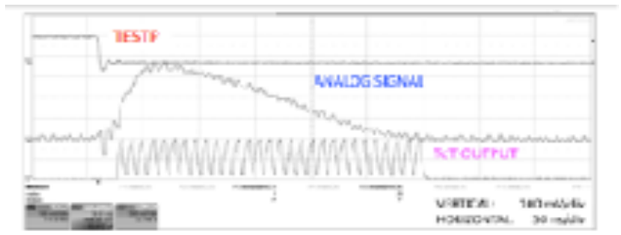
RD53A large scale prototype

Time

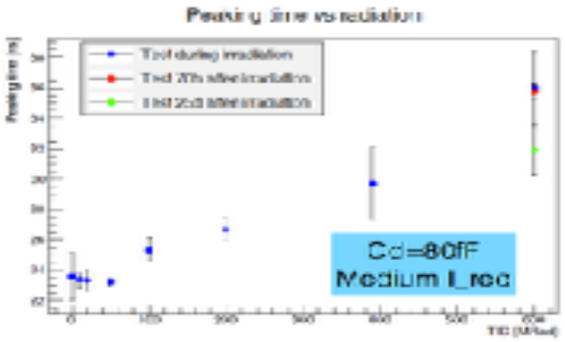
Synchronous Design

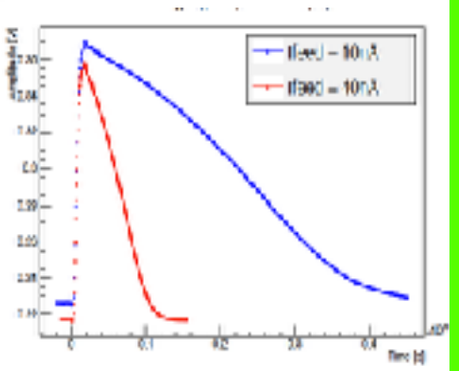
- Compact: 35x35 um^2,Low power (<5uW)
- Low Noise (<100e$^-$), Fast ToT (~150ns),
- Rad-Hard (6-800 MRad)

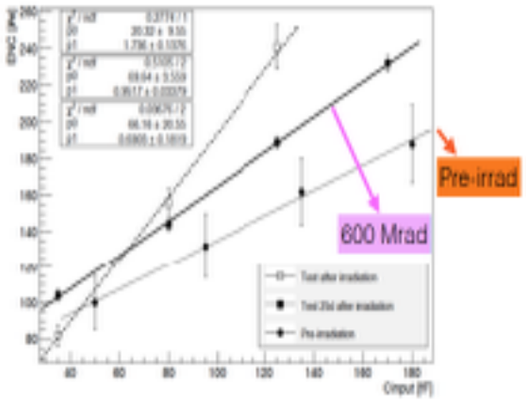




ToT frequency vs radiation

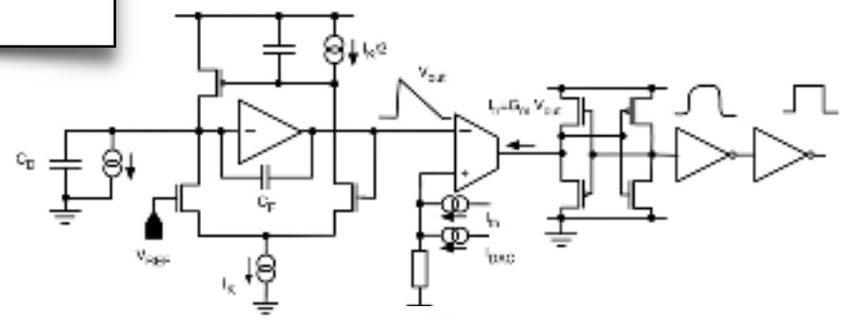


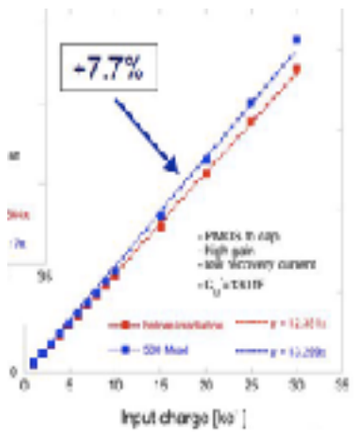


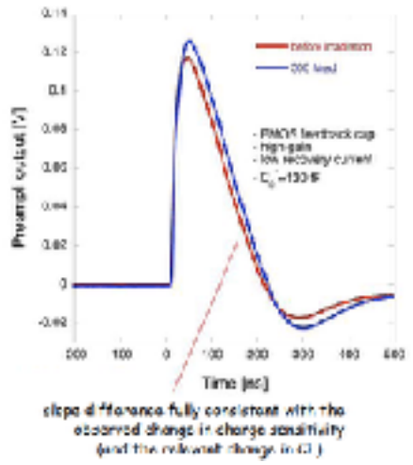


ANALOG Very Front ENDs

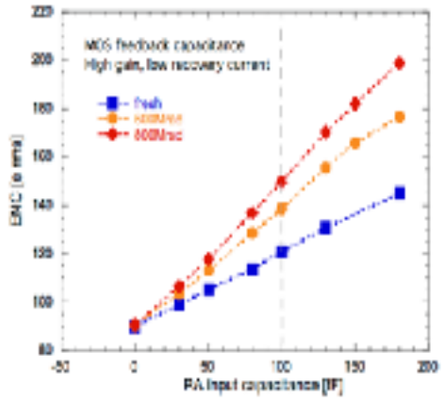
Asynchronous designn



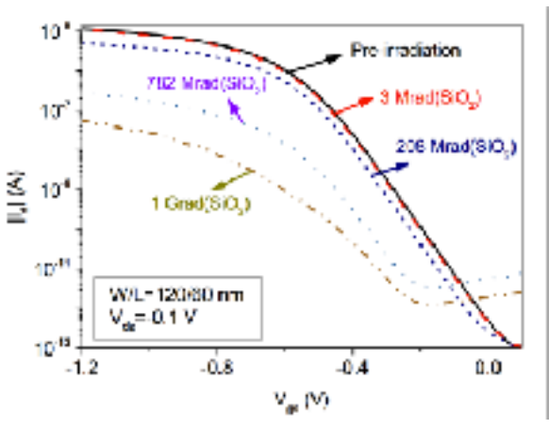


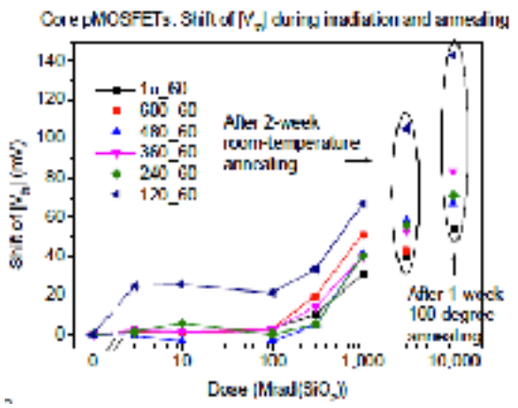


slope difference fully consistent with the observed change in charge sensitivity (and the relevant change in C_D)

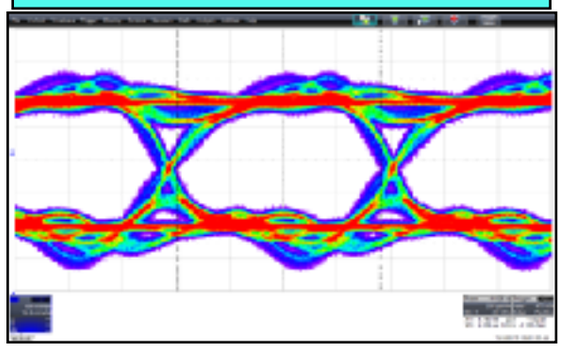


Radiation Characterisation

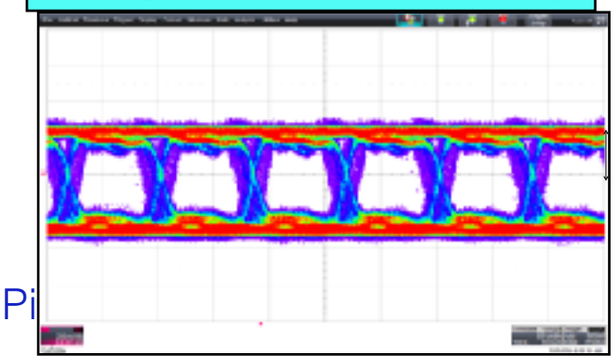


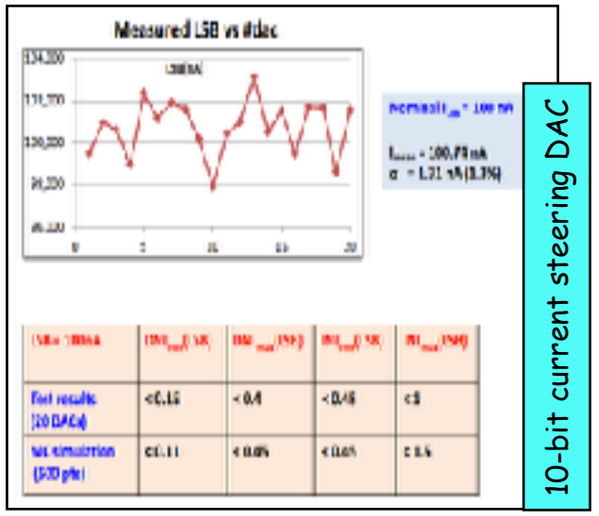


Eye diagram: SLVS driver@1.2 Gbps

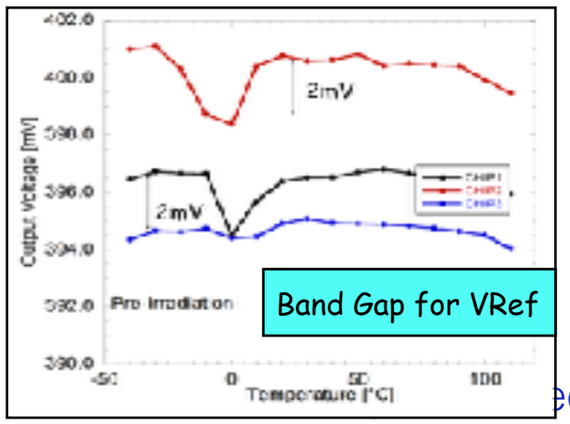


Eye diagram: SLVS receiver@1.2 Gbps





10-bit current steering DAC



Band Gap for VRef

IP-Blocks

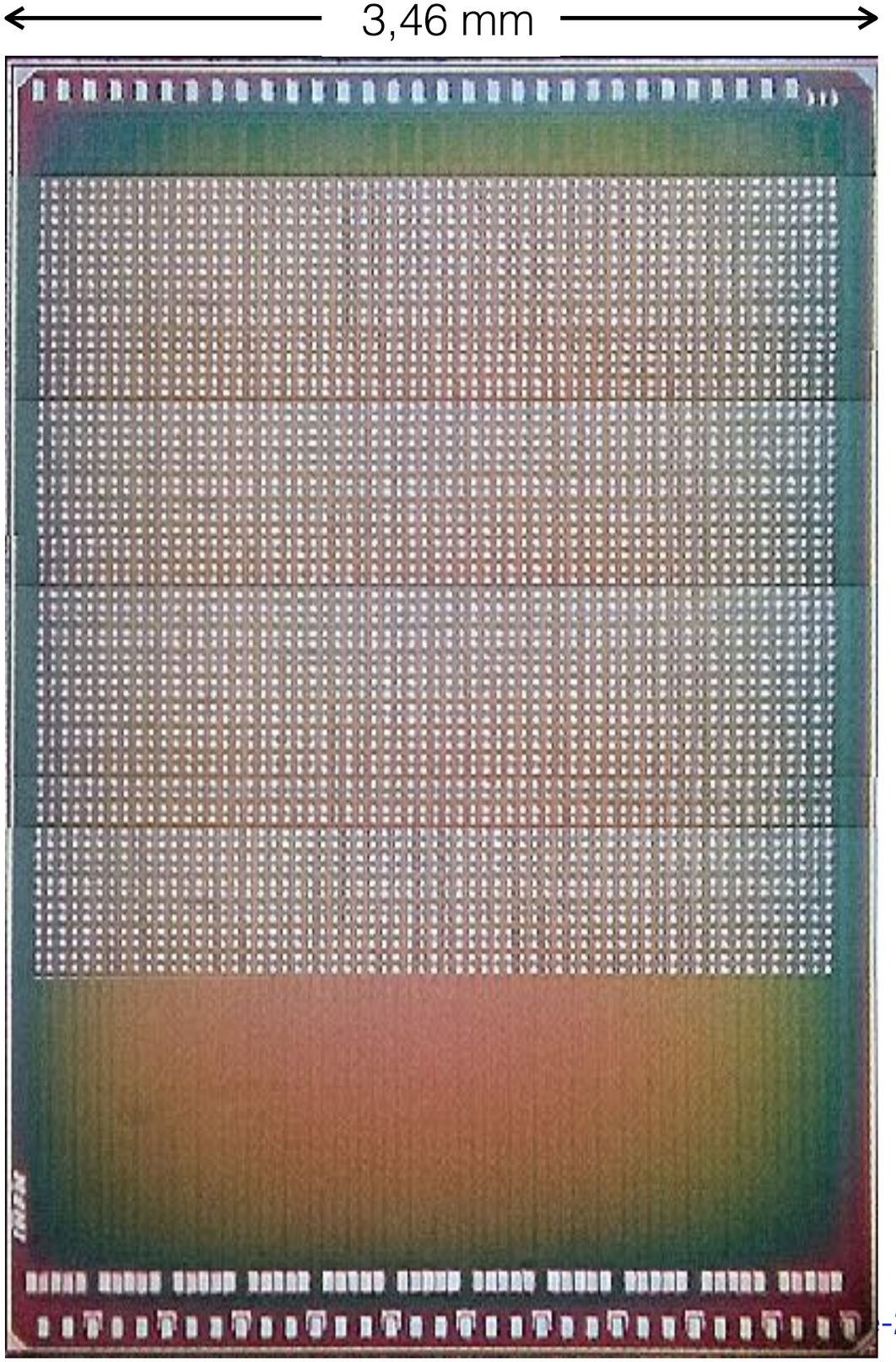
List of CHIPIX65 IP-blocks

- Band Gap : Pavia
- DAC :Bari
- SLVDS driver : Pavia, Pisa
- SLVDS receiver : Pavia,Pisa
- PLL : Tor,Padova
- SER : Pisa
- DES : Pisa
- Monitoring ADC: Bari
- SRAM EOC : Milano
- Dual Digital Cell : Milano
- DC-DC : Lecce

CHIPIX65
Design Submissions

DESIGN	TEAM	2014				2015				2016		Rad. characterization
		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	
SER	Pisa			v1			v1					V1
DES	Pisa			v1			v1					
SLVS-TX/RX	Pisa						v1			v2		v1
SLVS-TX/RX	Pavia						v1					v1
BandGap	Pavia			v1			v2					v2
DualRail Dig	Milano						v1					
DICE RAM	Milano			v1						v2		
DAC-curr	Bari			v1								v1
ADC	Bari						v1			v2		
PLL	Torino									v1		
DC-DC	Lecce									v1		
VFE-synch	Torino			v1			v2					v2
VFE-async	Pavia			v1			v2					v2
CHIPIX_DEMO (64x64)	ALL										X	

CHIPIX65-FE0: Summary



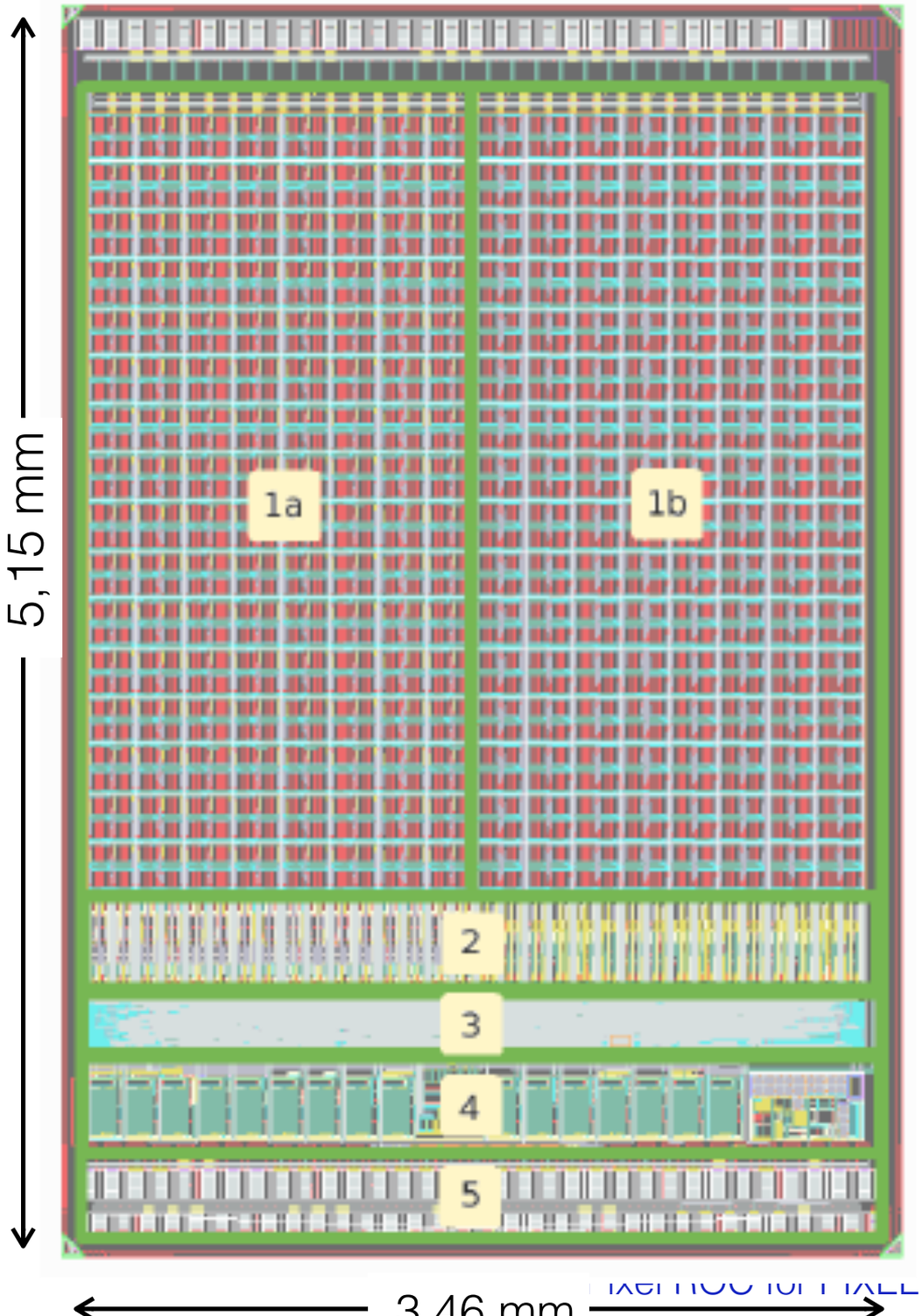
	RD53A Specs	CHIPIX65-FE0
Technology	65nm CMOS	yes
Pixel size	50x50 um2	yes
Detector foreseen	Cap<100fF, Leakage<10nA	yes
Detection threshold	<600 e-	ok, bare chip 250e-
In-Time threshold	<1200 e-	ok
Noise hits	<1E-6	ok
Trigger rate	1 MHz	ok
Trigger Latency	12,5 usec	ok
Hit Rate	< 3 GHz/cm2	ok
Hit Loss at Max hit rate	< 1%	ok
Charge resolution	at least 4-bits (500e-)	5-bits (200-500e-)
Pixel analog/digital	4uA / 4uA	ok
Pixel array	400x192 pixel (2cm2)	64x64
Radiation tolerance	500 Mrad, 1E16 1 MeV n/cm2	Analog ok, digital tbd

Full INFN development (about 1 year work):
- Two Analog Very Front Ends
- IP-block (DAC,ADC, I/O, BandGap, sLVS-TX/Rx, Serialiser)
- Digital design, digital-on-top, chip integration

~3 Millions digital standard cells
(400 each pixel)

submitted: 5/7/2016
Arrived: 26/9/2016

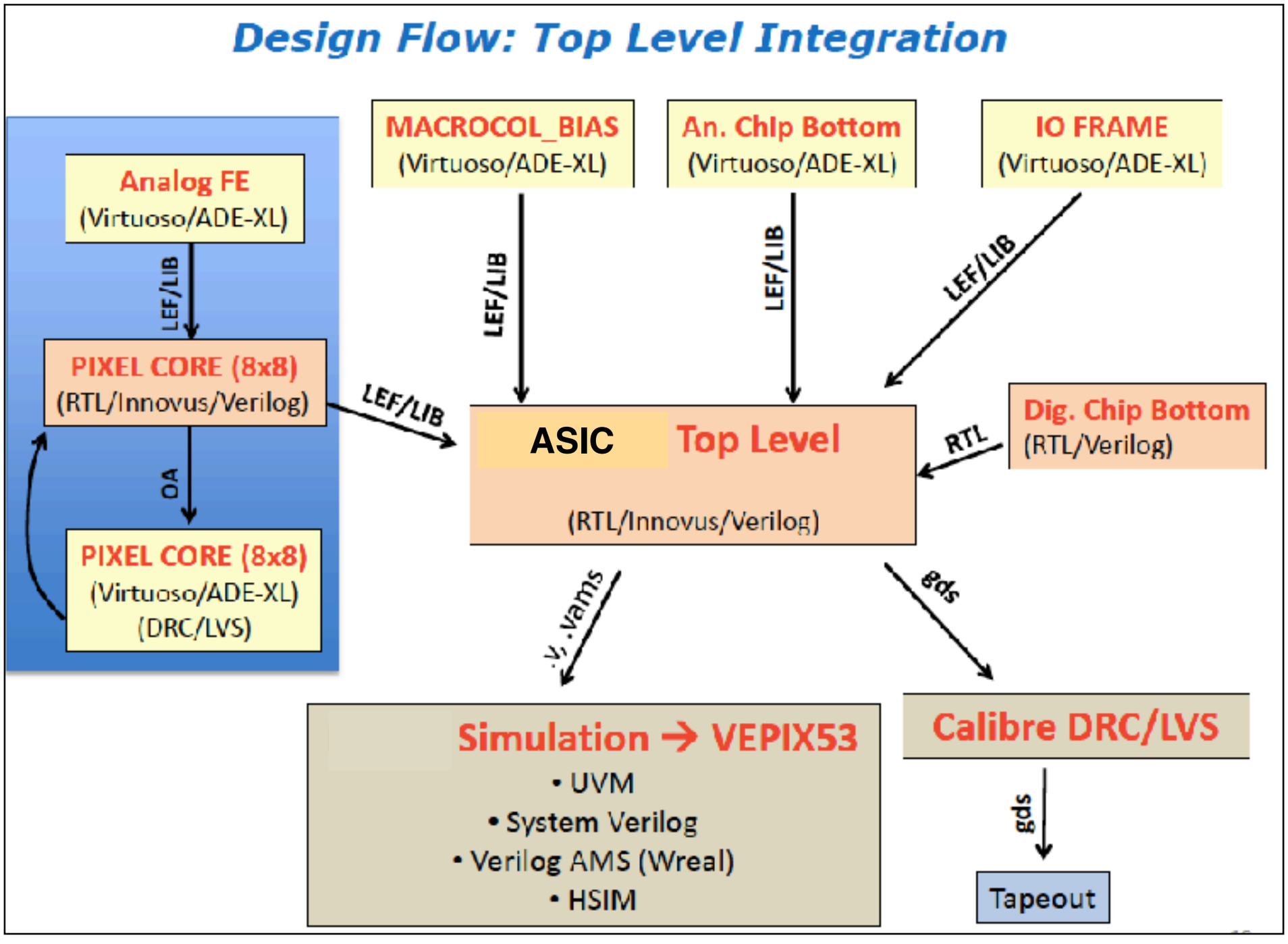
CHIPIX65-FE0 layout



1. 64 × 64 Pixel Array
   - a Synchronous Front-End Architecture — VFE-Torino
   - b Asynchronous Front-End Architecture — VFE-Bg/Pv
2. Column Bias Cells with current mirrors (Analog)
3. End of Column and SER (Digital)
4. Global DACs, BGR and ADC
5. SLVS TX/RX and I/O cells

- FIFO-based readout architecture, SPI-based chip configuration
- integration of available silicon-proven IP-blocks designed for RD53:
  - **Bandgap Voltage Reference** (Pavia INFN)
  - **SLVS transmitters/receivers** (Pisa INFN)
  - **High-speed SER** (Pisa INFN)
  - **10-bit biasing DAC** (Bari INFN)
  - **12-bit monitoring ADC** (Bari INFN)
- modified CERN rad-hard I/O library

ASIC design methodology



Additional tools for verification:

- Voltus
- Tempus

CHIPIX65-FE0 Design Team

CHIPIX Integration and Floor Planning

L.Pacher(*)

Digital

A.Paterno(*), L.Pacher

Analog Front Ends

E.Monteil(*), L.Gaioni(*), L.Ratti

IP-Blocks

F.De Canio(*), G.Traversi, F.Loddo(*), G.Magazzu, C.Marzocca, **F.Liciulli, F.Ciciriello**

Analog Bias and Monitoring

F.Loddo

Architecture Simulation and Verification

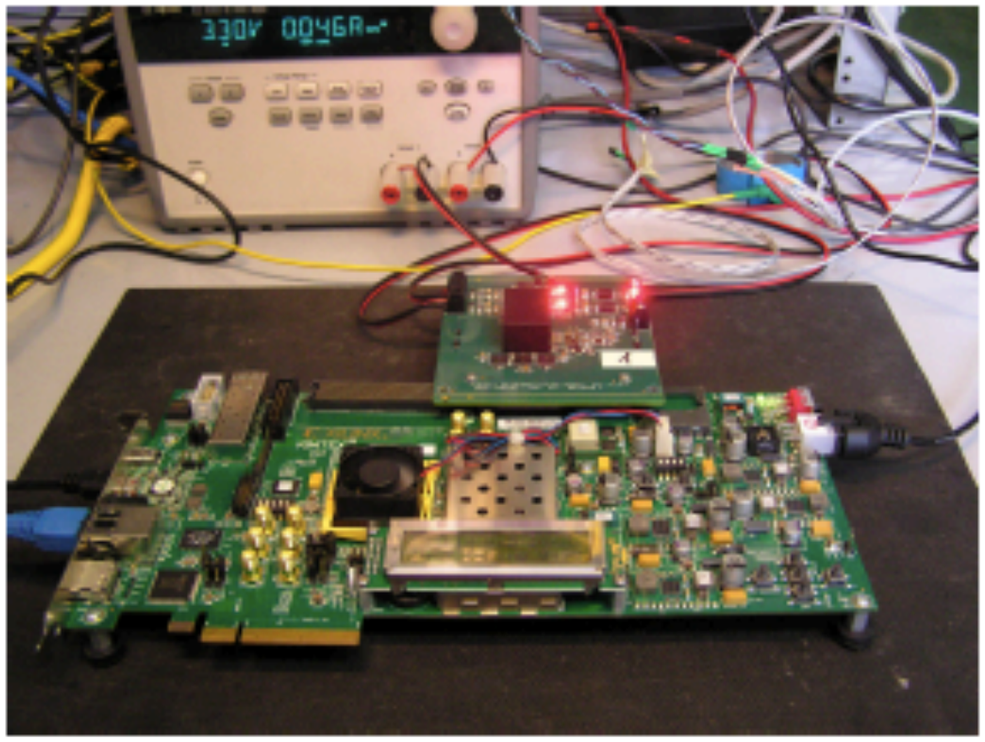
S.Marconi(*), E.Conti(*), G.Mazza, G.Dellacasa

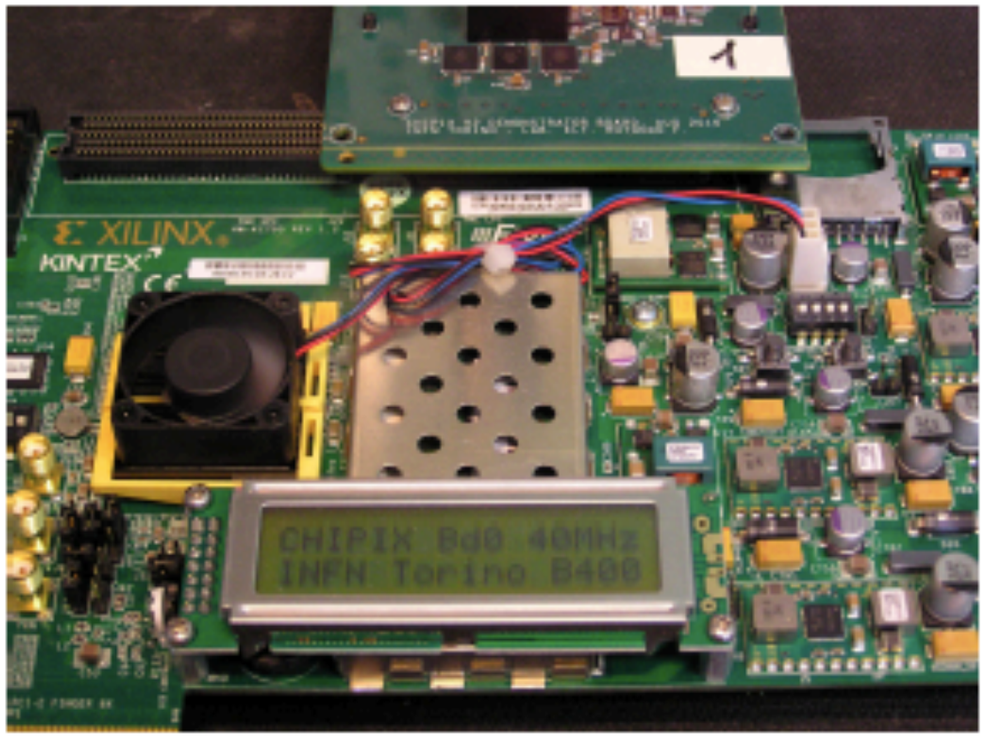
Young researchers are strongly contributing (in bold).

(*) : also part of RD53A design team

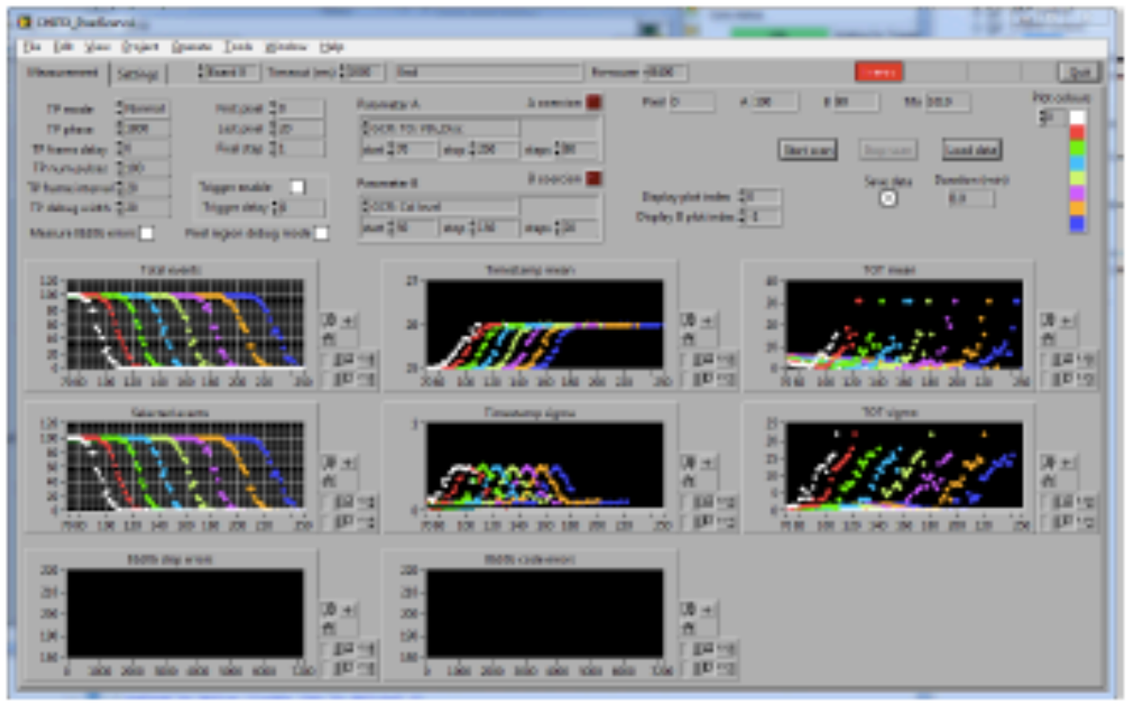
Testing of CHIPIX65-FE0: First Results

Test Set-up





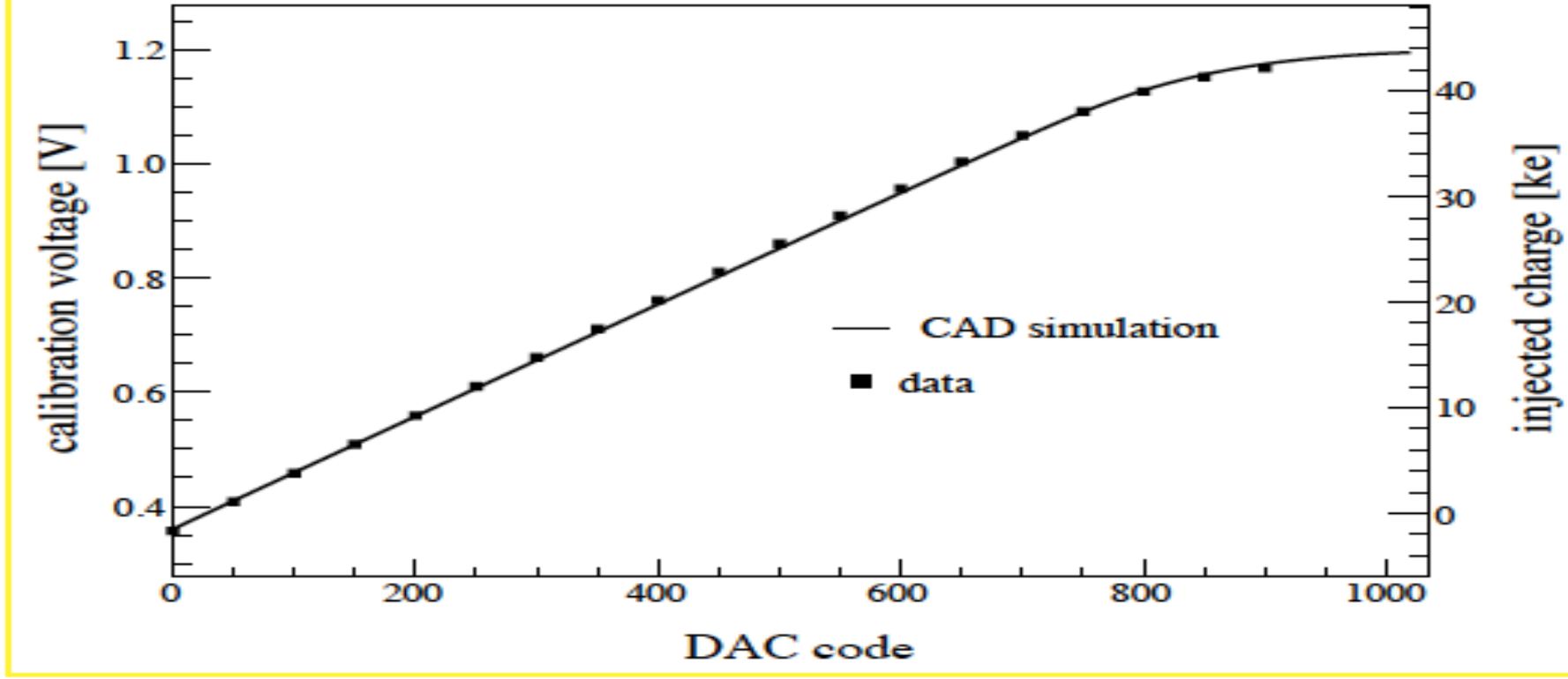
- chips received back from the foundry: END OF SEPTEMBER, 2016
- preliminary tests started in Turin: TWO WEEKS AGO
- full-digital ASIC/FPGA interface (FMC)
- prototype wire-bonded on a custom test board
- a few test points for global bias voltages/currents
- FPGA Xilinx Virtex 7 board
- LabView data acquisition test interface



Chip Performance summary

- **CHIP-configuration works correctly**
  - DAC / EoC / Pixel configuration via SPI
- **Bias distribution works correctly**
- **Regional digital architecture tested**
  - triggerless, triggered, binary / 5-bit digitization, debug-mode
- **Readout works fine**
  - EoC, Data output at 320 MHz with 8b10b encoding
- **ALL IP-block work:**
  - BandGap, DAC, ADC, sLVS-Tx/Rx, Serialiser
- **Analog VFE work fine**

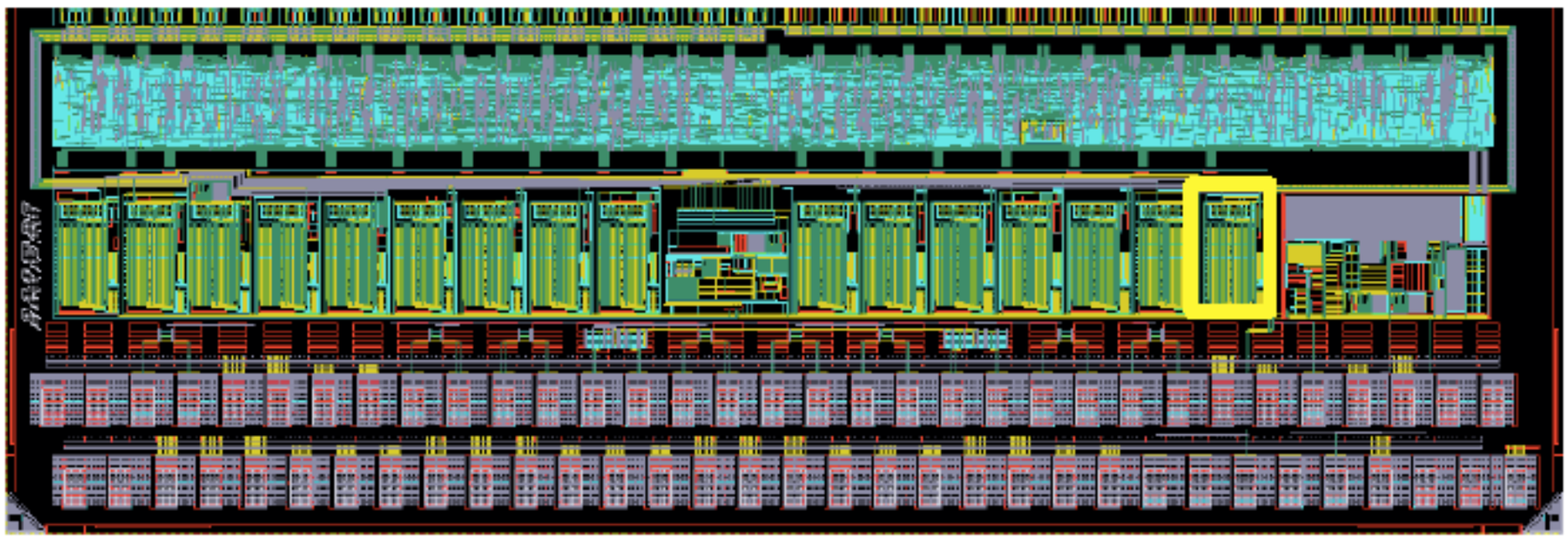
Charge Injection: DAC setting



Via a 10-bit DAC the calibration signal is sent to the pixel.

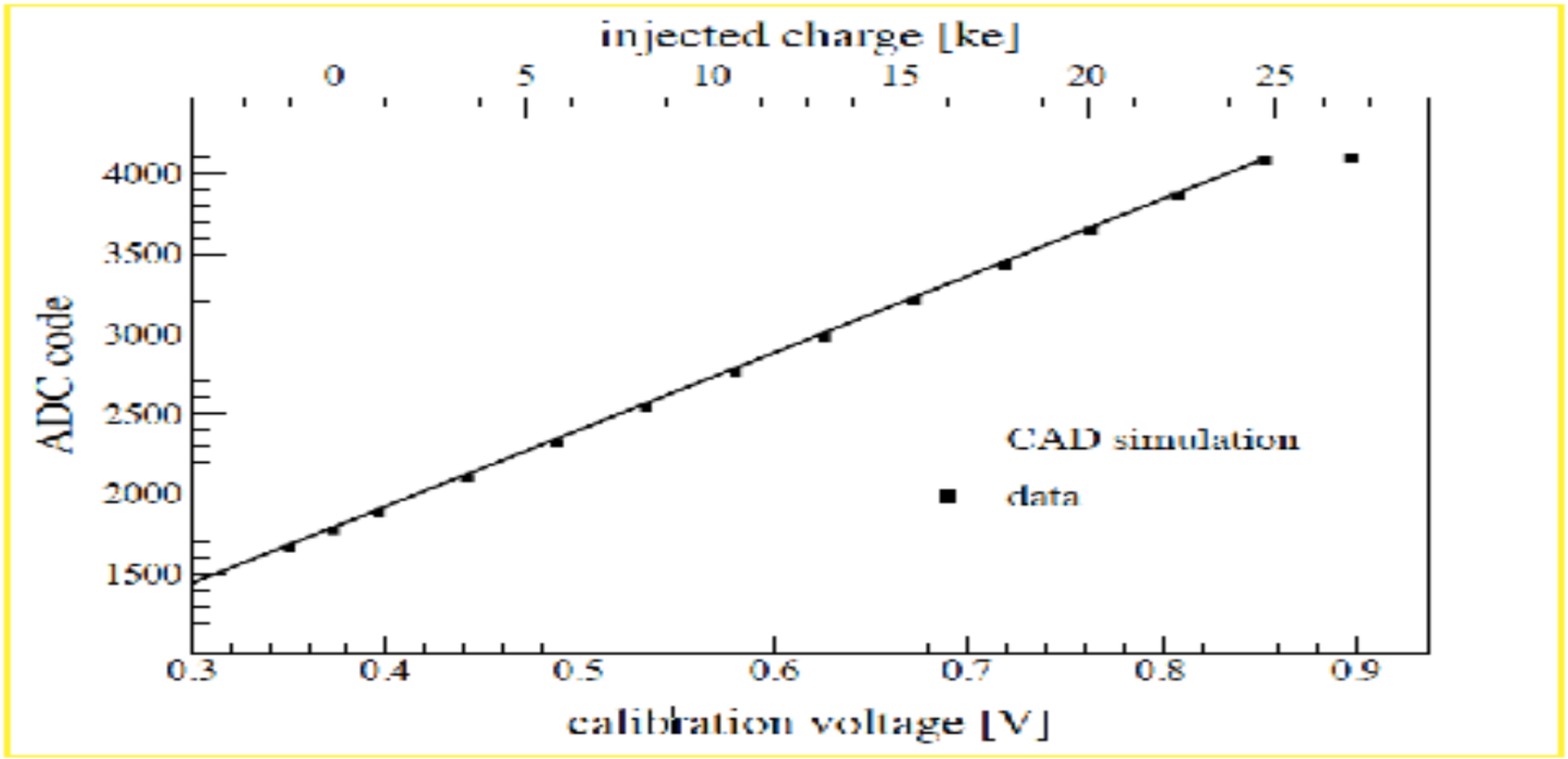
Q= Cin Vcal

1 DAC count= 48e-

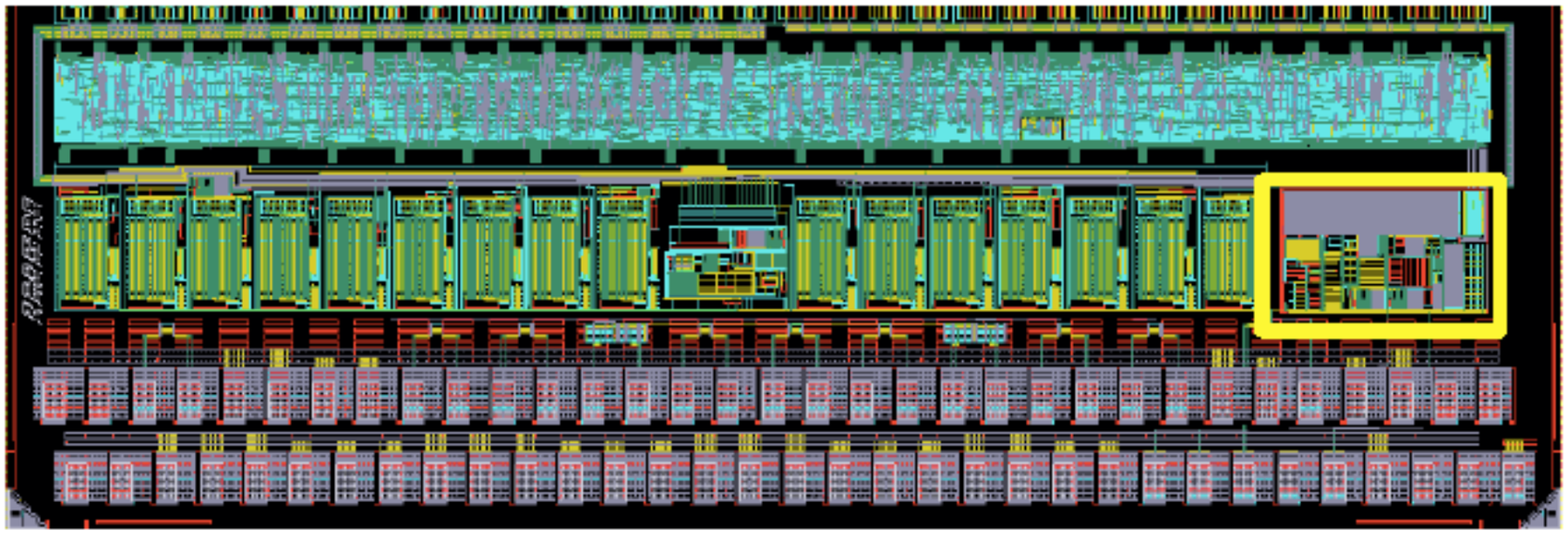


Total of 16 DAC:
- 9 VFE-TO
- 6 VFE-BG/PV
- 1 VCAL

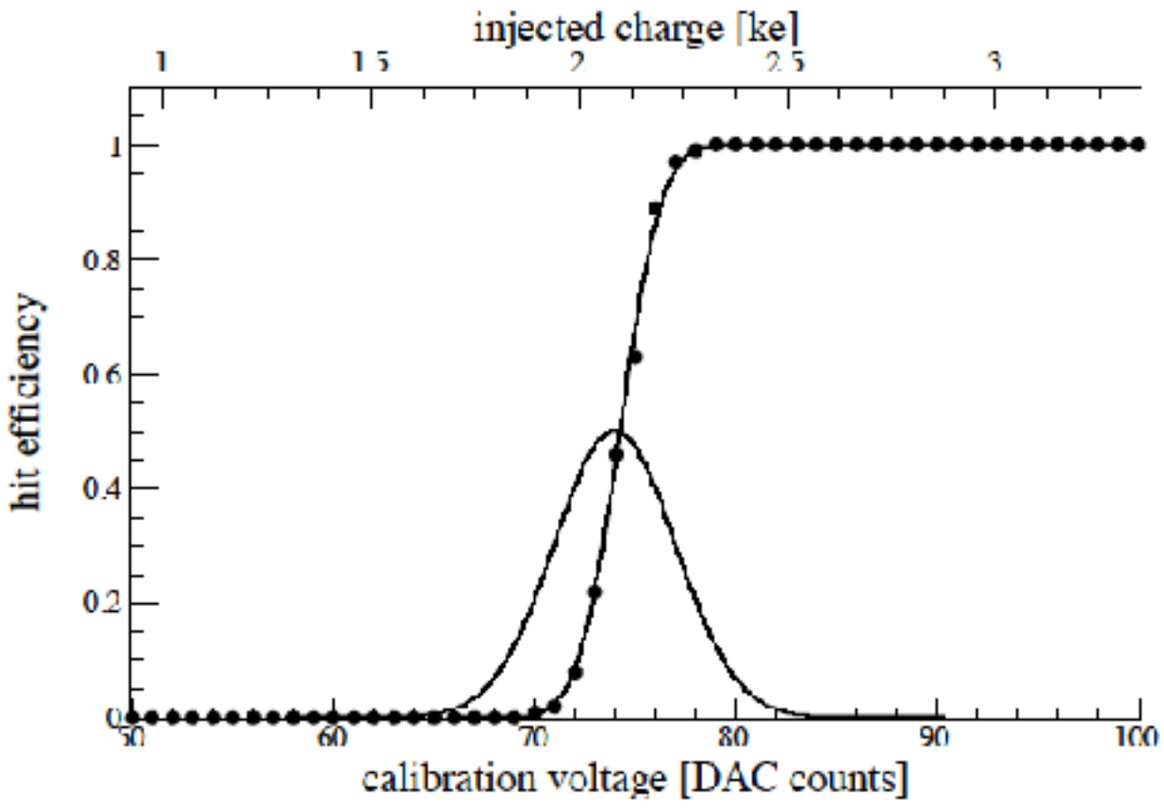
ADC - monitoring

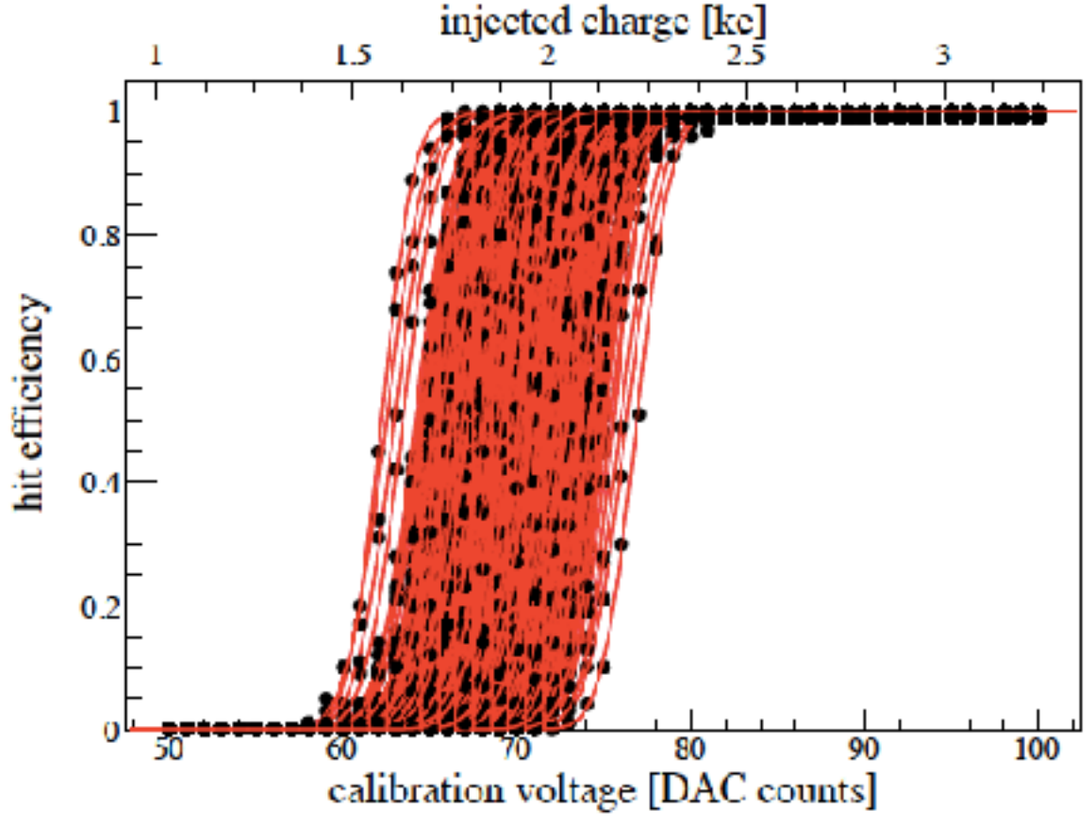


We can monitor via an internal ADC all:
- Bias currents
- Bias Voltage
- Cal Voltage



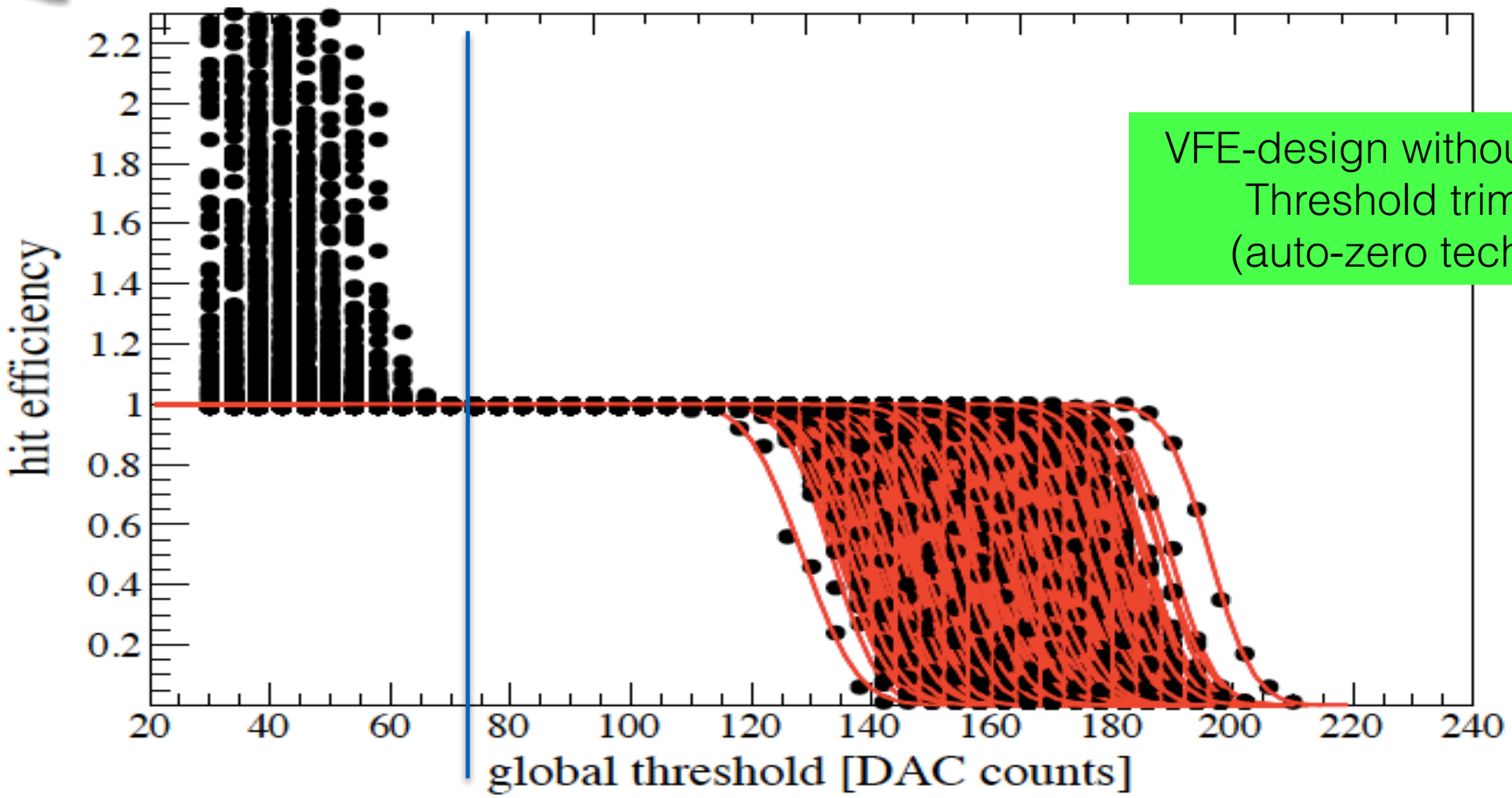
Measurement of Threshold and noise
S-Curve: Charge scan





- all pixels tested and fully working
- autozeroing performed each 200 μs
- effective NOISE and THRESHOLD values determined by means of S-curves
- measurements performed with CHARGE SCANS and FIXED THRESHOLD
- HIT EFFICIENCY recorded for 100 charge-injection pulses
- measured points fitted using an error function (sigmoid)
- noise and threshold values extracted from means and variances distributions

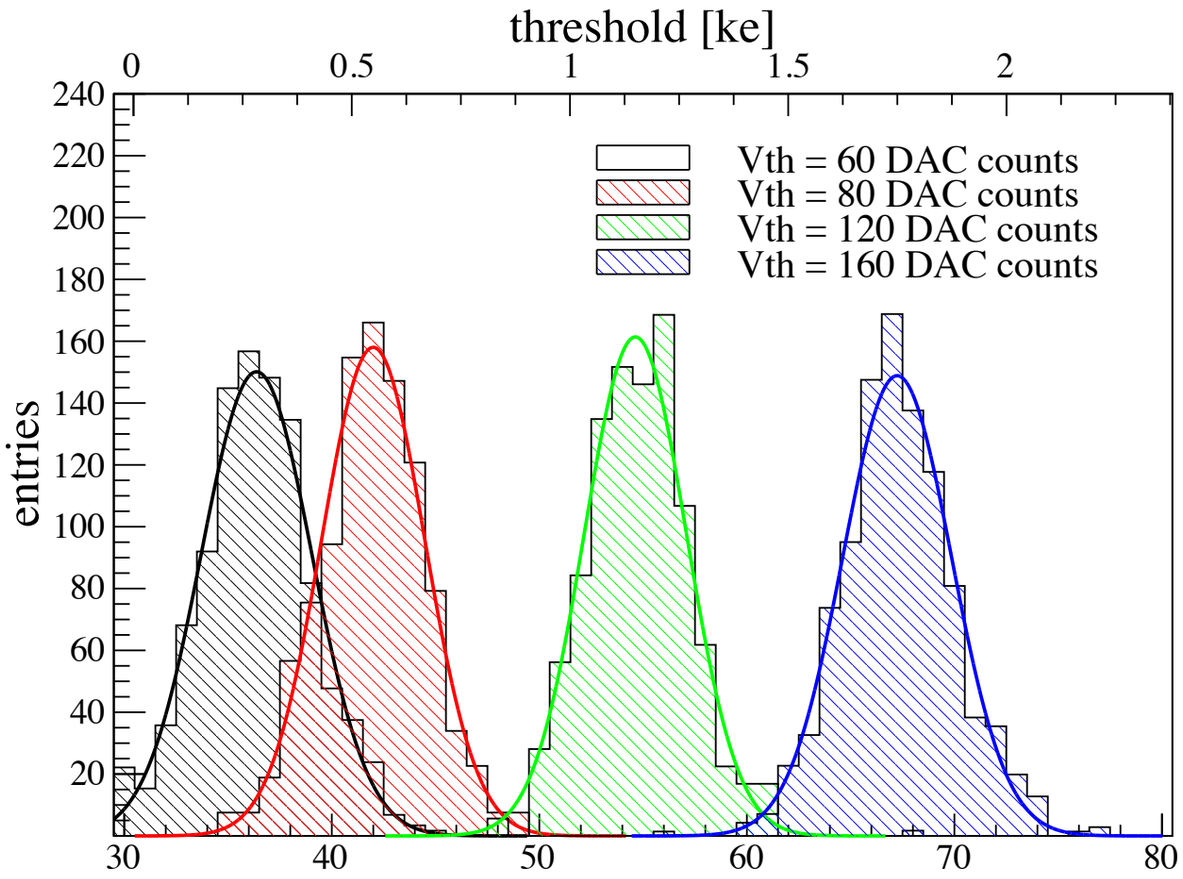
VFE-TO
Looking for lowest threshold



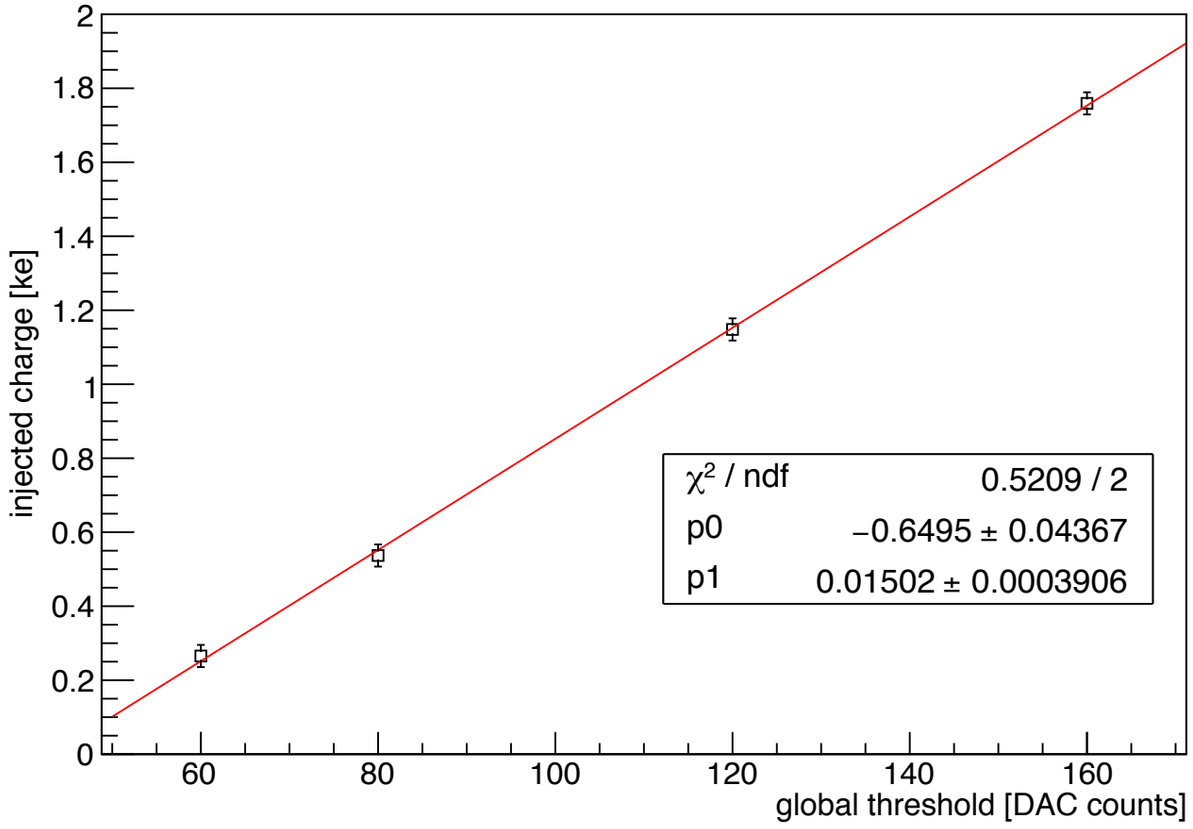
VFE-design without need of Threshold trimming (auto-zero technique)

- Vth=60 DAC-counts corresponds to 250 e- (see next slide)
- auto-zero : 75ns every 100 usec
- Calibration signal sent with random time distance from auto-zeroing
- no pixel has been excluded

VFE-TO
Threshold measurement



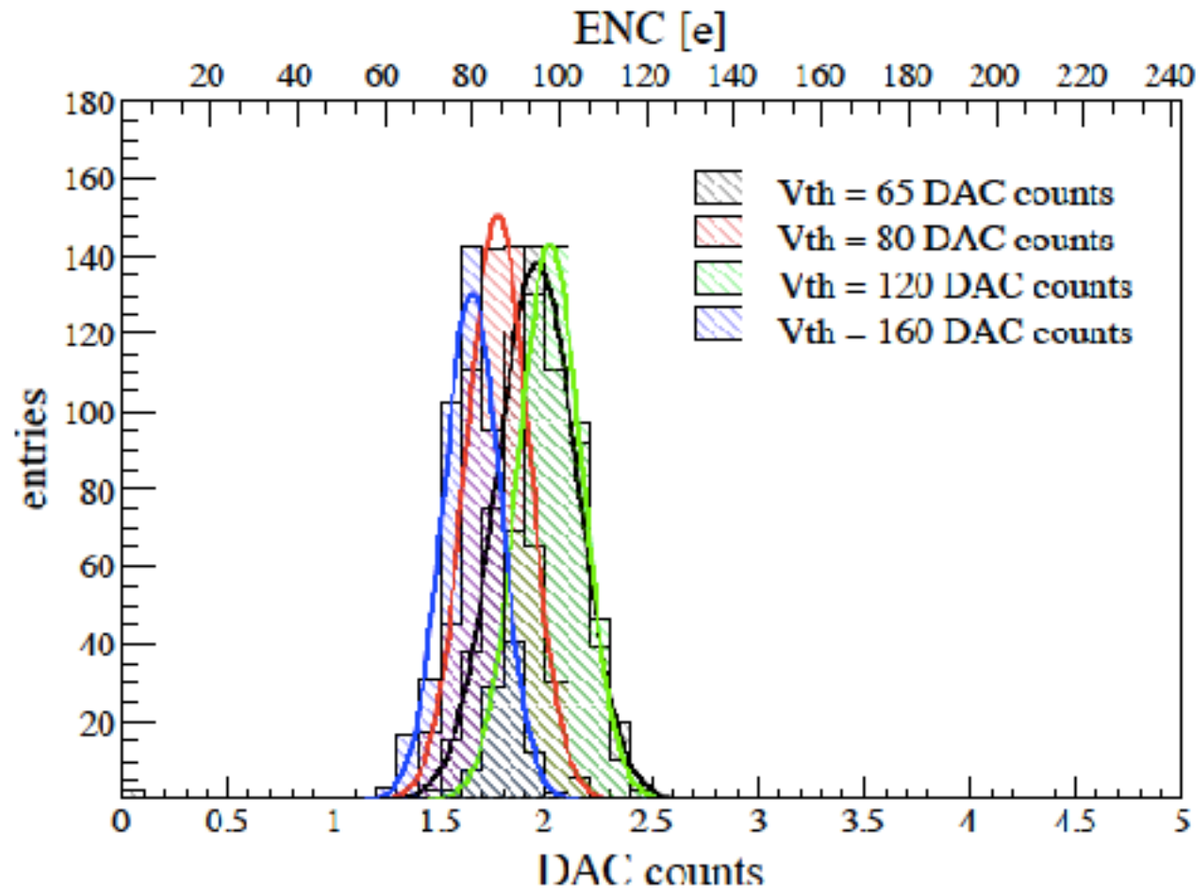
DAC counts

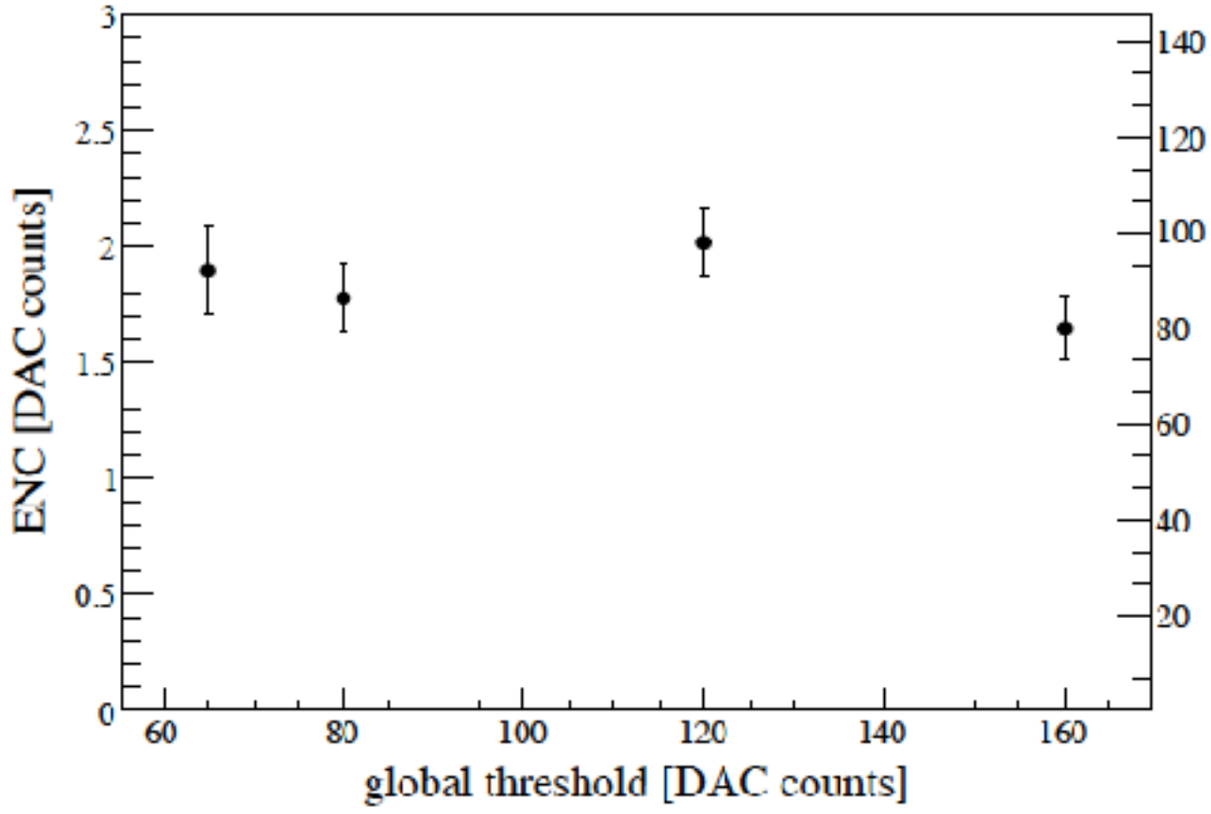


- **<threshold>=250e-** achieved
- no pixel excluded
- Dispersion of around 120e-

Charge threshold is linear with voltage difference at the discriminator

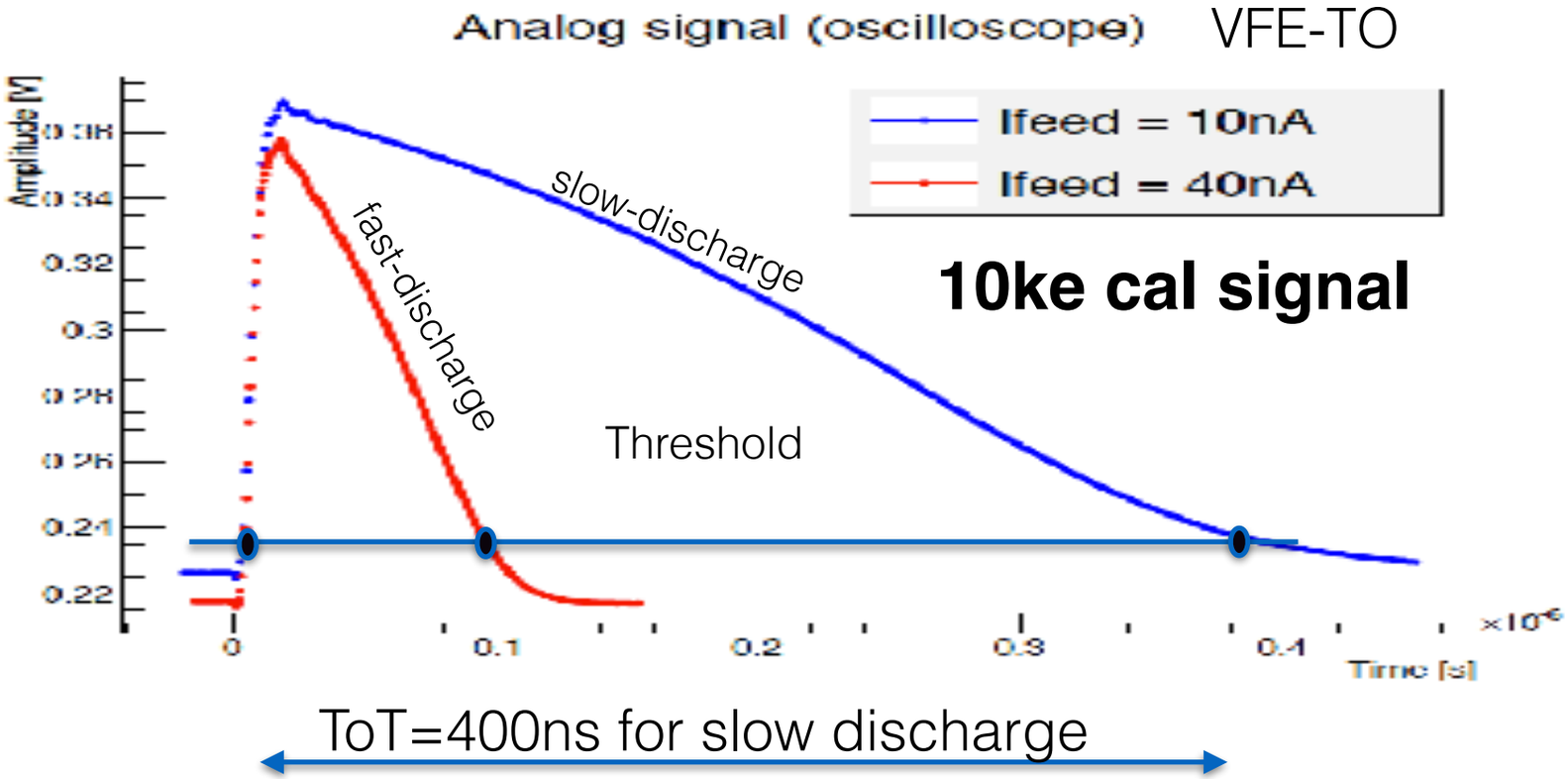
VFE-TO
Noise measurement





- ENC measured for different values of fixed global threshold
- constant behavior with threshold values as expected
- ENC ~ 90 e^- RMS in good agreement with CAD simulations
- very low-noise performance assured despite intense latch and region-logic switching activity

Analog - ToT counting

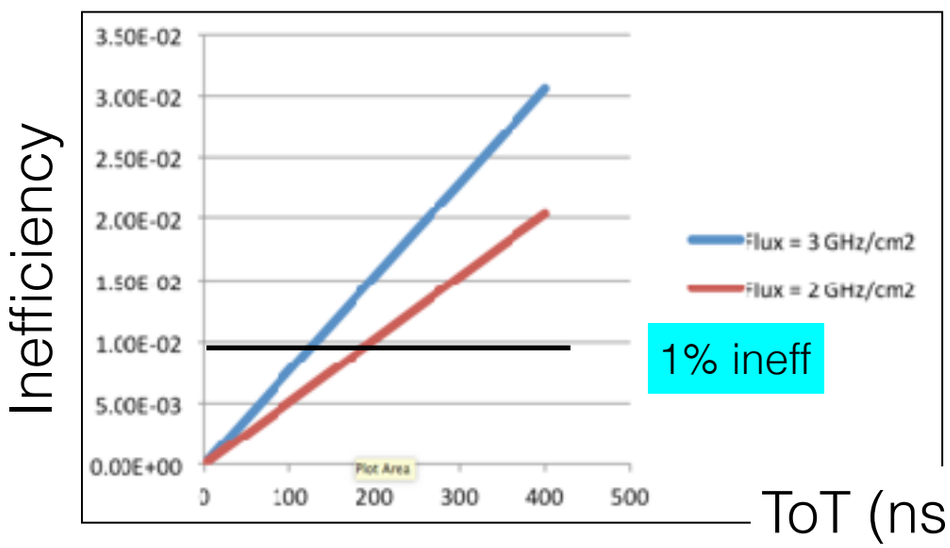


A clocked counter counts when signal above threshold :

- easy - small
- done per pixel
- low power

Cons: dead-time

Needed :
=> Fast Linear Discharge
Shorter signal
=> Fast Counting
TO get enough resolution

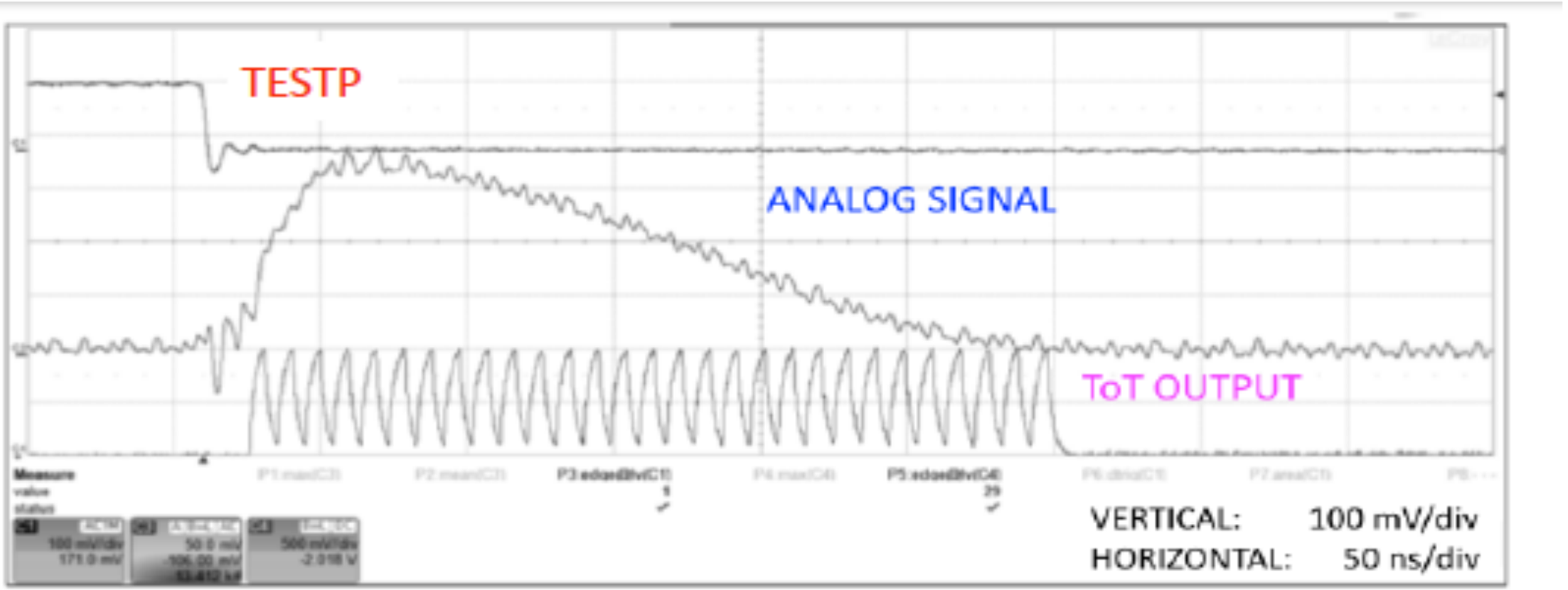


TO OBTAIN <1% inefficiency from Analog pile-up

1.<ToT_pix> should be < 135ns

2. For 4-bit (600e-) ToT counter @ > 60 MHz

VFE-TO
Fast ToT counting

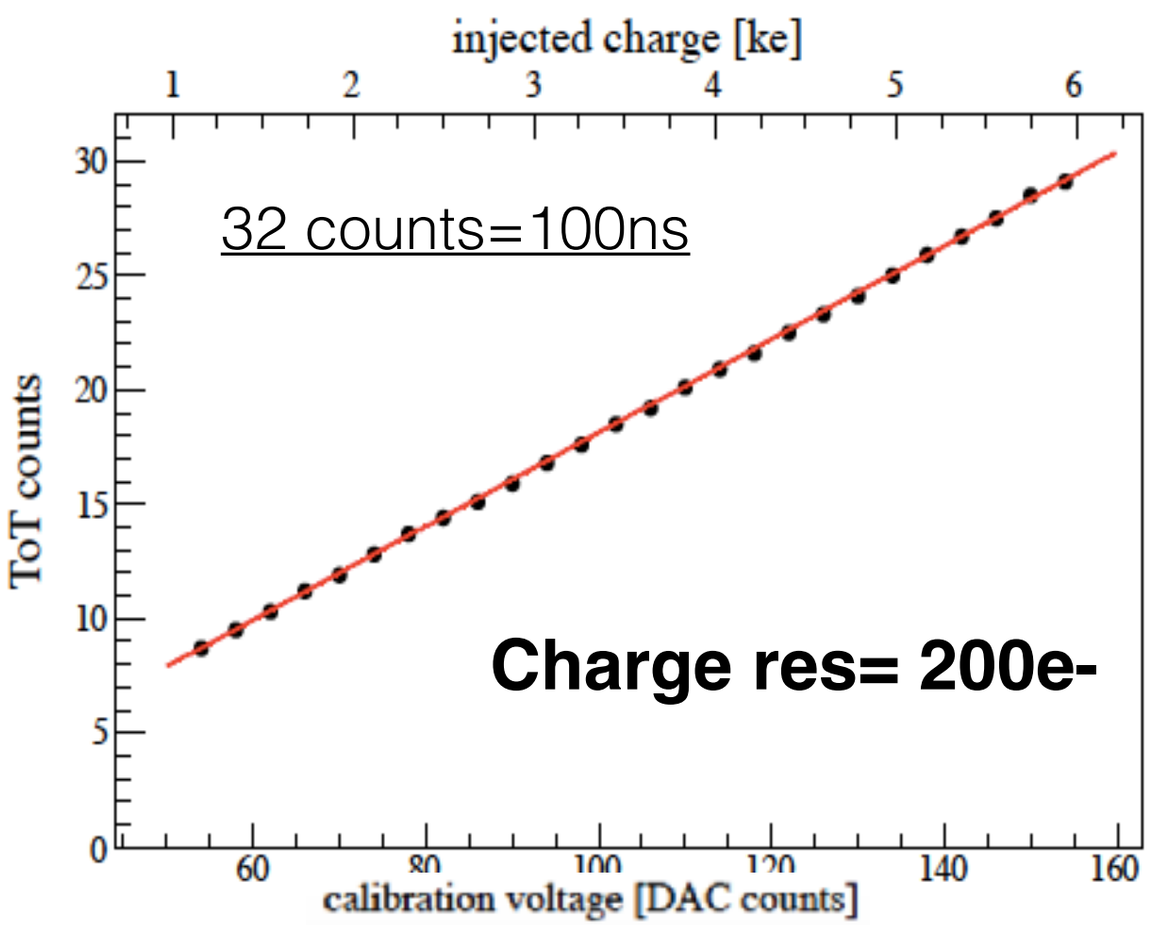


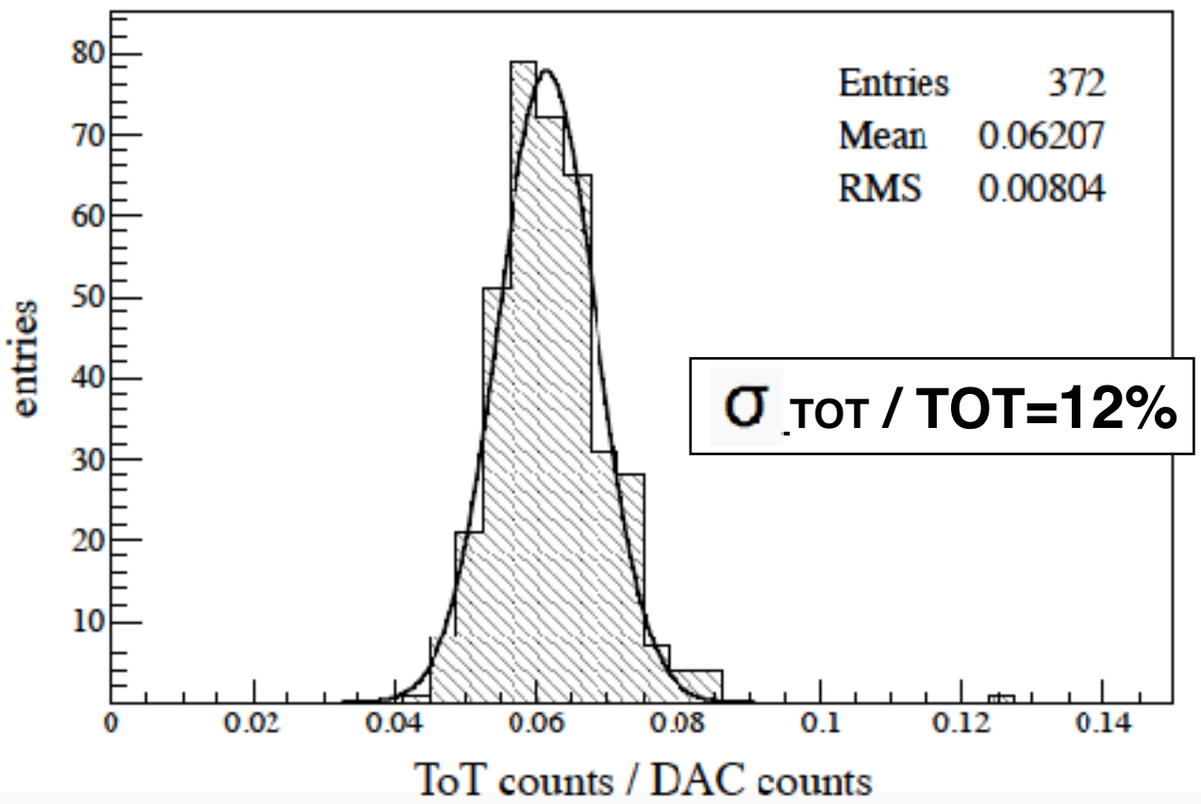
A signal above discriminator threshold start a local oscillator (rough VCO) with a frequency controlled by a 10-b DAC.
The increase of power is of around 5% (0,2 uW/pix) at 3 GHz/cm2

VFE-TO
Fast-ToT measurements

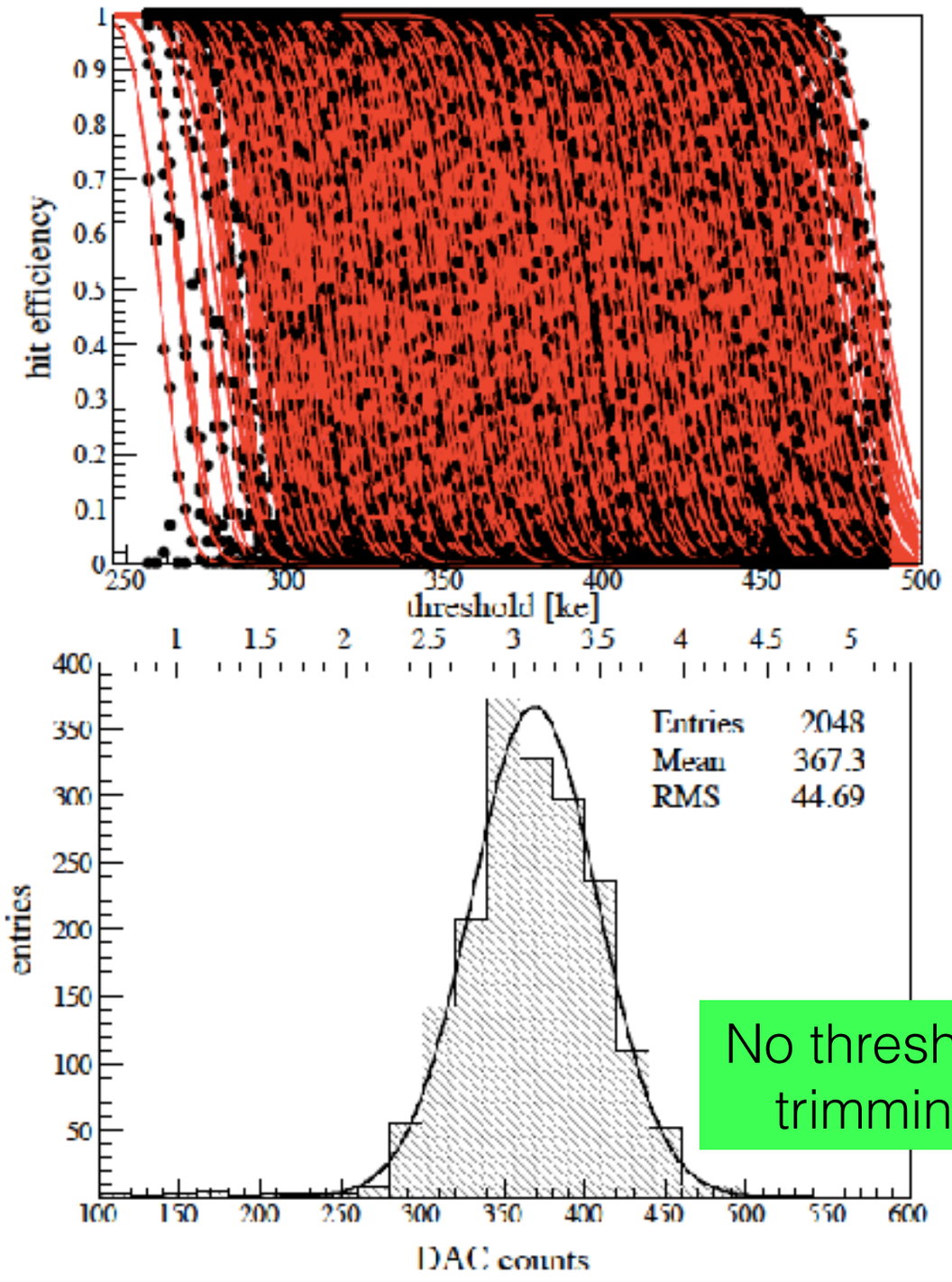
- Good ToT Linearity - 5 bit ToT
- Here shown measurement with 320MHz Fast ToT
- Fast-Tot-clock frequency can be varied via a 10-bit DAC

- Slope dispersion of about 12% expected from mismatch in I-Feed



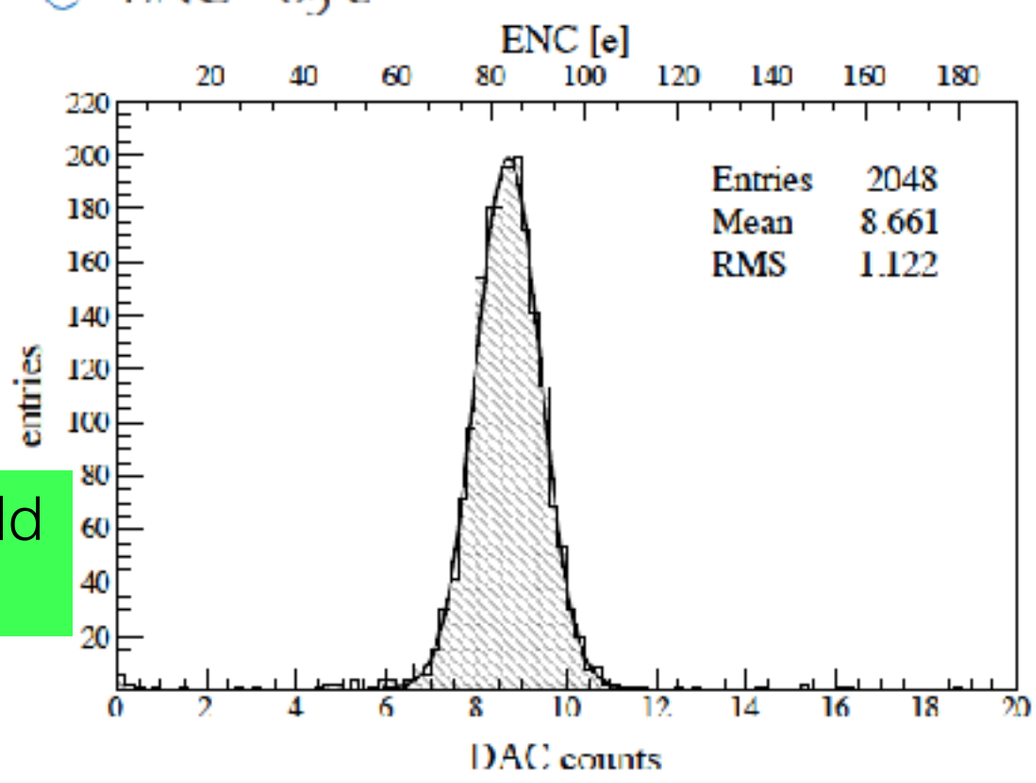


VFE-BG/PV
Threshold and noise

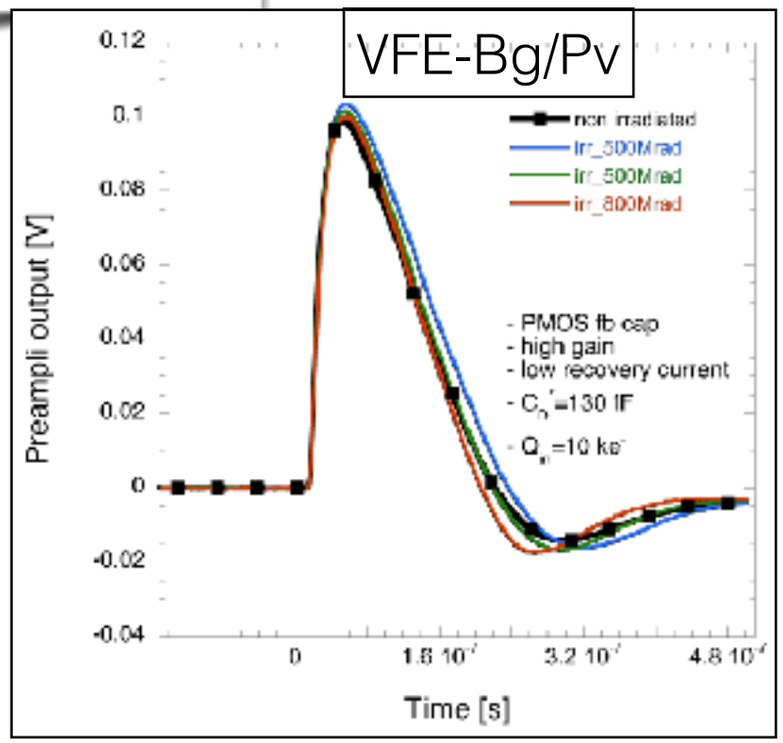


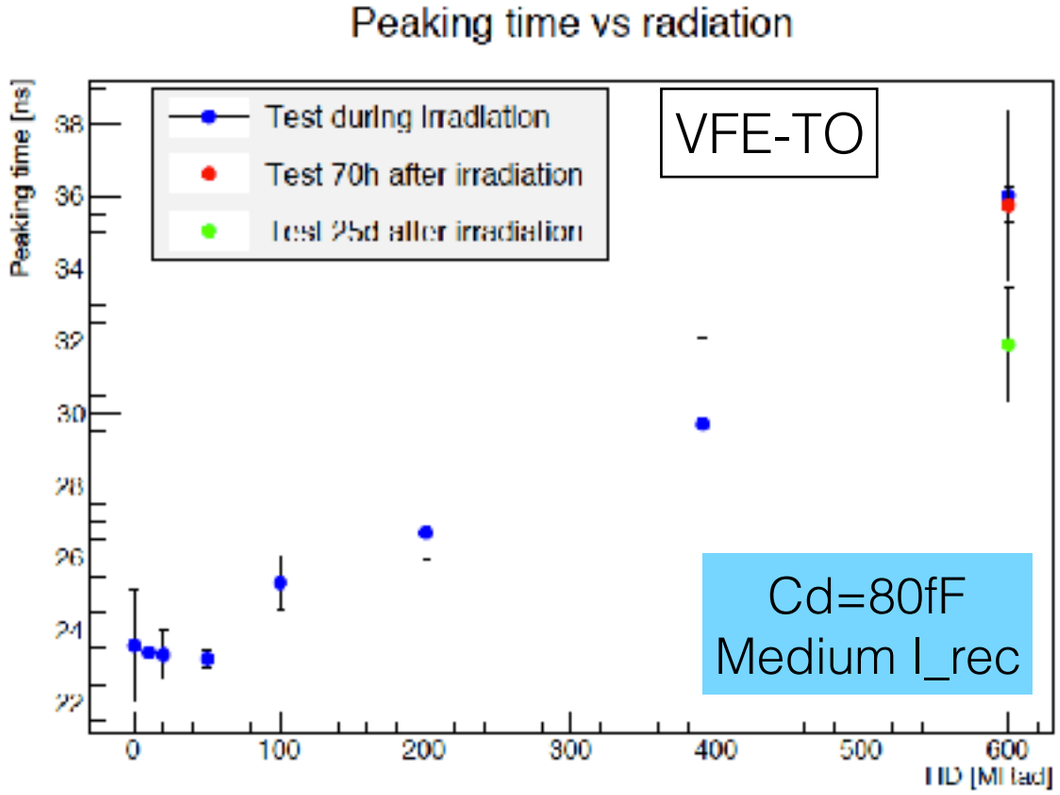
- all pixels tested and fully working
- untrimmed threshold dispersion
- preliminary results indicate ~400 e^- threshold dispersion, in agreement with CAD simulations
- automated calibration algorithm not yet supported by DAQ interface
- ENC ~85 e^-

No threshold trimming



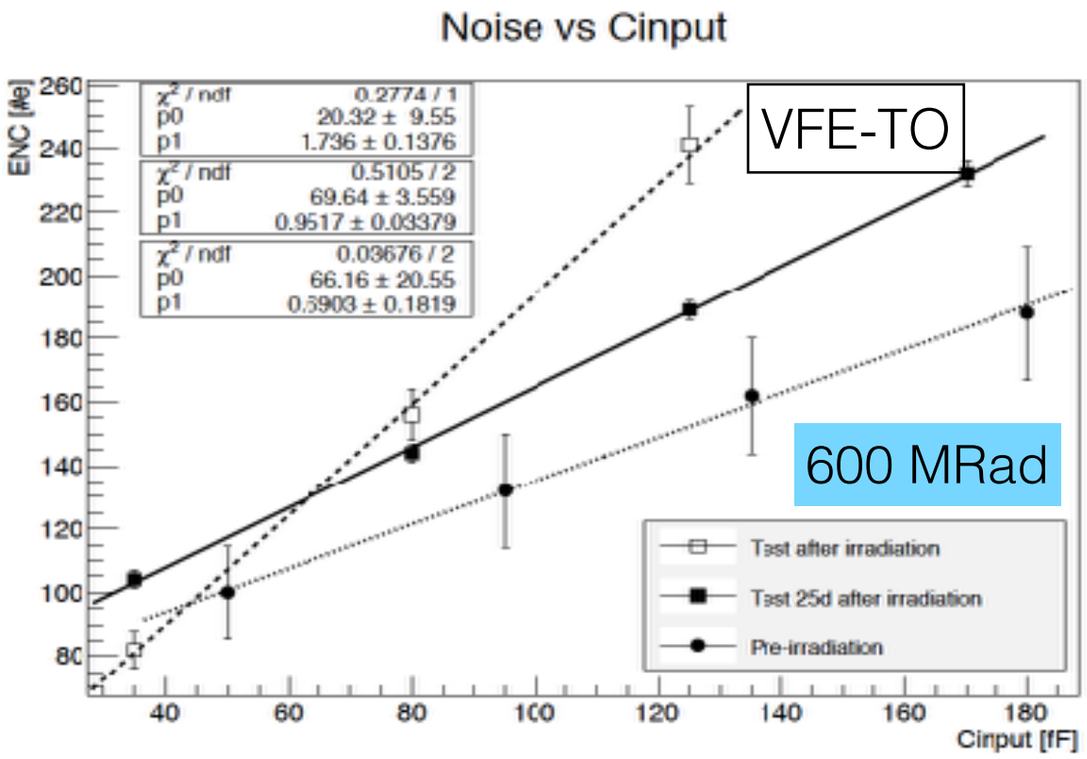
VFEs are rad-hard

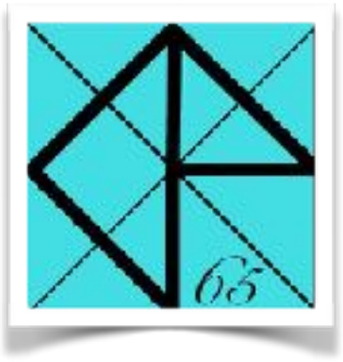




- No major worry: **analog-architectures tested under radiation** and no serious problem seen

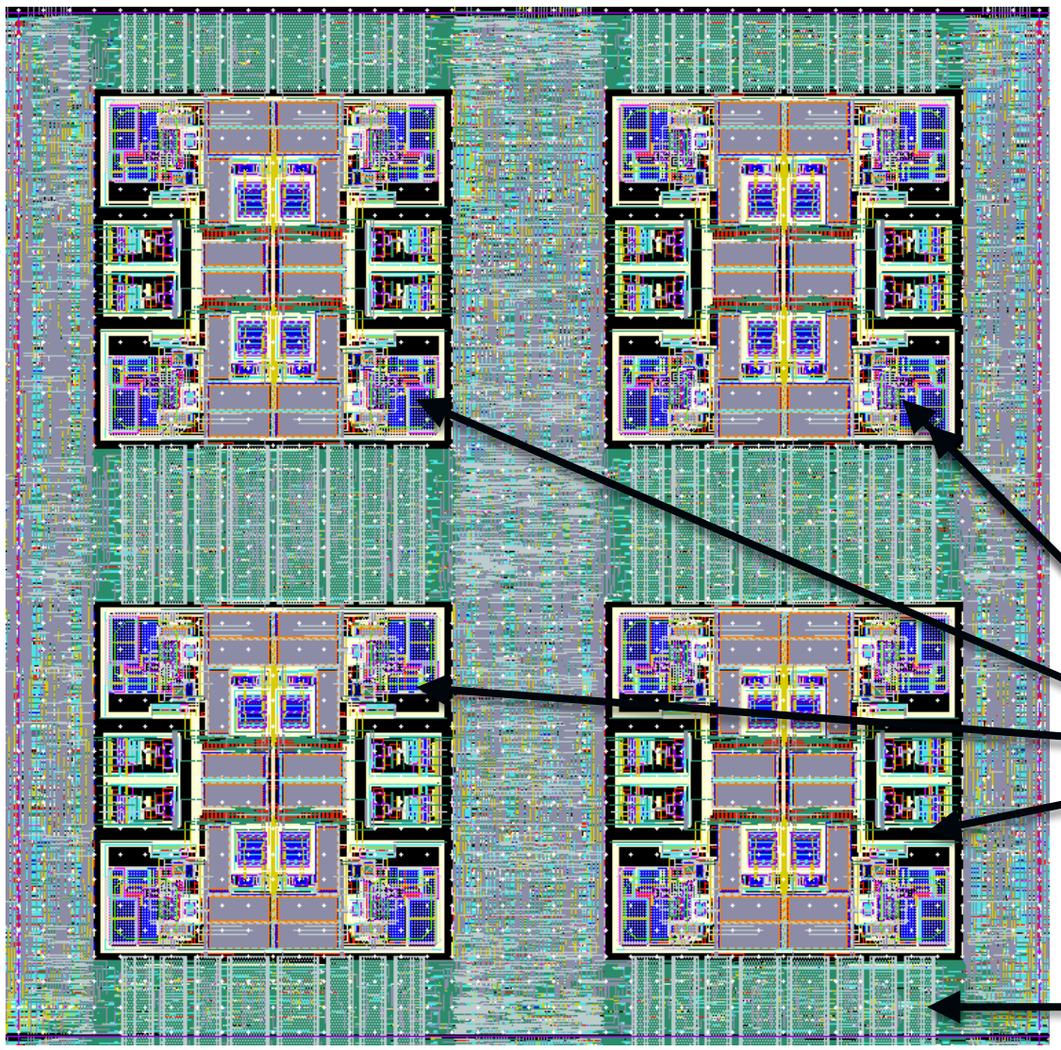
- Gain decrease of ~5%
- Slower signal but looks ok
- 10-20% increase of noise





CHIPIX65 digital architecture

CHIPIX65 Regional architecture extended to (4x4) pixels



Pixel region provides :

- pixel configuration register
- ToT counting
- Local storage waiting trigger
- Trigger matching (zero-suppr)
- Readout to end-of-column

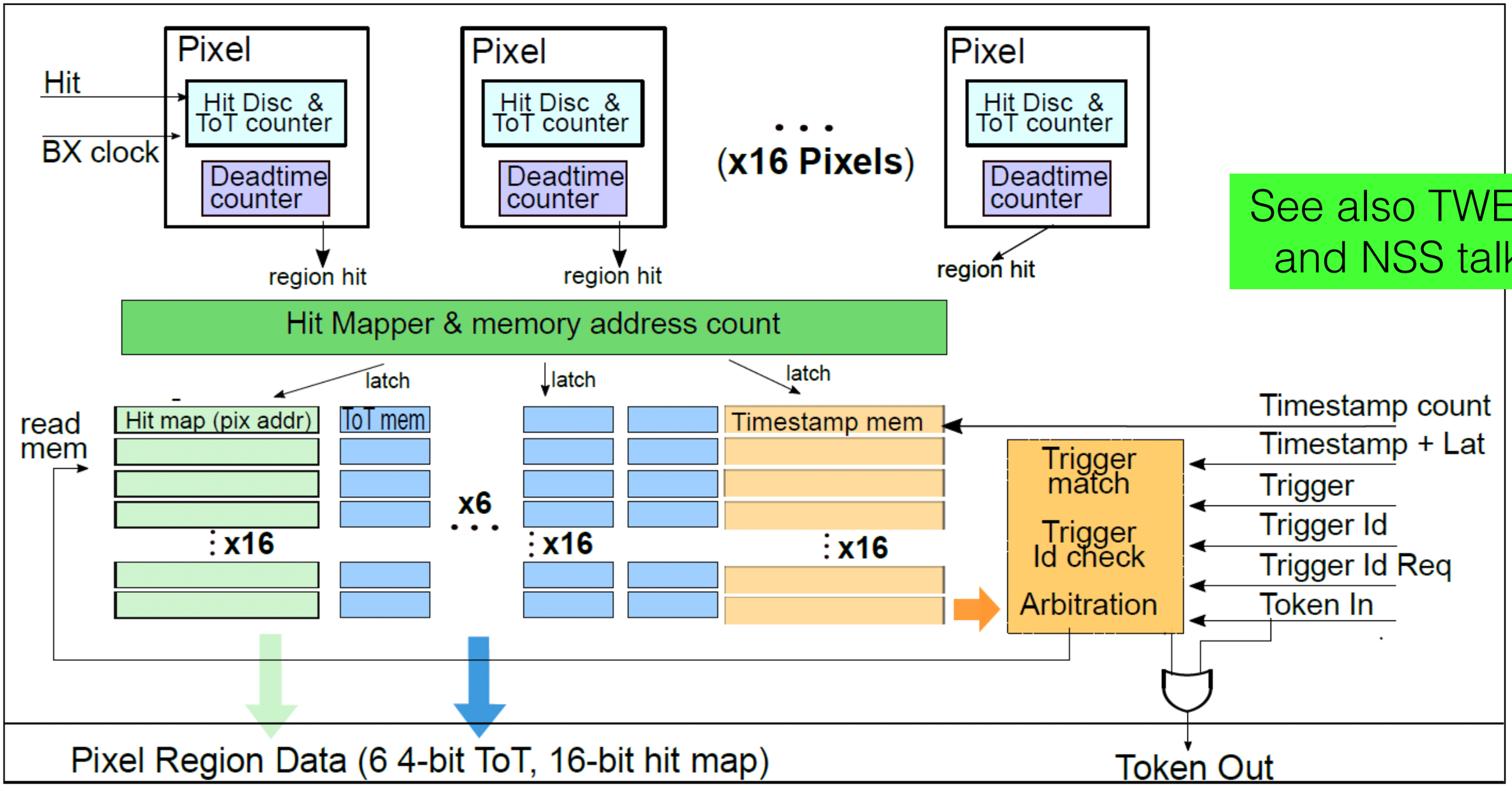
Analog VFE in four (2x2) islands

Digital architecture logic distributed in the (4x4) Region

AREA for digital is tight: idea is to make real use of sharing digital resources among more pixel

- FEI4 architecture NOT convenient for regions larger than (2x2)
- NEW architecture developed by CHIPIX65 based on (4x4)

CHIPIX65
Novel digital architecture



See also TWEPP and NSS talks

CHIPIX65 architecture performance @ 3GHz/cm^2

Metrics	**4x4 PR architecture**		**2x2 PR architecture (1x4)**	
	40MHz FE	*128MHz FE*	*40MHz FE*	*128MHz FE*
Hit loss due to dead time (%)	3.19	0.94	0.72	0.42
Hit loss due to buffer overflow (%)	*16 loc.*: 0.24	*16 loc.*: 0.29	*8 loc.*: 0.74 (0.57)	*8 loc.*: 0.76 (0.57)
ToT loss due to limited ToTs (%)	0.10	0.11	–	
Total hit loss (%) *(ToT loss excl.)*	***16 loc.*: 3.44**	***16 loc.*: 1.23**	***8 loc.*: 1.46 (1.29)**	***8 loc.*: 1.19 (0.99)**

Today Status

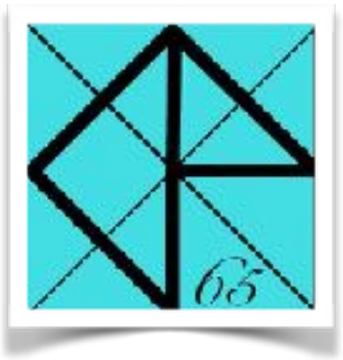
Low Power and area saving

…now moving to better efficiency

CHIPIX65 architecture				
Analog	Power 3GHz/cm2, Tr=1 MGHz uW/pix	Power with 0 GHz/cm2, No Trigger uW/pix	AREA um2	AREA %
VFE-asynch	4,51	4,05	876	68%
VFE-TO (synch) 40MHz ToT	4,52	4,25	860	68%
VFE-TO (synch) Fast ToT	4,73	4,25	idem	idem

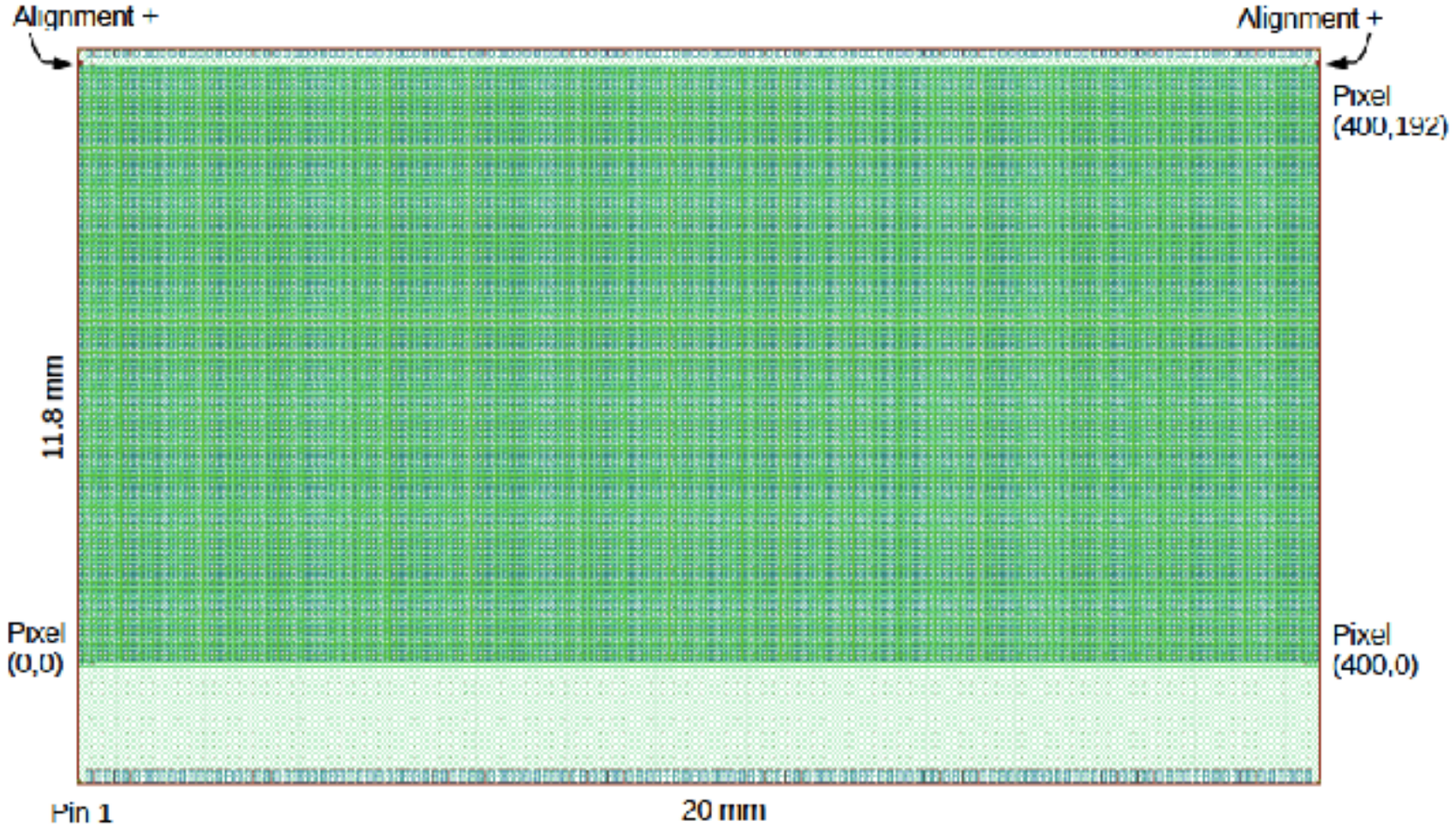
gain of 15% in area

CHIPIX65 architecture - VFE-TO FastToT		
#bit	Power 3GHz/cm2, Tr=1 MGHz uW/pix	AREA %
4-bit ToT	4,73	68%
5-bit ToT	4,96	73%
6-bit ToT	5,62	79%



Next Steps

RD53A



- Large size prototype chip
- Base-line for CMS and ATLAS chip

Submission foreseen:
Spring 2017

We just had 1-day design review (Tuesday) with external reviewer:
==> very positive outcome

Large Design team:

- coordination: F.Loddo (INFN-Ba)
- deputy: T.Hemperek (Bonn)
- about 13 designers - (7 from INFN)
- Weekly meeting
- from middle January ALL at CERN for finalisation and verification work

Parameter	Typ.	Max.
Core direct supply voltage	1.2 V	1.32 V
ShuLDO input voltage	1.5 V	2.0 V
Per pixel analog current	4 μA	8 μA
Per pixel digital current	4 μA	6 μA
RD53A Periphery analog current	30 mA	60 mA
RD53A Periphery digital current	30 mA	60 mA
Output drivers (each)	20 mA	30 mA
Total RD53A current (4 outputs)	0.75 A	1.3 A
400x384 chip periphery analog current	50 mA	100 mA
400x384 chip periphery digital current	60 mA	120 mA
Total 400x384 chip current (4 outputs)	1.4 A	2.5 A

Table 1: Power supply limits

FROM SMALL demonstrators towards RD53A)

Characteristics	FE65P2	CHIPIX65-FE0	RD53A
Pixel Matrix	64x64	64x64	400x192
Matrix Organization	(2x2) analog islands Pixel Regions (4x64) COREs	(2x2) analog islands Pixel Regions (4x4) COREs	(2x2) analog islands Pixel Regions (8x8) COREs
Pixel Regions	(2x2) pixels distributed data buffer trigger matching	(4x4) pixels centralized data buffer trigger matching	(2x2) & (4x4) pixels tbd trigger matching
VFE	VFE-1	VFE-2 VFE-3	VFE-1, VFE-2 VFE-3,
Analog-Digital Isolation	Analog triple well. .Digital triple well .	Analog triple well	Analog triple well Digital triple well
Signal Digitisation	4-bits	binary or 5-bits	4 or 8 bits
. Building Blocks	few not RD53	. BandGap, DAC, ADC SER, sLVS-Tx/Rx.	BandGap, DAC, ADC Ana-Buffer, PON-reset, Sh-LDO sLVS-Tx/Rx, Cable Driver, PLL-CDR, Temp Sensor
Bias-Distribution	Single stage mirroring	Double stage mirroring	Double stage mirroring
Radiation hard design	Analog	Analog	Analog and Digital
Powering	Standard	Standard	Serial-Powering

Conclusions

- A CMOS 65nm FE ASIC is the only viable solution for inner layers of Phase 2 pixel detectors and it is also a preferable solution for the other layers overall.

- CHIPIX65 project has boosted the INFN towards the use of CMOS 65nm and to work a real application for a Pixel Phase 2 readout ASIC. High level, effective and innovative contributions to all the aspects and measured in the framework of RD53 international collaboration

- A CHIPIX65_FE0 first results are VERY promising: works low threshold (250e-), Fast-ToT, 2 VFE, IP-blocks
    - irradiation test in early 2017; bump-bonding foreseen to planar / 3D

- INFN / CHIPIX65 is essential for the RD53A design and test

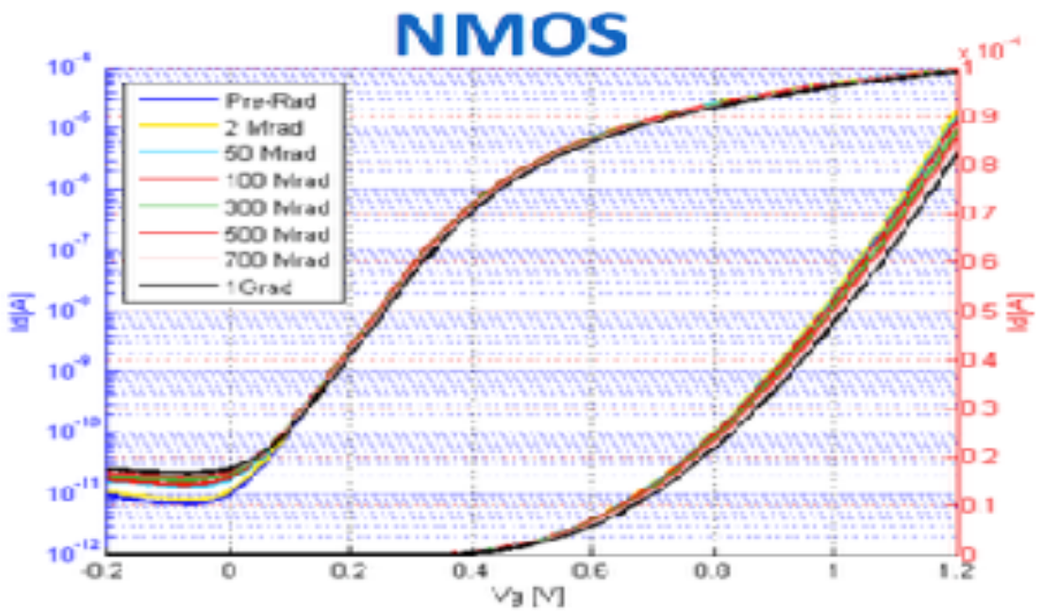
- Now we have matured enough experience in INFN to continue after RD53A to design the future ASIC for the Phase-2 Pixel detector

Radiation Effects

Total Dose effects

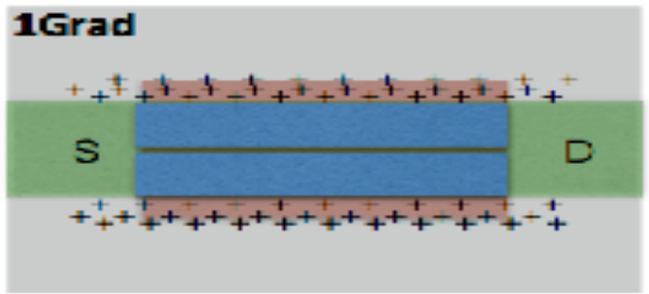
TID has no effects on

- Vth does not change - gate oxide is rad-hard
- CMOS leakage current (Ids) - STI stop current flowing

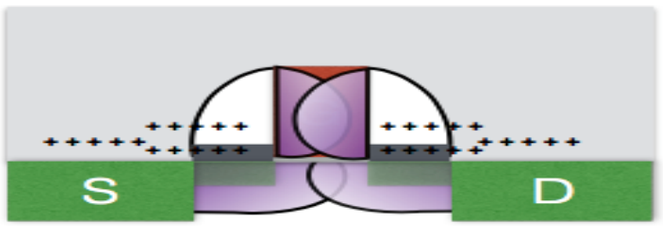


TID HAS effects on small gates (L or W)

- **RINCE** (small W) and **RISCE** (small L) effects
  - Max current (I_{on}) decreases
  - Transconductance decrease (G_m)
- Effects mainly on small size CMOS, i**mpact on minimum size digital circuits**



L=min size

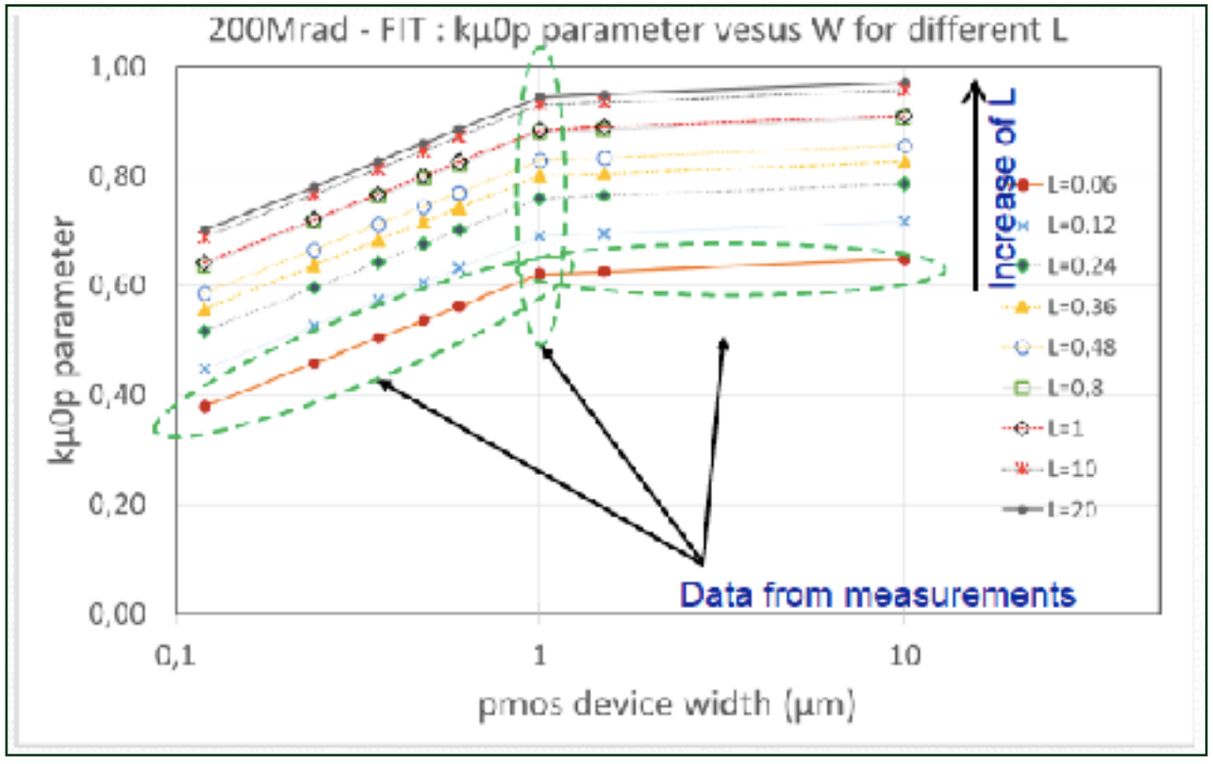


Modeling radiation damage

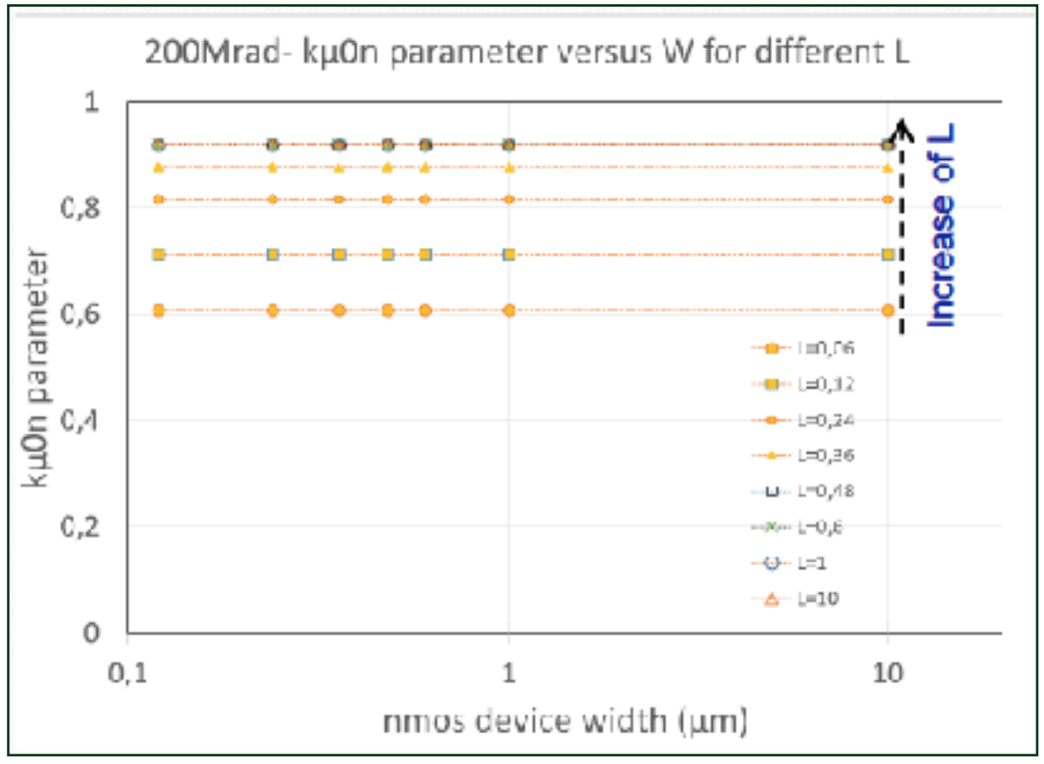
All data measured by RD53 on CMOS are fitted using a simple model.
Very power tools to verify all the design of IP-block, VFE and digital circuitry

The mobility factor kμ0n is defined as μ0_rad/μ0_prerad

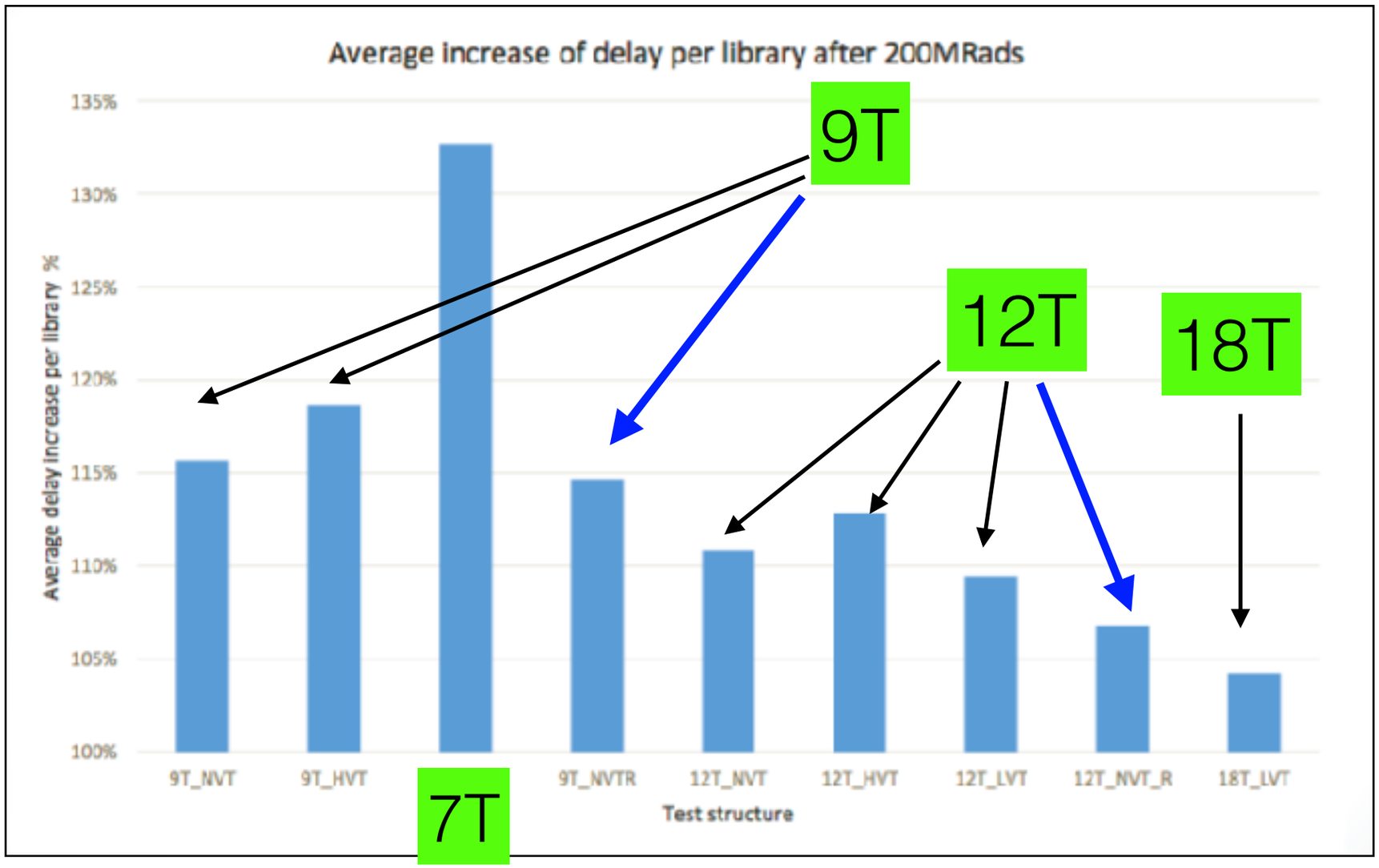
P-MOS modeling fitting data



N-MOS modeling fitting data



DRAD : first results



NEXT Steps:

- Repeat tests with cooling:
  - 200 MRads with cooling.
  - 1000 MRads with cooling.
- Radiation campaign up to 500MRads.
- Continue with the current annealing testing and annealing at 100˚C.

CELL HEIGHT

7 Track: 1.4 uM

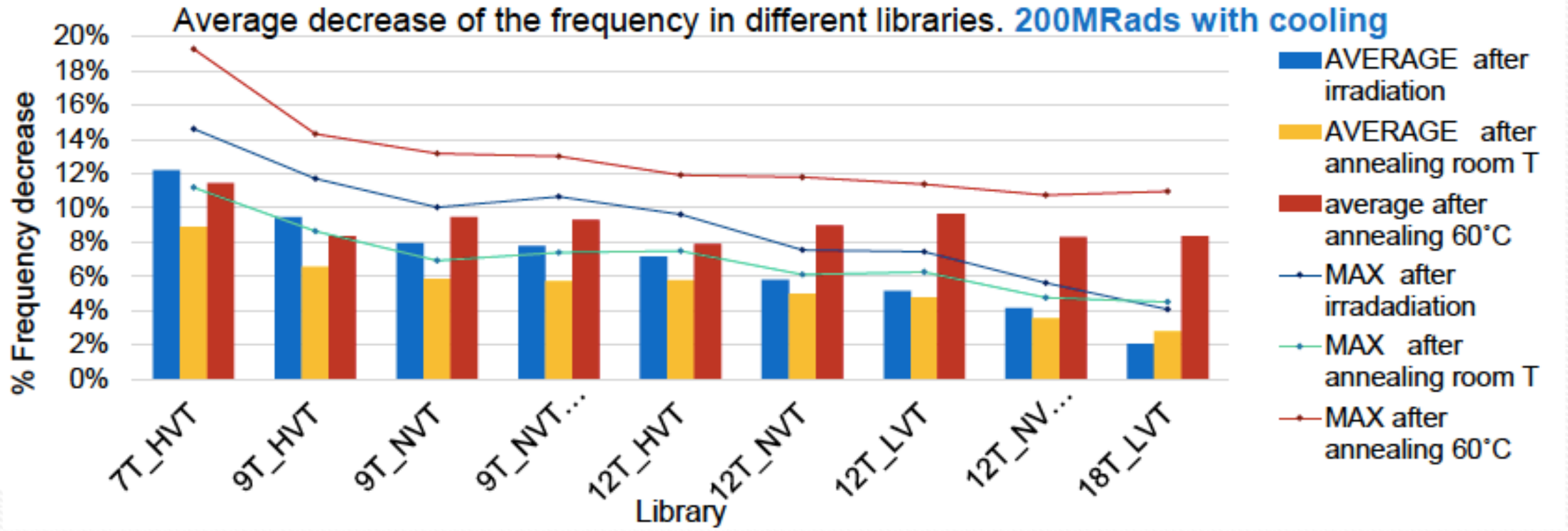
9 Track: 1.8 uM

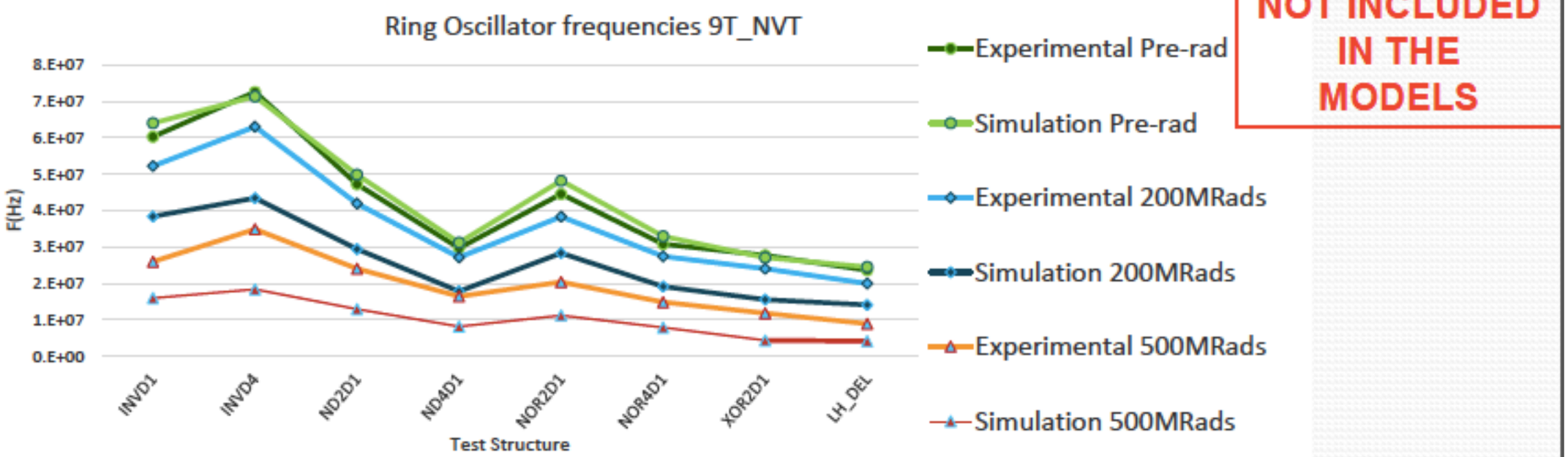
12 Track: 2.4 uM

18 Track: 3.6 uM

- 9T is the digital library for Pixel-Matrix (7T cannot be used)
- so far results in agreement with simulation models derived from single MOS radiation characterisation results

Damage in digital

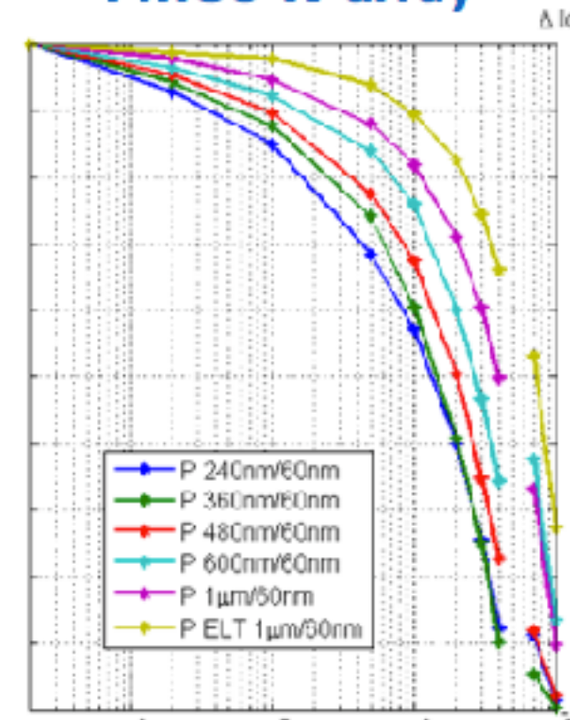




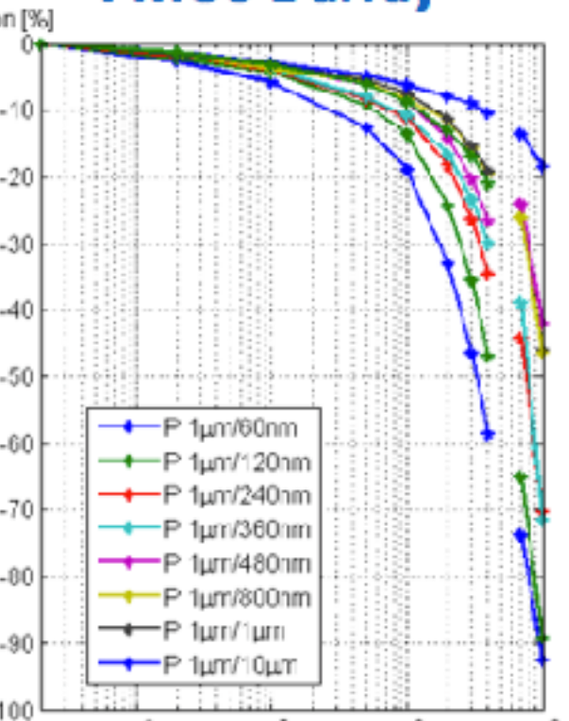
ANNEALING NOT INCLUDED IN THE MODELS

Radiation-Induced Narrow Channel Effect (RINCE)
Radiation-Induced Short Channel Effect (RISCE)

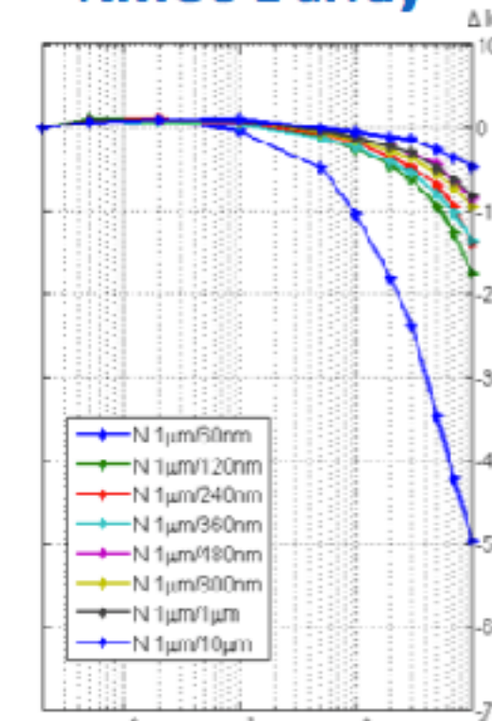
PMOS W array



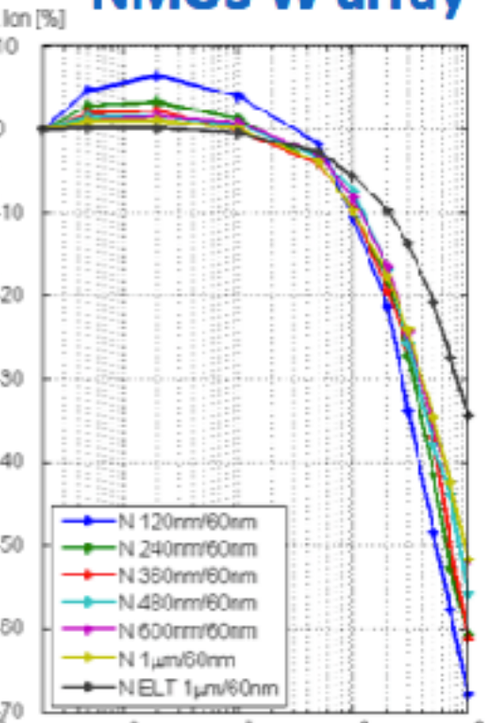
PMOS L array



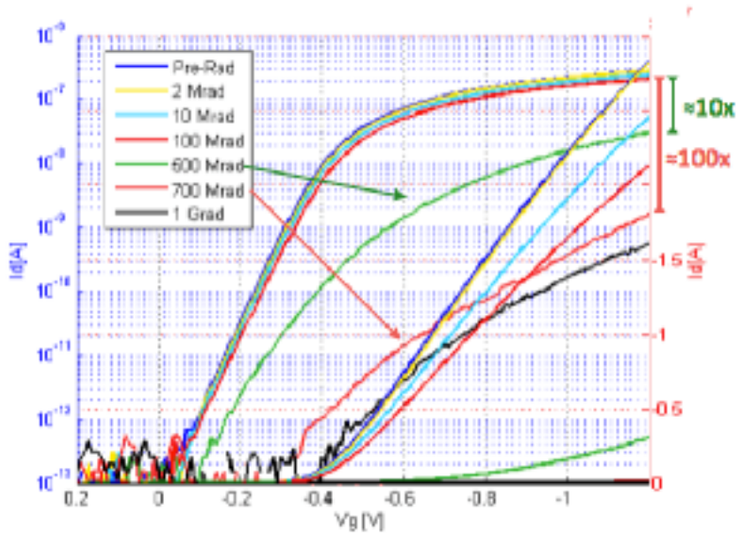
NMOS L array



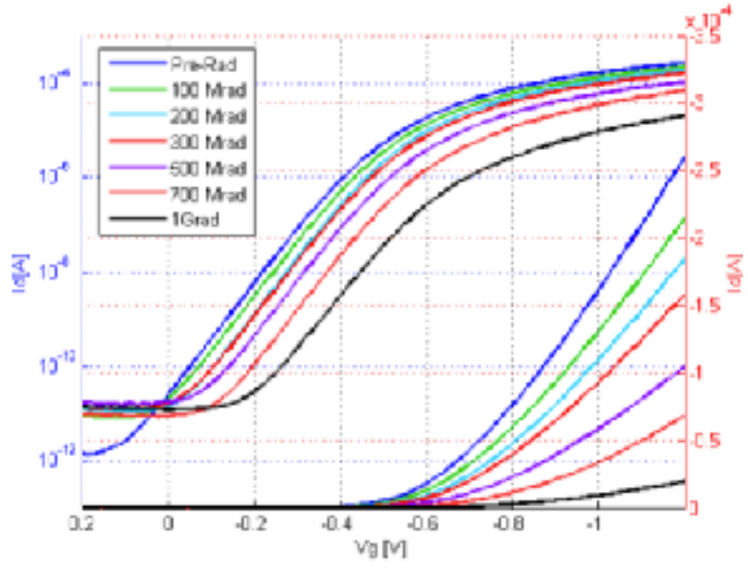
NMOS W array



PMOS



PMOS



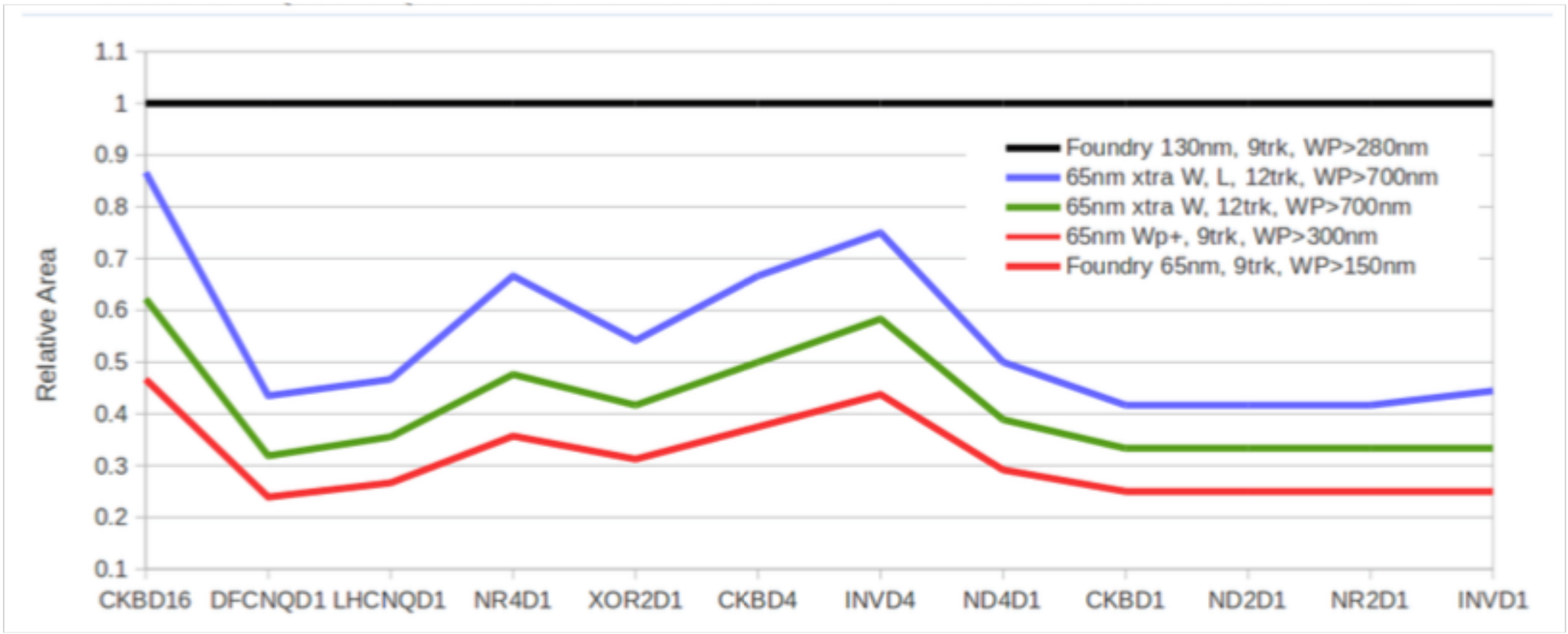
RINCE:
narrow PMOS do not work above 500 MRad

here L=1um, W=120nm

RISCE:
short PMOS more affected than NMOS, but not a big problem

here L=60nm, W=1um

Area Comparison

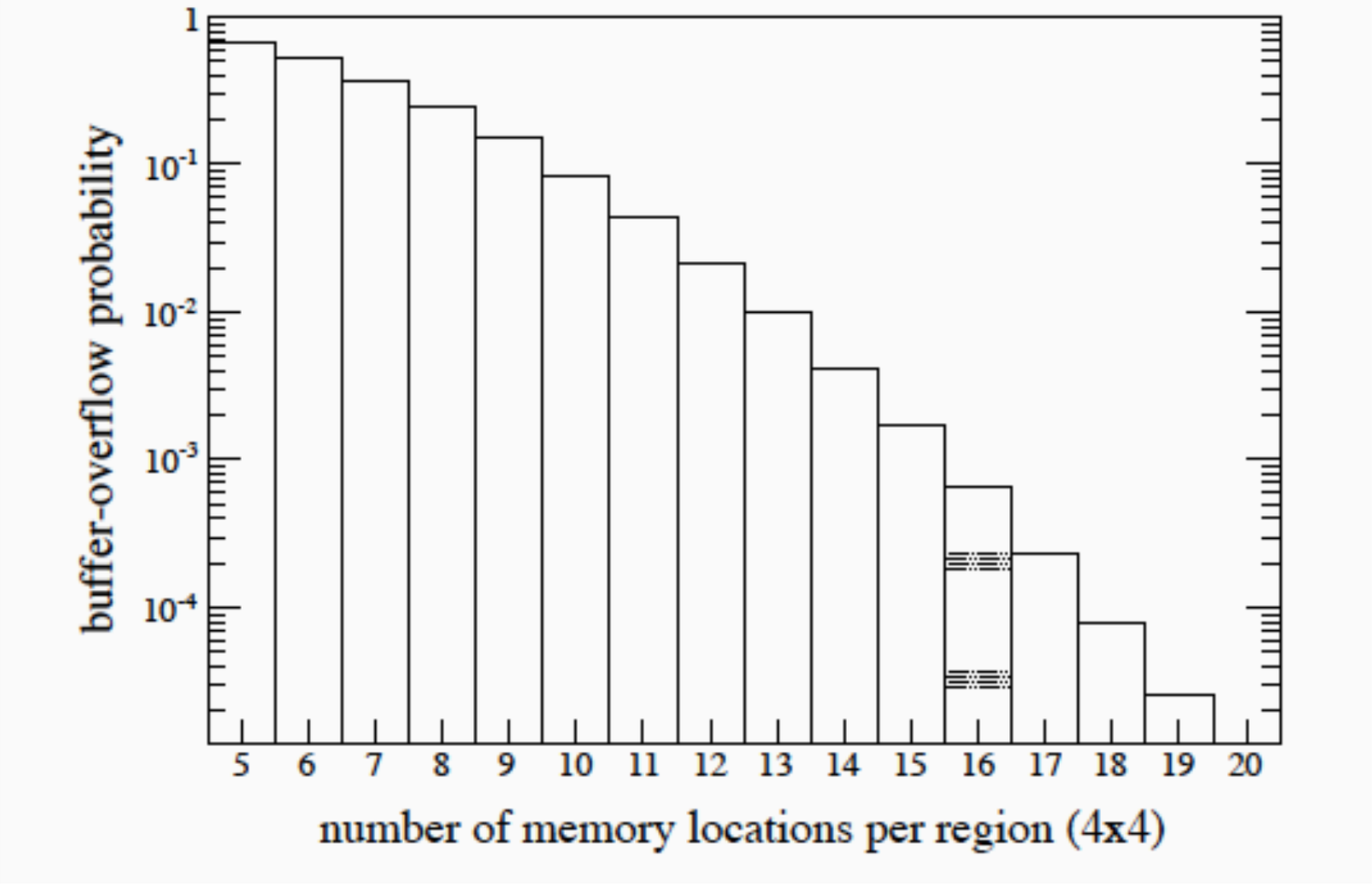


Are MODIFIED 65nm digital cell convenient w.r.t. 130nm ?

YES !

AREA GAIN of : 3-4 times for Standard-lib (with minimal W increase);
2-3 times for Enlarged 12T

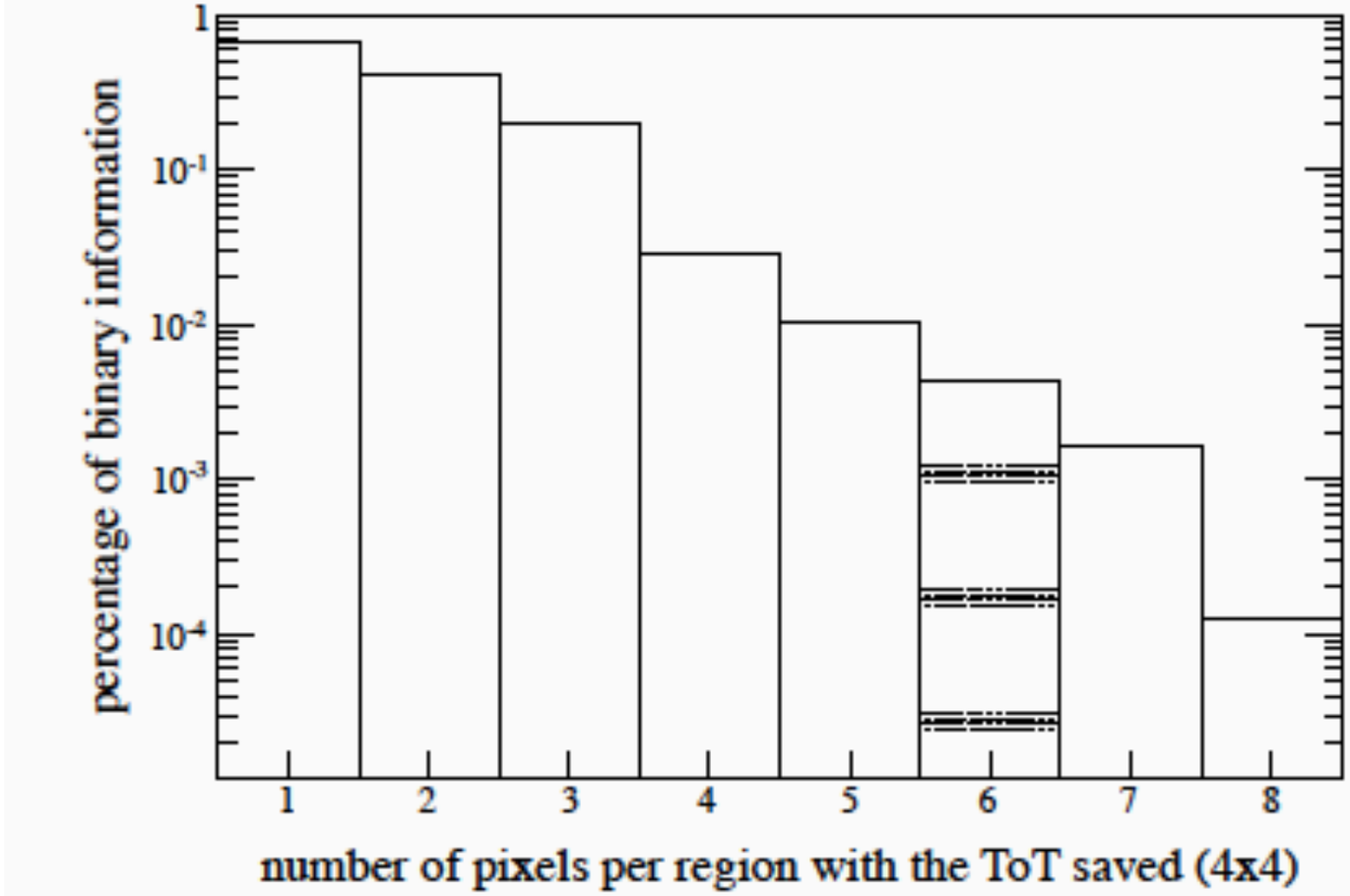
Hit losses from Latency buffer depth



#LOC=15 : 0,16%
#LOC=16 : 0,06%

- Depth of memory buffer =16 provide negligible losses
- We could implement ‘double’ locations for low rate / higher resolution ? (low priority work)

Binary INFO due to limitation in latency buffer width

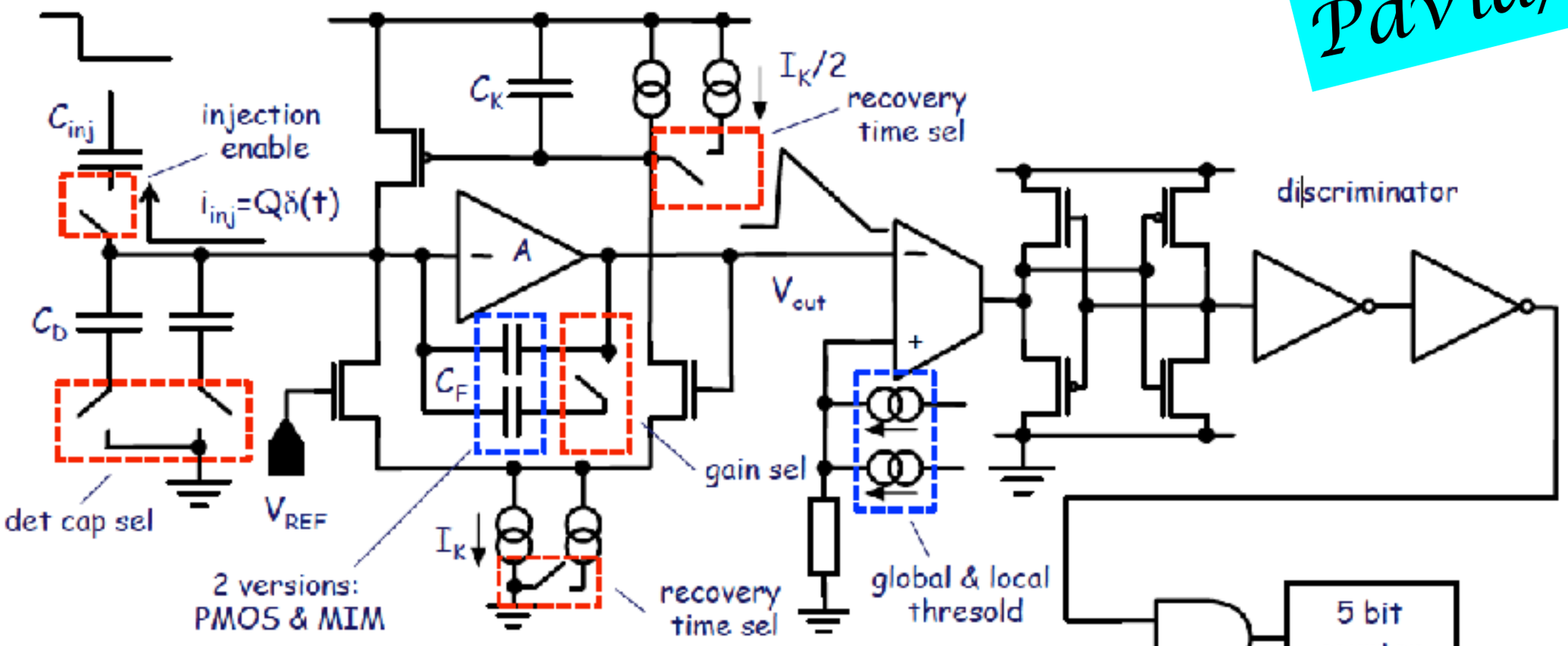


6 PIX: 0,4% binary info
4 PIX: 1,1% binary info

- This is NOT a hit loss: binary info STILL available
- Possible to ‘compress’ saturated channels (to be studied)

Asynch Analog FE

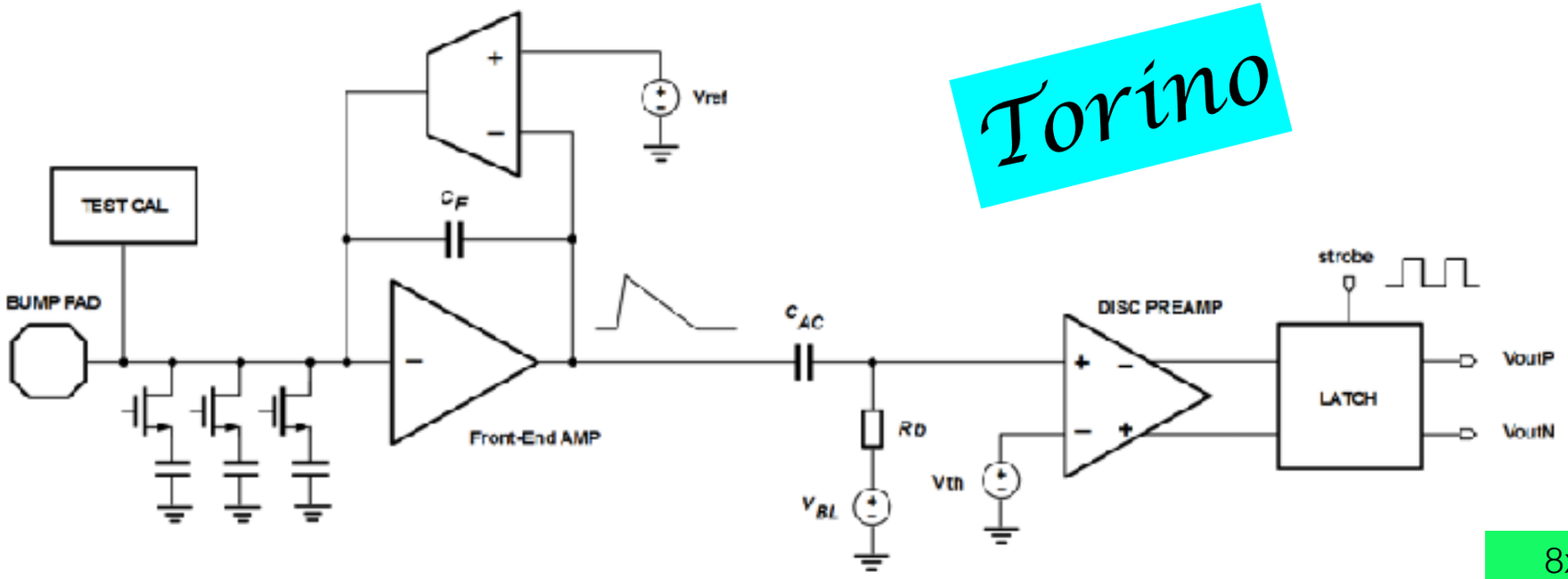
Pavia/Bg



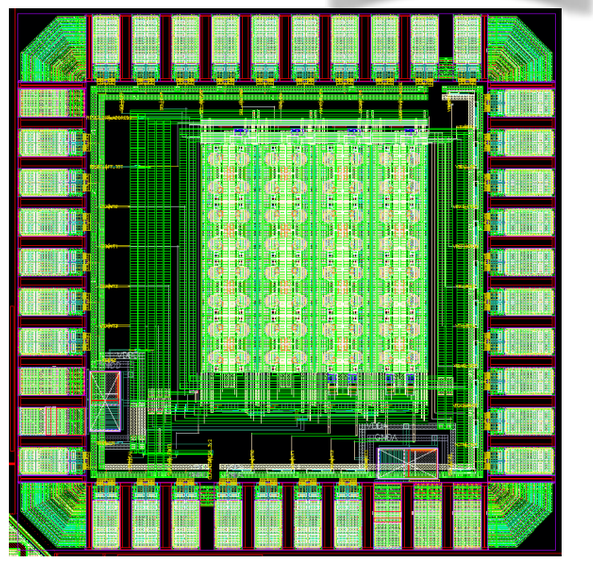
- Single ampli stage for minimum power dissipation (~5 uW)
- Krummenacher feedback to comply with the expected large increase in the detector leakage current (up to ~10 nA)
- 30000 electron maximum input charge expected, ~450 mV preampli output dynamic range
- Selectable gain, recovery current and detector emulating capacitance
- 40 MHz clock, 5 bit dual edge counter, 400 ns maximum ToT

Dual Edge counter

Synchronous Analog FE



Torino



8x8 pixel matrix submitted and tested
Analog readout of CSA and Discriminator (via buffers)

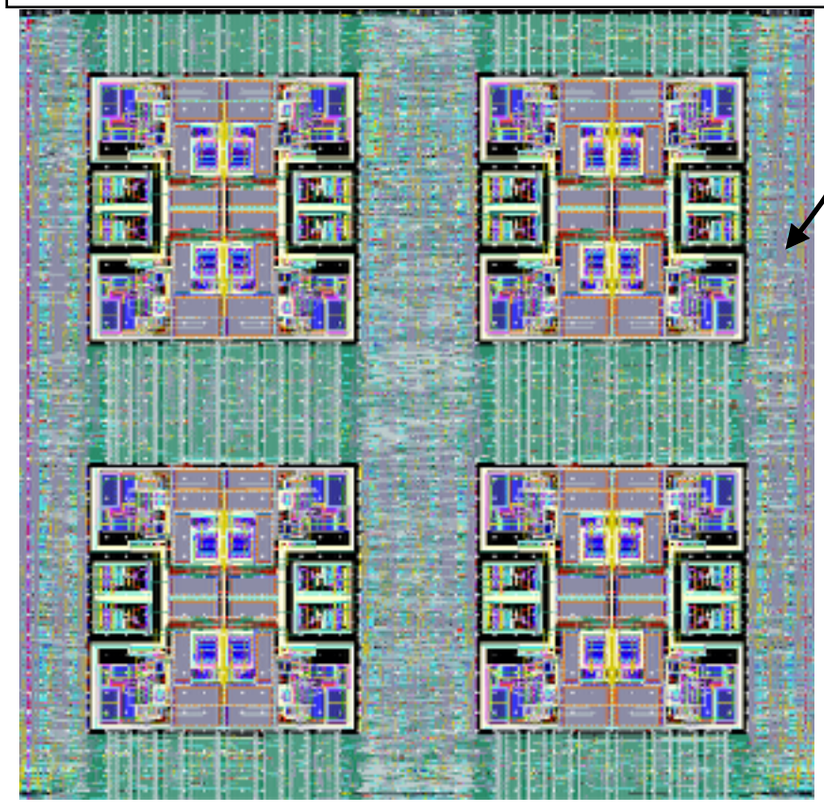
- **PREAMPLIFIER**
  - One stage CSA with Krummenacher feedback
- **Synchronous DISCRIMINATOR**
  - (AC coupled to CSA)
  - off-set compensated diff.amplif. + latch;
  - **FAST Time-over-Threshold**
    - Local oscillator strobing Latch (to 800MHz
- **Calibration circuit**
  - digital signal + DC calibration leve

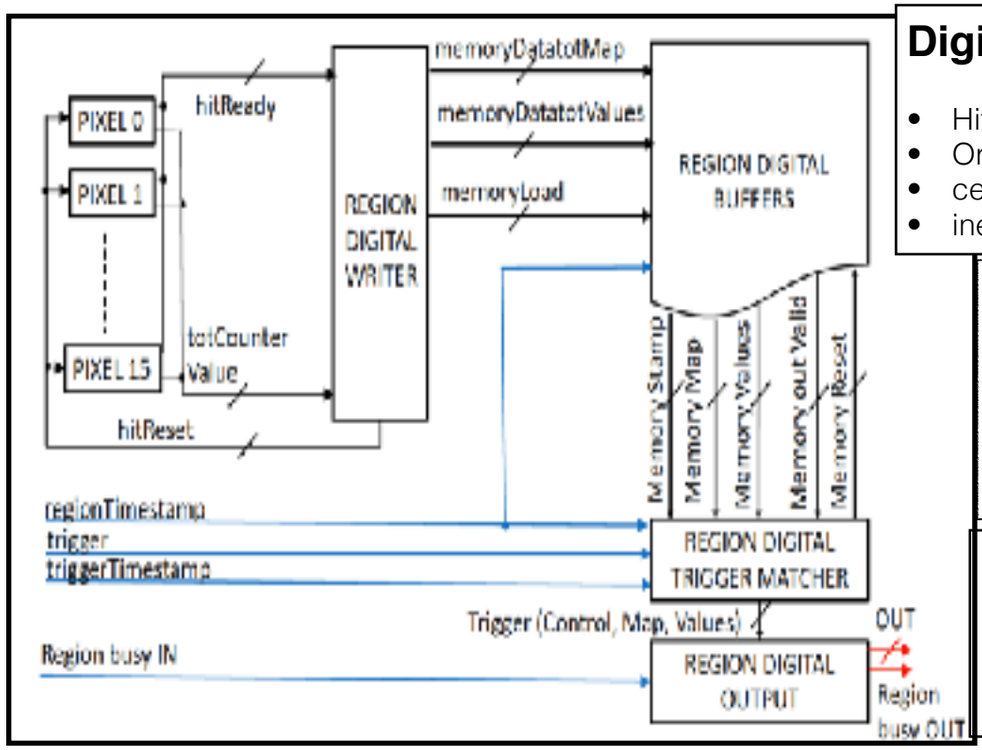
Performance SUMMARY

- Compact: < 35um x 35 um
- Low power: < 5.5 uW (with ToT logic)
- Low noise: ENC=100e @C_{det}=100 fF
- Leakage compensation: up to 50nA/pixel
- Fast Charge measurement:
  - 10 ke in : 90 / 360 ns (Fast / Slow recovery current)
  - can achieve up to 7-8bit (125-250e /ADC) - no ext clock
- NO Threshold-Trimming:
  - autozeroing made by hardware

CHIPIX65 demonstrator

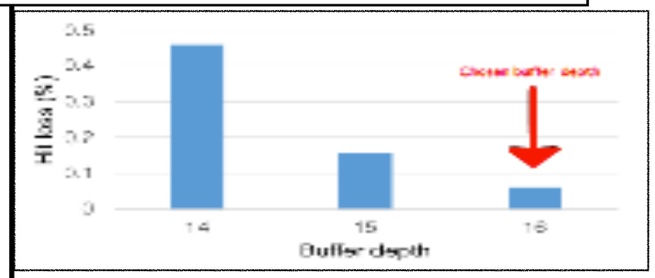
(4x4) Pixel Regions with four (2x2) analog island on digital see





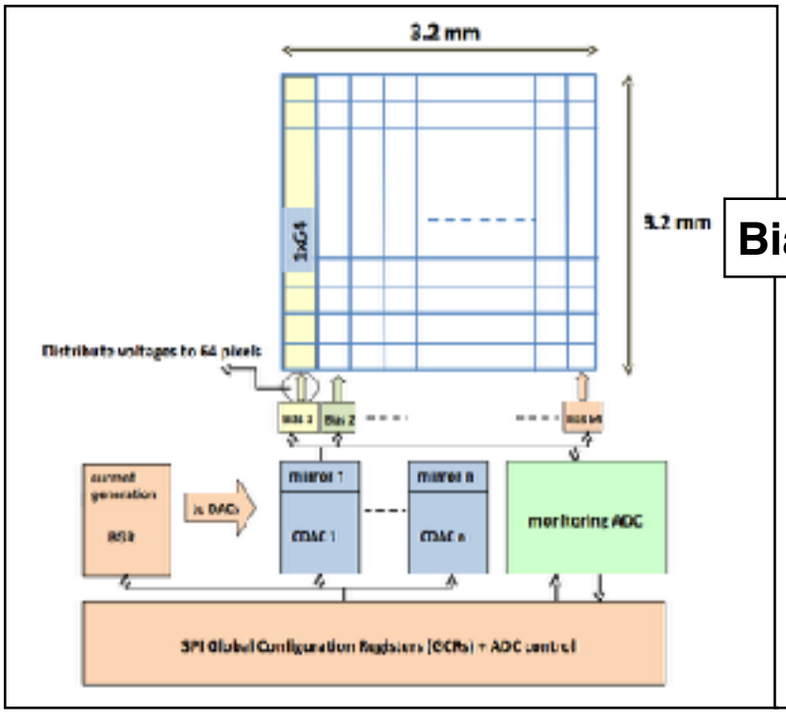
Digital architecture:

- Hit local storage + Local Trigger-Matching
- Organised into (4x4) Pixel Region
- central latency buffer
- inefficiency<0.2%



Running mode:

- Triggered / triggerless / debug
- BinaryOnly/5-bit ToT
- EOC scan-chain

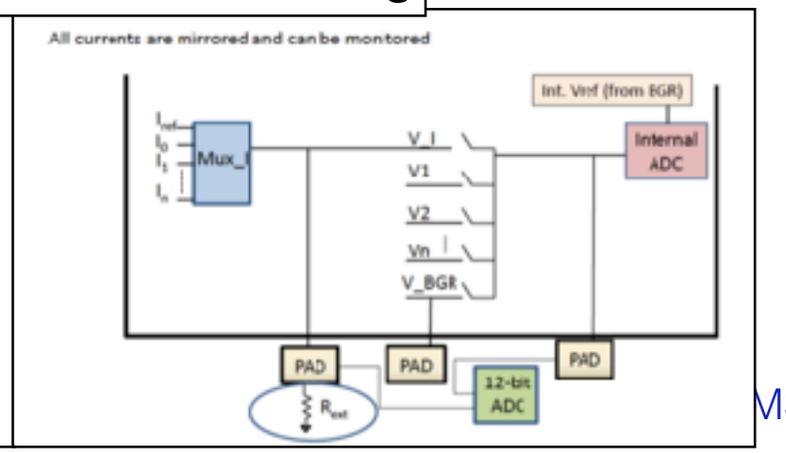


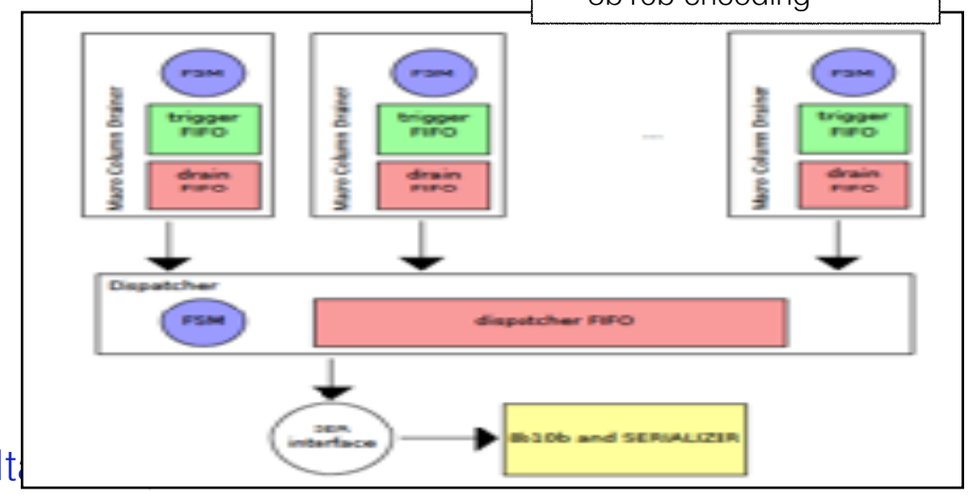
- 2 Very Front End (each 32x64 pixels)
- 16 DAC (10bit current steering), 1 BandGap, 1 monitoring ADC (12bit)
- 8 x sLVS-RX, 2 x sLVS-TX, 1 Serializer

Input / Output:

- Fully digital
- Configuration via SPI
- serial readout@320 MHz
- 8b10b encoding

Bias and monitoring





RD53: IP blocks

- List of required ~20 IP blocks: assigned to various groups
- Initial specs review done in June 2014
  - 2014: 7 first prototypes submitted
  - 2015: remaining prototypes
  - 2016: versions for RD53A
- IP-block for RD53A have to be prototyped, characterised and tested before / after irradiation up to at least 500 Mrad.

BIAS

- Band Gap : **CPPM, Pavia, CERN**
- DAC : **Bari**, Prague

In/Out

- I/O PAD : **CERN, LBNL**
- SLVDS driver : **Pavia, Pisa**
- SLVDS receiver : **Pavia,Pisa**
- PLL : Bonn
- SER : Bonn, **Pisa**
- DES : **Pisa**
- CDR : Bonn
- Cable Driver : Bonn

Power Monitor

- Monitoring ADC : **CPPM, Bari, CERN**
- Temperature Sensor: **CPPM**
- Radiation Sensor : **CPPM**
- Analog Buff RtoR : RAL

Power

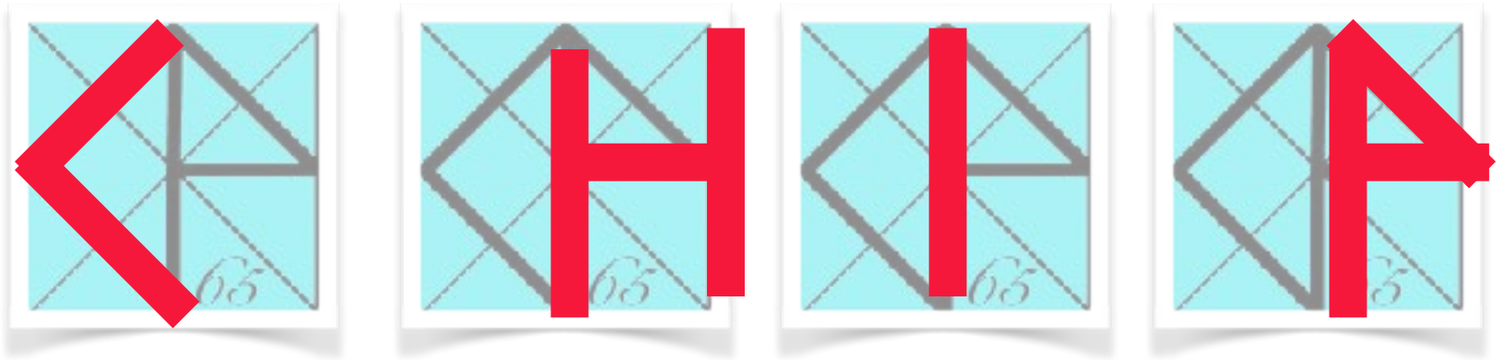
- Power-ON Reset : **Sevilla**
- Shunt LDO : Dortmund

Others

- Config. Memories : **CPPM**
- SRAM EOC : **CERN, Milano**
- Others : VCO, EFUSE, DC-DC….

IP on bold have prototypes TESTED and oK

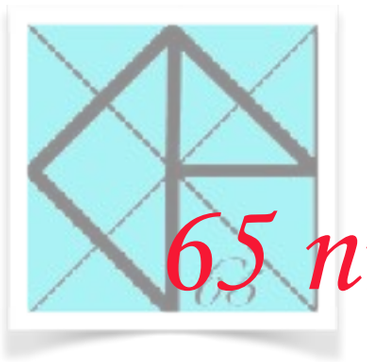
An innovative



for a

EL detector

using a CMOS



65 nm technology