3D Integration Technology using Through Silicon Vias for Hybrid Pixel Detector Modules

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MOTIVATION

Hybrid pixel detector modules are the main building blocks of silicon particle tracking detectors in high energy physics experiments as well as in x-ray cameras for research and development using synchrotron radiation. Wire bonding is used so far to connect the readout ICs to the detector services. The 3D integration technology with through-silicon-vias (TSVs) offers several advantages in terms of reduction of peripheral area of hybrid modules as well as reduction of signal path length for fast signal readout.
The TSV process has been demonstrated on two different types of readout chips: the ATLAS FE-I4B and the MEDIPIX3RX chip. In case of the ATLAS FE-I4B readout chip the goal is to achieve a very compact hybrid module design with a minimum of material budget for the innermost layers of HEP pixel tracking detectors. Using TSVs for MEDIPIX3 hybrid x-ray camera modules we can achieve a four side stitchable hybrid module for a scalable increase of sensitive detector area with a minimum of insensitive space between two adjacent modules.

TSV FORMATION PROCESS (Via last-, Via backside process)

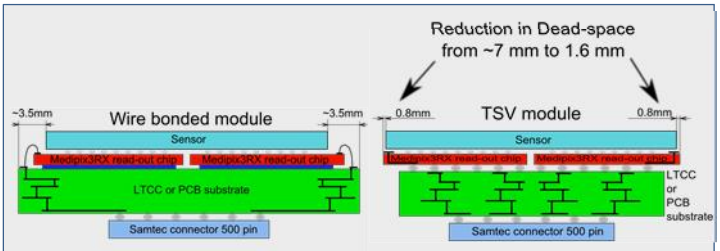
- ASIC wafer front side: UBM formation process
- Temporary carrier wafer bonding (glue bonding)
- Backside thinning (grinding, wet etching, CMP, DRIE etching)
- TSV silicon etching (DRIE BOSCH Process)
- TSV-insulation (TEOS, PE-CVD, SA-CVD, Polymer)
- Adhesion/barrier- + seed-layer (Ti (TiW, TiN, Ta(N)) / Cu HI-PVD)
- Via filling (ECD Cu bottom up filling, MO-CVD W)
- Backside passivation (CVD oxide/nitride, polymer)
- Backside contact formation (Cu RDL, Al RDL, UBM)
- Carrier wafer debonding + front side cleaning
- Dicing

The TSV process was demonstrated on two different types of readout chips: the ATLAS FE-I4B and the MEDIPIX3RX chip. Both types are already prepared for this TSV backside process in terms of the design of the TSV landing pad as part of the internal M1 IC layer. The TSV metallization will be connected to this internal IC pad. Therefore the TSV formation process has to be adapted to the internal layer structure of the readout chip. A Cu liner filling process is used for TSV metallization and interconnection to the TSV landing pad. This process step is also used to form the RDL on the backside of the ROC chip. Finally a polymer passivation and a solderable UBM metallization is deposited onto readout chip backside.

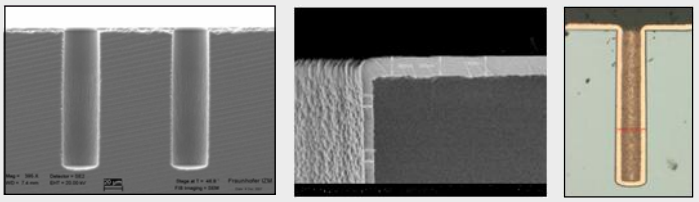
RESULTS

The first batches of ATLAS FE-I4B ROC wafer and MEDIPIX3 ROC wafer have been processed. Functional tests have been performed at DESY Hamburg and are currently under test at Bonn University. In case of the MEDIPIX ROC a special TSV landing pad design with „perforations“ was observed which may result in shorts between TSV and M2 layer of the IC. As a conclusion a second batch was started with re-designed TSV dimensions and optimized process parameters to avoid this issue.
Beside the functional tests reliability investigations were performed at Fraunhofer IZM. A MEDIPIX ROC with TSVs was stressed from room temperature to reflow temperature at 260°C for three times. No changes could be observed by microscopy and at cross sections. In addition to this test ROCs were stressed in a thermal cycling test between -55°C and 125°C. No delamination of layers could be observed up to 300 cycles. After that number of cycles delamination were observed outside the TSV interconnection area only between polymeric dielectric layer and oxide passivation or metal layer. The adhesion will be optimized in further batches.

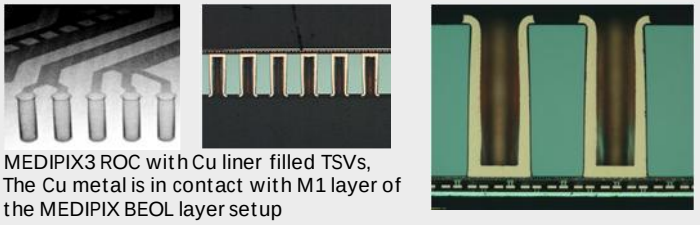
After test of the electrical functionality the ROCs will be flip chip assembled to sensor tiles and finally bonded onto LTCC or PCB.



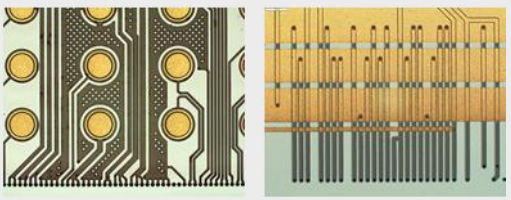
Schematically setup of a hybrid pixel module
(interconnection with wire bonding left, with TSV right)



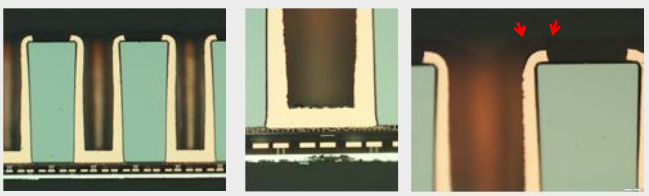
Main steps of TSV formation process:
from left: TSV silicon DRIE, oxide passivation, Cu liner filling



MEDIPIX3 ROC with Cu liner filled TSVs,
The Cu metal is in contact with M1 layer of the MEDIPIX BEOL layer setup



Backside RDL for 2nd level Assembly to LTCC or PCB
Left: MEDIPIX ROC with pads for solder ball bumping
Right: ATLAS ROC with bus structure pads for wire bonding



TSV after 3x reflow
No degradation observed

TSV after 1000 T-cycles (-55°C / 125°C)
- No degradation observed at via bottom
- Cracks and delamination observed in dielectric polymer layer

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