Development of a Detector Control System for the ATLAS Pixel detector in the HL-LHC

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ATLAS

BERGISCHE UNIVERSITÄT WUPPERTAL

Niklaus Lehmann[1], Michael Karagounis[2], Susanne Kersten[1], Christian Zeitnitz[1]

[1]University of Wuppertal, [2]FH Dortmund

Detector Control System (DCS)

The increased number of modules in the inner tracker (ITk) Pixel detector at the High-Luminosity LHC (HL-LHC) requires a new powering scheme. A serial powering was chosen as a baseline. We are working on the development of a new DCS to operate with serial power. It foresees three independent paths:

   **1. Safety path**   **2. Control path**   **3. Diagnostics path**

Each of these paths has its own services and can act independently of the others. They are ordered with respect to the reliability and availability with the safety path having the highest reliability.

Serial power chain

A constant current I_{SP} is flowing trough all modules in series. The local voltages are generated with shunt regulators.

This power scheme reduces the number of required power lines. In comparison with a parallel powering, the serial power has a smaller current and therefore less loss in the lines. On the other side, risks are that the chain could be broken by a failure of a single module what affects the operation of the whole chain.

The DCS has to take into account the risks of the serial power chain and work within its environment. The challenge is to operate independently from the serial current used for the modules. A dedicated ASIC is in development for this reason. The DCS chip can monitor and control individual modules in the serial power chain while being powered from an independent source.
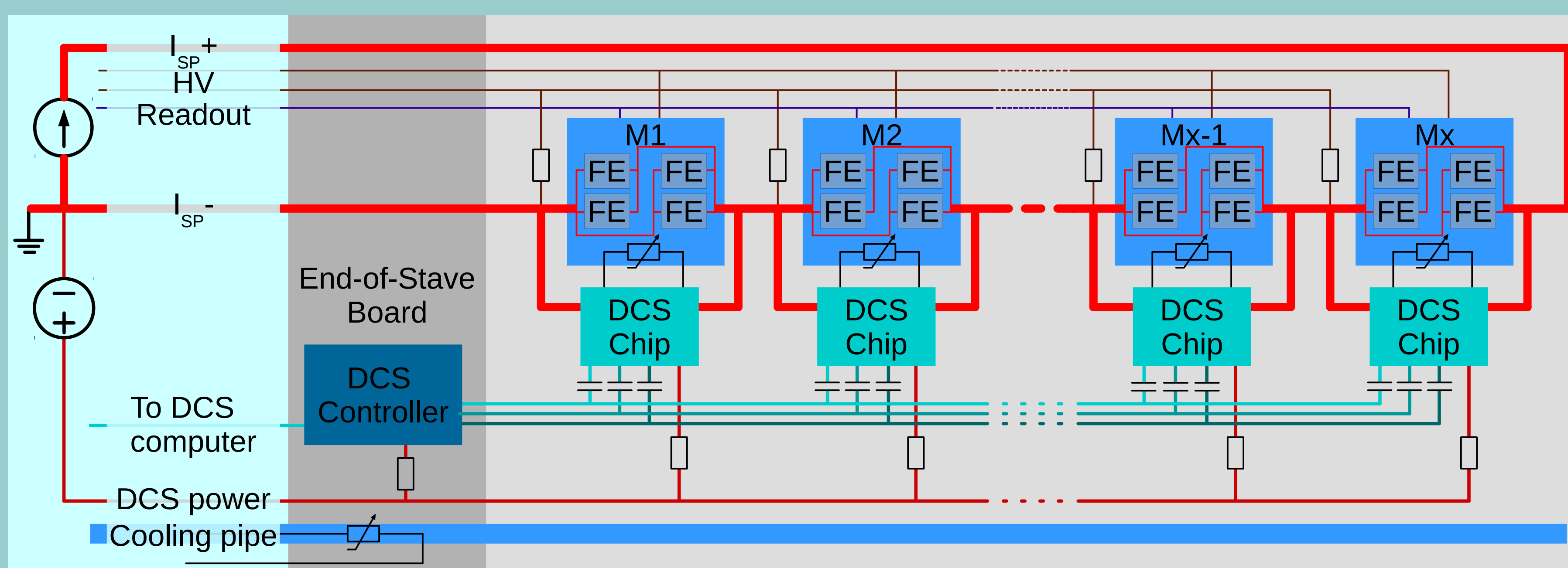
- Quad modules have four Front End (FE) chips in parallel (only two FEs for the innermost layer)
- One DCS chip per module
- Independent power line for DCS chip, return is merged with I_{SP}

Safety path

The safety path is a hardwired interlock system that directly reacts on the power supplies. It acts between devices to protect (sensors, front-end (FE) chips) and units which could cause risk (power supplies).
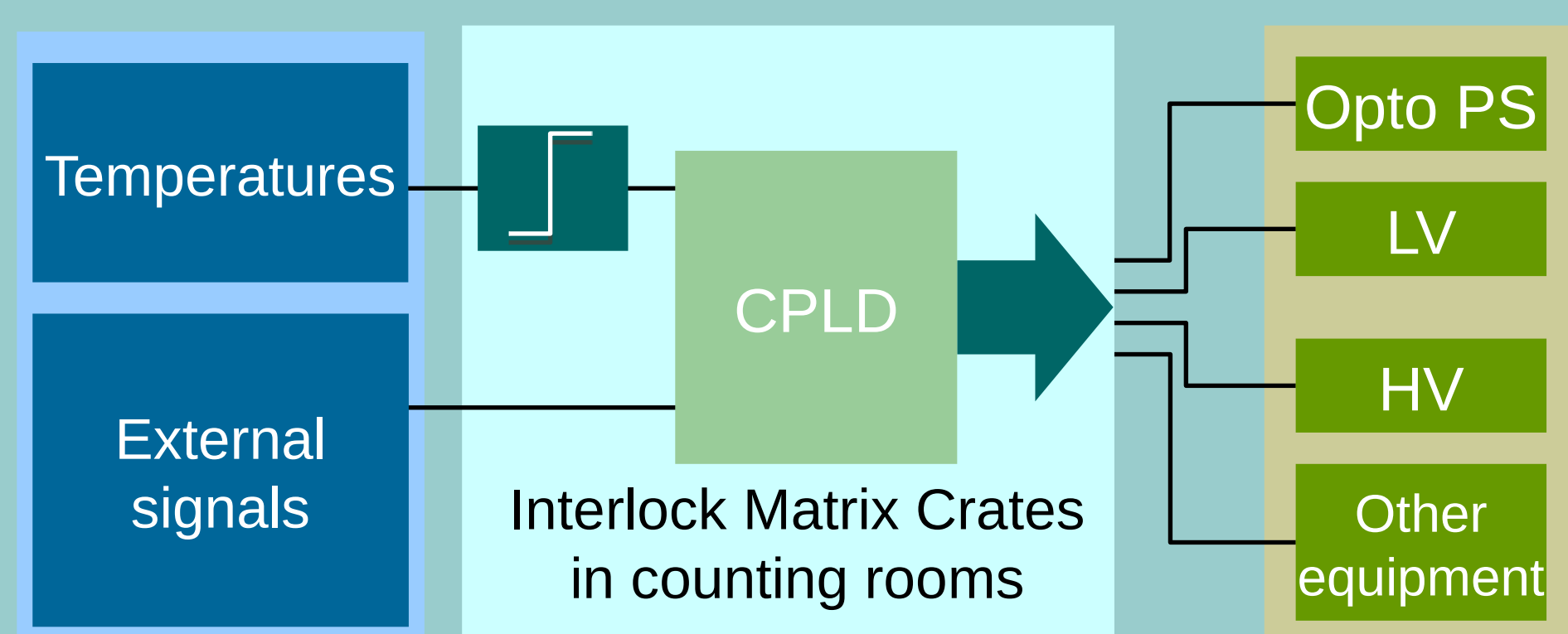
- Completely independent operation
- Permanently running
- Very robust – last line of defense
- Completely hardwired
  - No loading of parameters after start-up
  - No configuration via software
- Input from environmental sensors

Control path

The control path has an independent communication network to collect information about the detector and control the power to individual modules. This information contains the temperature of each module together with voltages. This allows to monitor the status of the detector at a module level even if the readout system is off.
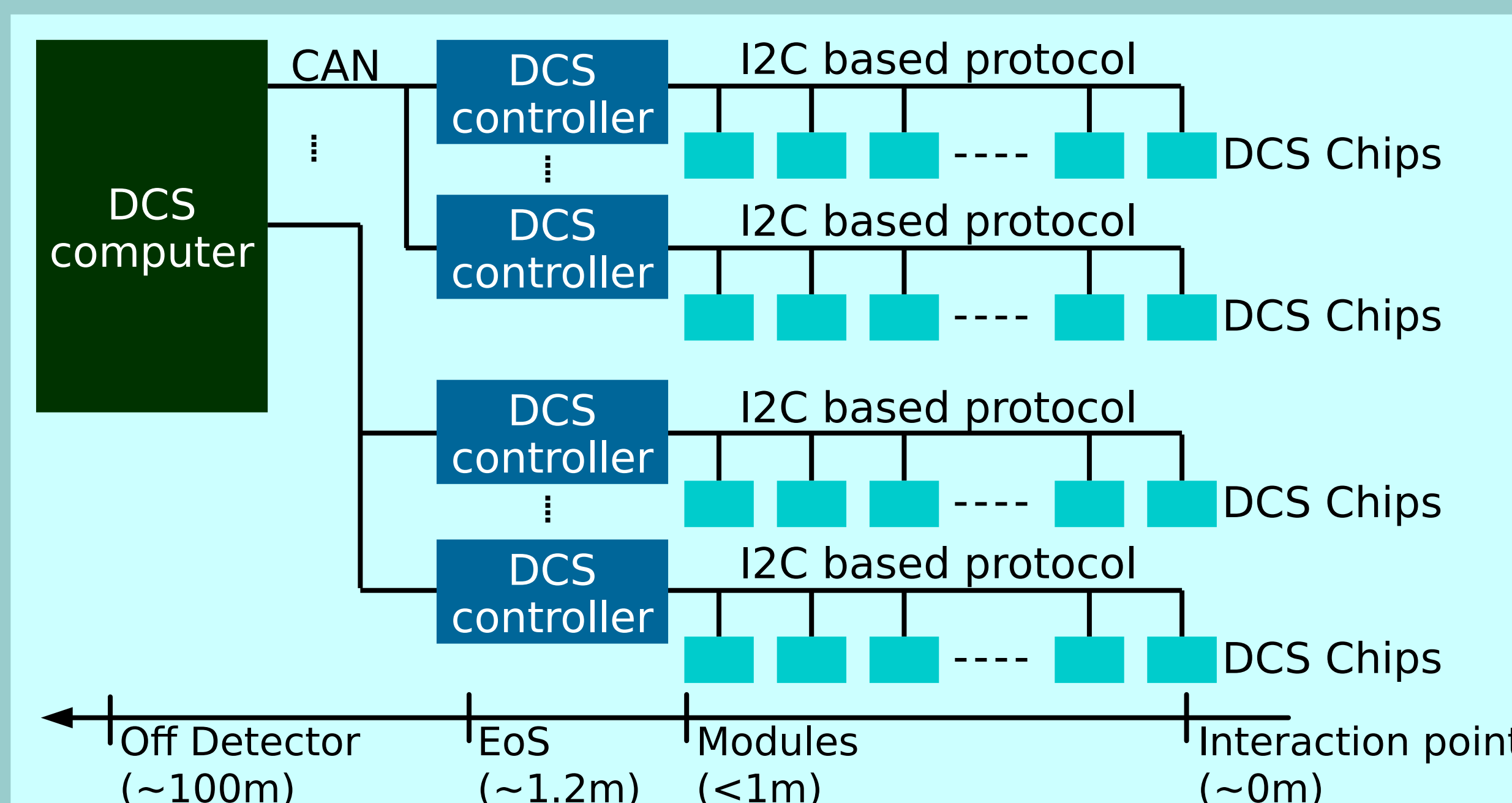
- DCS computer in counting room
- CAN based protocol to DCS controller
  - 100m cable length possible
  - 16/32 nodes on one line
- I2C based protocol to DCS chip
  - 8 nodes per chain
  - 3 single ended lines
- DCS chip with bypass to switch off modules

Diagnostics path

The third intended path for the DCS system has the highest granularity with FE level. The data readout will be used to transmit status information about the FE chips. This can include internal voltages and temperature information for redundancy.
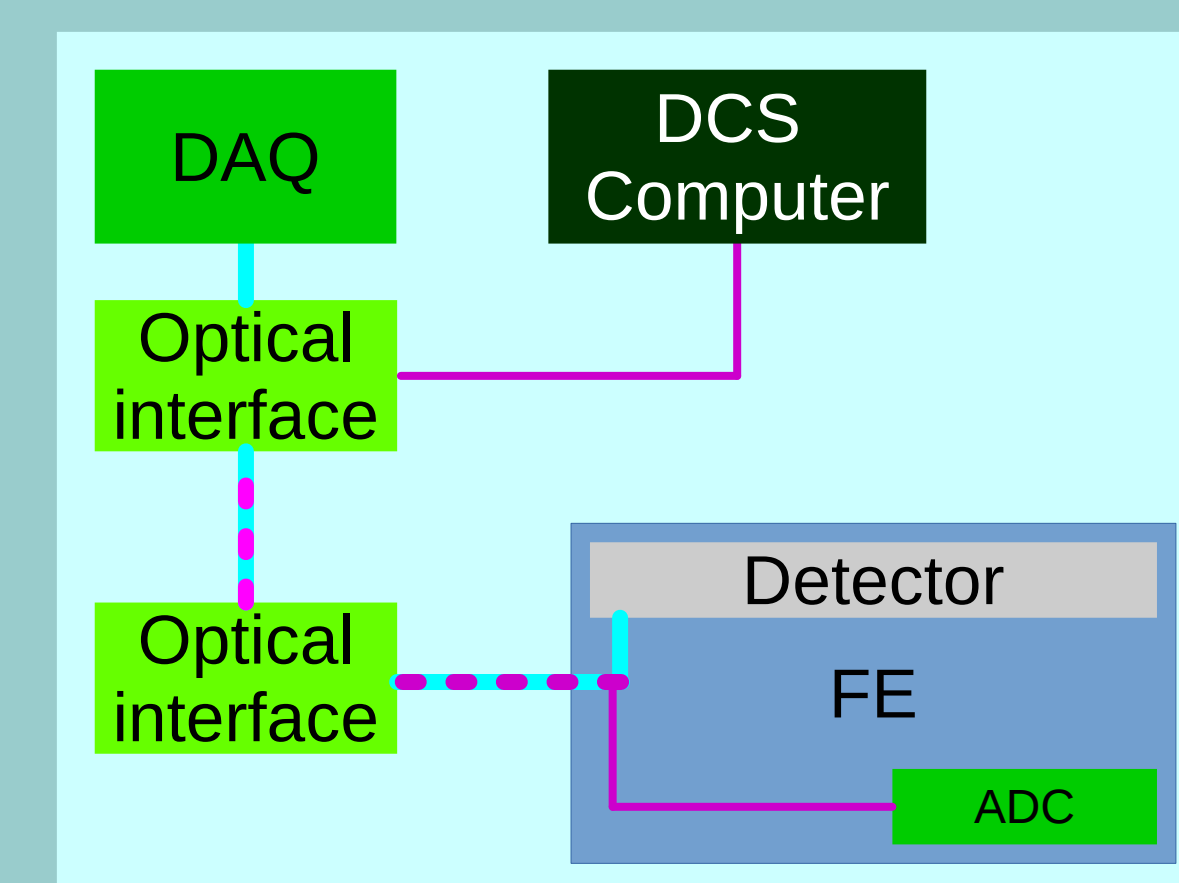

- FE sends DCS information on same medium as regular data
- Use of optical path
- DCS information and tracking data split after optical transmission

DCS chip: Pixel Serial Power & Protection (PSPP)

A new chip to monitor and control the serial power chain is in development. Two iterations of a prototype were already developed and fabricated. These prototypes (PSPPv1 and PSPPv2) demonstrated a proof of concept and allow first test in a serial power chain. A new version is in development, which addresses the adjusted requirements and improves the stability of the system.

Key features:

- Bypass transistor to switch off individual modules
- Internal voltage regulator to operate along serial powered modules
- Serial protocol for communication based on I2C
- AC coupled single ended lines
- Monitoring capabilities to measure temperature and voltages
- Module interlock to automatically react in case of over-voltage or over-heating
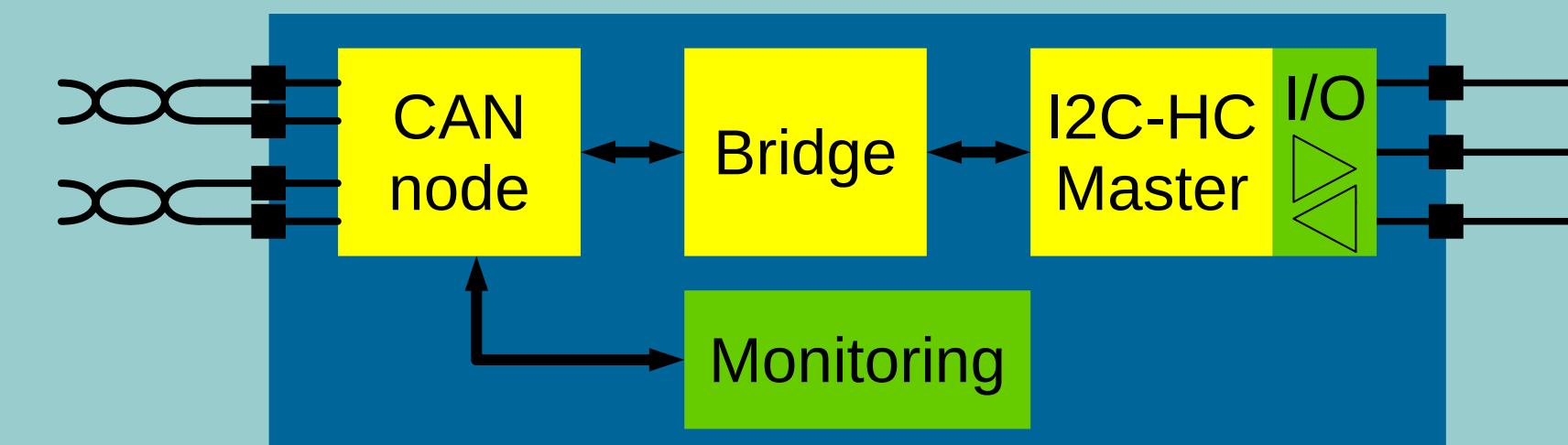- Interlock inactive in case of no-signal
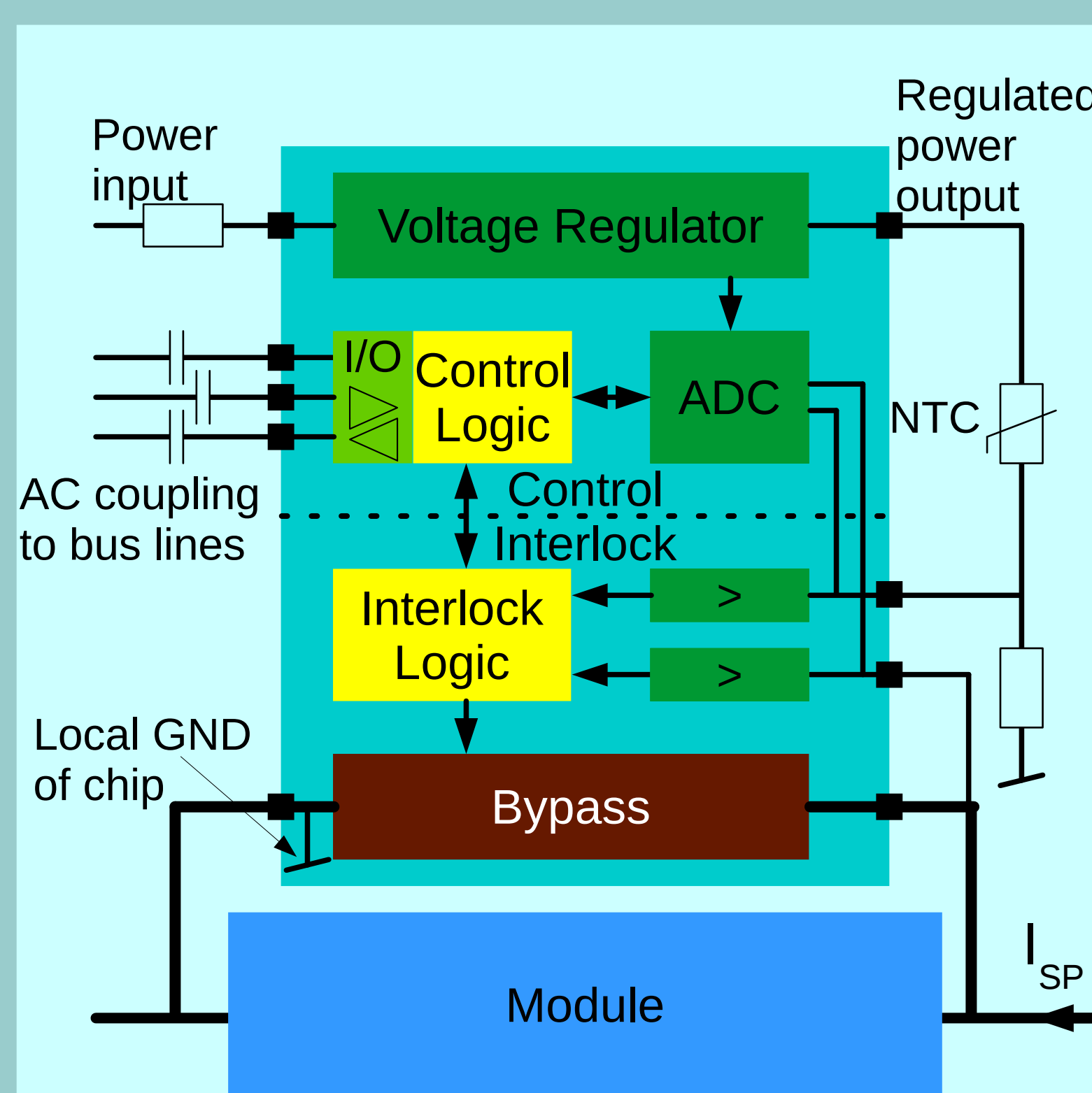
PSPPv2

Concept for PSPPv3

DCS controller

A second chip serves as a bridge between a long range protocol (CAN) and the short range protocol used to communicate with the DCS Chip.

The exact location of the controller is still open and multiple concepts exist.

I2C-HC: I2C with hamming code extension

- 8 data bits plus 4 cyclic hamming code bits to detect errors
- New physical layer
  - Use of manchester encoded signals to have DC balanced lines
  - Three lines
    - SCLx2: constant clock at twice the communication speed
    - SDAm: Commands from master to slaves
    - SDAs: Respond from slaves