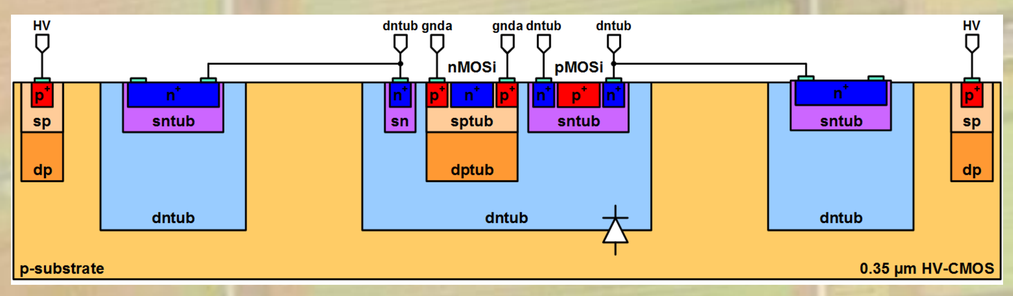
First results on the ATLAS HL-LHC H35DEMO pixel prototype

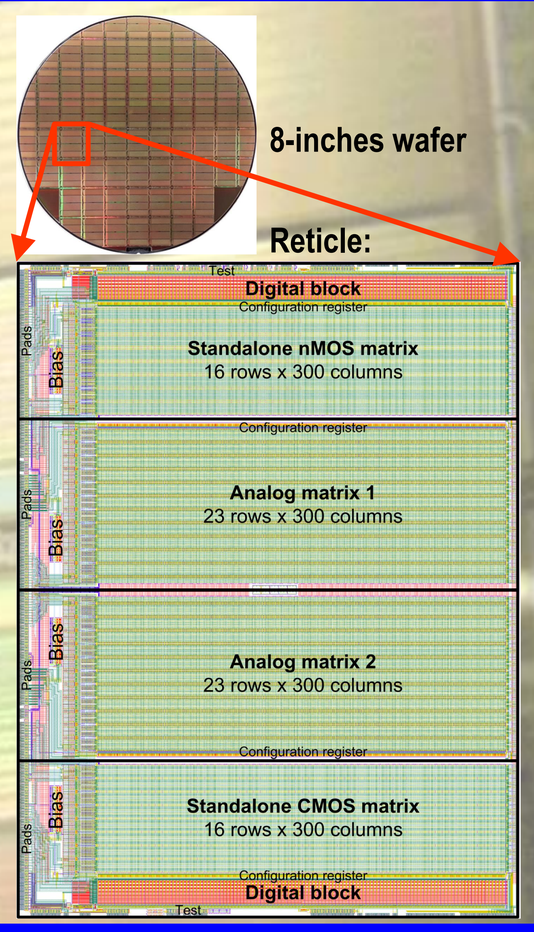
E. Vilella[(a)], R. Casanova[(b)], G. Casse[(a)], I. Peric[(c)], S. Powell[(a)], J. Vossebeld[(a)], S. Wonsak[(a)]

[(a)] University of Liverpool, Department of Physics, Oliver Lodge Building, Oxford Street, Liverpool L69 7ZE, United Kingdom
[(b)] Institut de Física d'Altes Energies (IFAE), The Barcelona Institute of Science and Technology, Edifici C7, Universitat Autònoma de Barcelona (UAB), E-08193 Bellaterra, Spain
[(c)] Karlsruher Institut für Technologie (KIT), Campus Nord, Hermann-von-Helmholtz-Platz 1, D-76344 Eggenstein Leopolshafen, Germany

Background

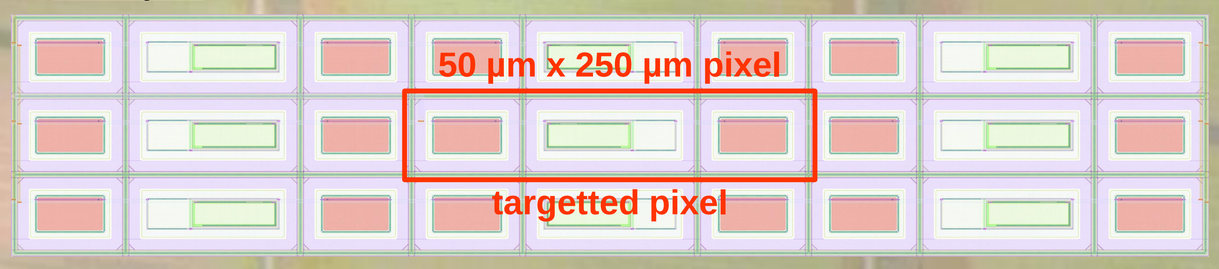
- The H35DEMO is an HV-CMOS pixel prototype aimed at proving that this sensing technology can be qualified as a tracker detector for harsh working environments such as the HL-LHC
- It is in the 0.35 µm HV-CMOS process from ams
- It was fabricated through an engineering run (substrate resistivities are 20 Ω·cm, 80 Ω·cm, 200 Ω·cm and 1 kΩ·cm)
- Reticle with large area of 18.49 mm x 24.40 mm
- The prototype includes:
  - 2 analogue matrices read out via FE-I4 (1 matrix with nMOS input preamplifier and 1 matrix with pMOS input preamplifier)
  - 2 fully monolithic matrices (1 matrix with in-pixel nMOS comparator and 1 matrix with off-pixel CMOS comparator)
  - test structures for sensor characterization
- The pixel size is 50 µm x 250 µm
- Pixel cross-section:



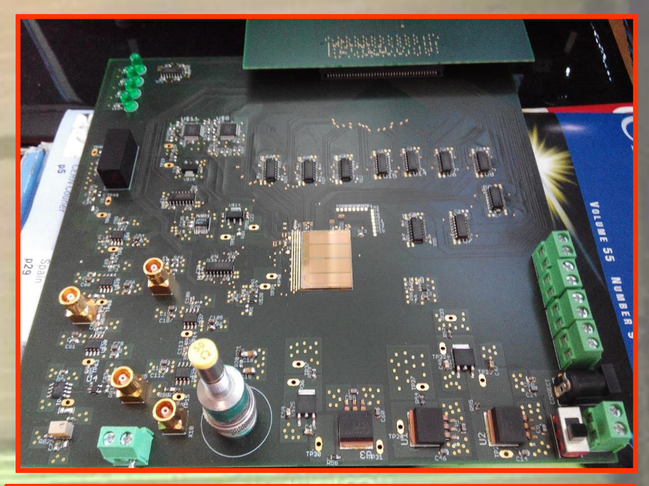


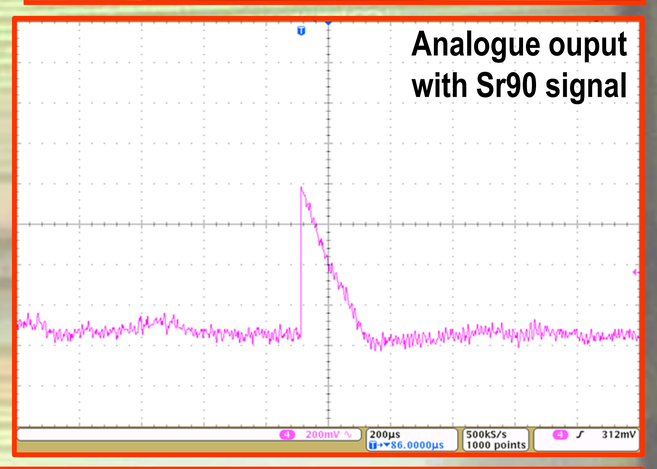
Measurements

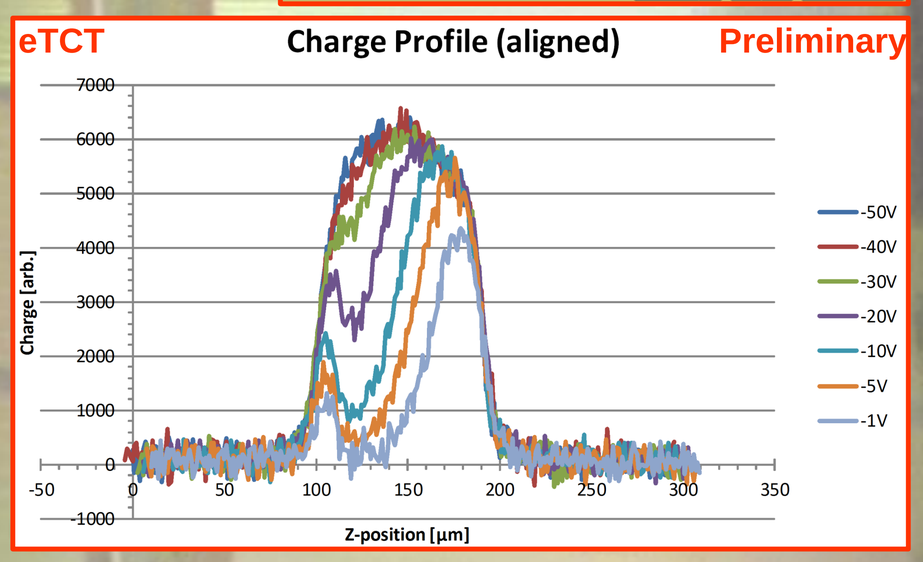
- Matrices:
  - The set-up is based on a custom pcb designed by *Uni. Liverpool* and an FGPA development board from *Xilinx* (ZC706)
  - Pcb details:
    - To measure the nMOS fully monolithic matrix using the on-chip digital readout electronics
    - All the connections between the ASIC and the peripheral pads are made by wire-bonding
    - LVDS links to the FPGA development board are through an FMC connector
  - Future plans include the design of pcbs to measure the other 3 matrices
- Test structures:
  - The set-up is based on a TCT/eTCT system and a user interface from *particulars* (scripts from *DESY*). With this system, a pulsed laser illuminates the DUT and e^--h^+ pairs that induce signal are created inside the targetted detector area. It is possible to map the collected charge as a function of the position where the charge was generated. With eTCT, it is possible to get the electric field map inside the bulk.
  - The set-up also includes a custom pcb designed by *Uni. Liverpool* + back side processed ASIC to improve charge collection
  - Back side processing of a 1 kΩ·cm wafer at *Ion Beam Services* consists of:
    - Thinning to 100 µm, back side p^+ implantation (Boron), thermal annealing and back side metallization
  - The DUT is a 3 x 3 matrix of 50 µm x 250 µm pixels without electronics. The central pixel can be read out individually.
  - TCT/eTCT system details:
    - Picosecond pulsed laser (350 - 400 ps) with a pulse rate of 1 kHz
    - Wavelength of 1064 nm
    - Beam size and focusing position calculated using the knife-edge technique
    - Laser scan with 1 µm steps
  - At -40 V of bias voltage, the sensor is fully depleted
  - DUT layout:



- Measurements are on-going







Conclusion

- Custom pcbs have been designed to measure the different circuits in the H35DEMO prototype
- First results show that the prototype is working well
- eTCT results show a fully depleted sensor at -40 V

References:

[(1)] I. Peric, A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology, *Nucl. Instrum. Meth.* A 582 (2007) 876.
[(2)] E. Vilella et al., Prototyping of an HV-CMOS demonstrator for the High Luminosity-LHC upgrade, J. Instrum. 11 (2016) C01012.

Contact → vilella@hep.ph.liv.ac.uk (E. Vilella)