HV-CMOS Detectors in BCD8 Technology

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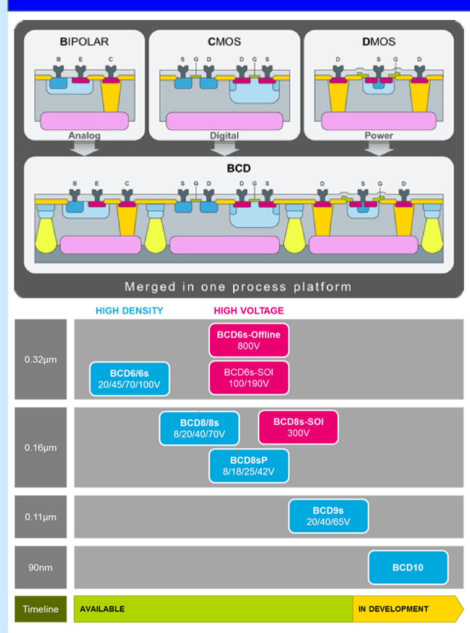
Introduction

This work describes the first pixel detectors realized with the BCD8 technology by STMicroelectronics. The BCD8 is a 160 nm process integrating bipolar, CMOS and DMOS devices and it is mostly used for automotive application. A version with 70 V voltage capability has been tested to evaluate its suitability for the realization of CMOS sensors with a depleted region of several tens of micrometer. Sensors featuring 250X50 µm² pixels on a 125 Ωcm resistivity substrate have been characterized. The characterization shows a uniform breakdown at 70 V before irradiation and a capacitance of ~ 80 fF at 50 V reverse bias voltage. The response to ionizing radiation is tested using radioactive sources and an X-ray tune, reading out the detector with an external spectroscopy chain.

BCD8 Technology



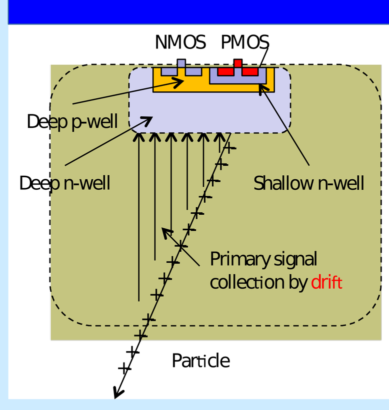
- Availability of different devices integrated in the same process
- **Epitaxial process**: can easily grow on different substrates.
- Possible to reach thick depletion layers: 30 µm looks an optimal compromise between signal and material thickness of the detector
- **Long-term availability**: one of the major production lines for ST automotive products.

References:

D. Riccardi et al., DOI: 10.1109/ISPSD.2007.4294935

R. Roggero et al., DOI: 10.1109/ISPSD.2013.6694422

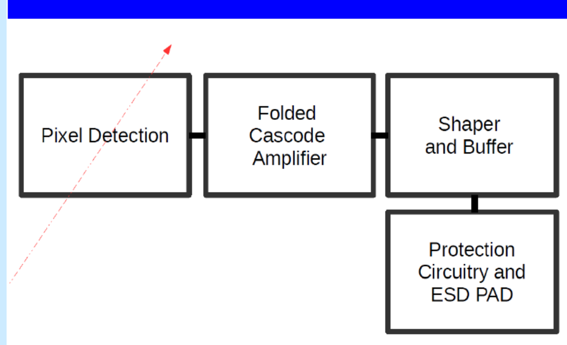
CMOS Image Sensor



CMOS sensor with depletion layer:

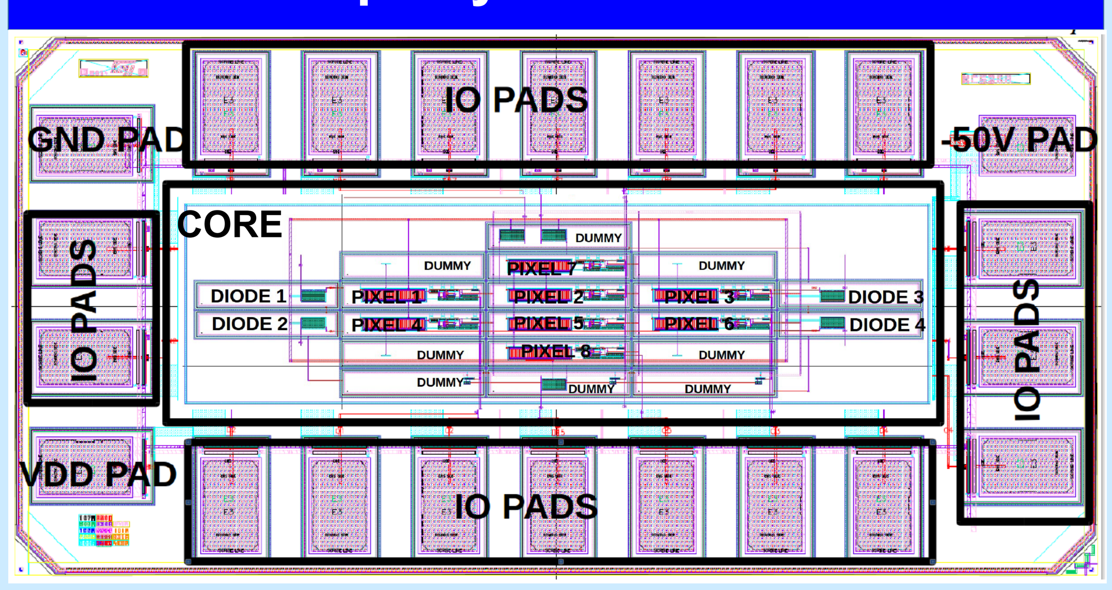
High-Voltage:
- For depletion
- High-Resistivity Substrate
- Designed with 100% fill factor

Top Level Block-diagram: KC53AA

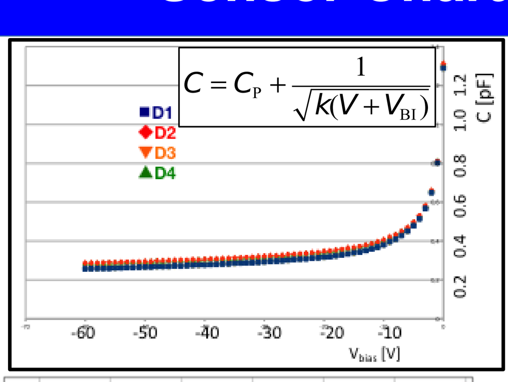


- First version of the prototype
- An array of **8 pixels and 4 passive diodes**
- Pixel area: **250X50 µm²**
- Current Injection circuitry

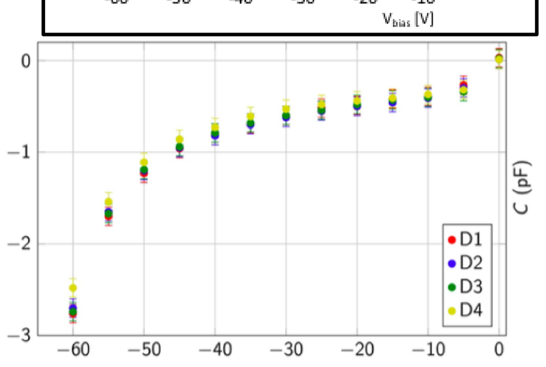
Chip Layout: KC53AA

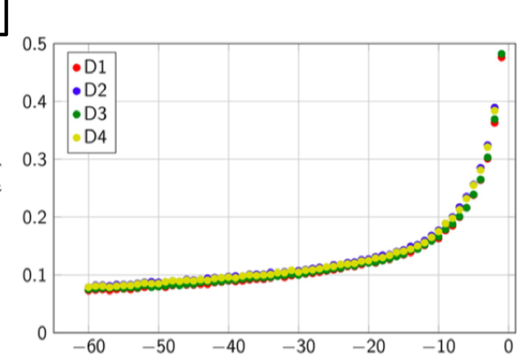


Sensor Characterization

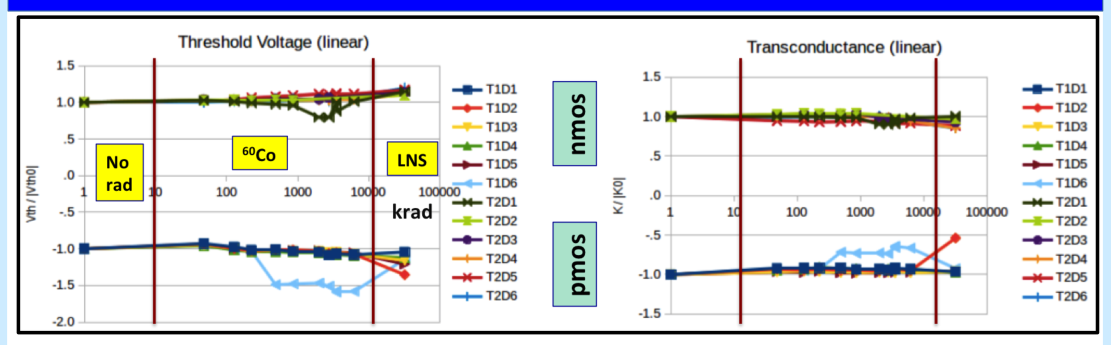


- Leakage current: **0.8-1.4 pA/pixel**
- Pixel capacitance: **80-90 fF at 50 V**





Radiation Hardness



Requirements for HL-HLC applications:

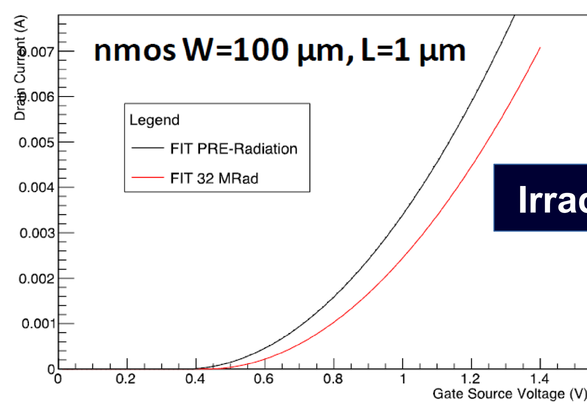
0.1-1 Grad dose, $10^{15\text{-}16}$ n_{eq}/cm² NIEL (depending on detector radius)

Irradiation tests:

- ^{60}Co γ and 62 MeV p
- Small variation of transistor thresholds and trans-conductance

– width: 10 — 100 µm

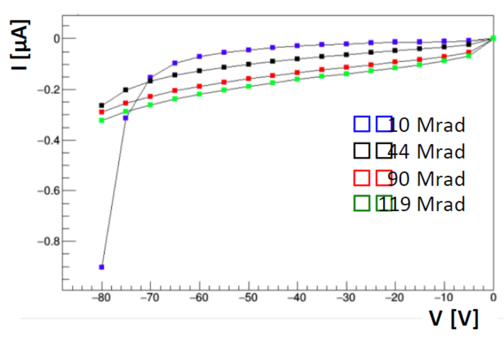
– length: 10 — 1 µm

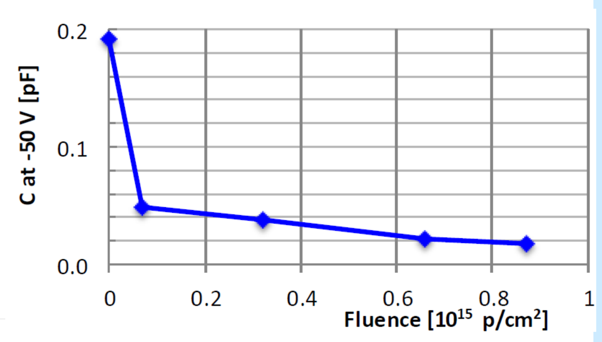


Irradiation on Transistor Arrays

$$I_D = \begin{cases} I_0 & V_{GS} < V_{th} \\ I_0 + K(V_{GS} - V_{th})^2 & V_{GS} > V_{th} \end{cases}$$

Irradiation of Sensor Diodes



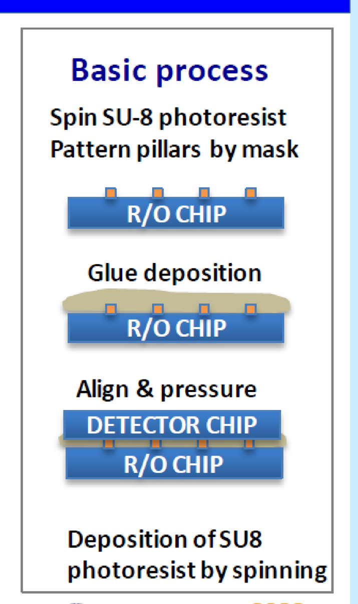


- 62 MeV p at LNS (Catania)
- Dose and NIEL compatible with requirements for operation at the HL-LHC (in the external pixel layers)
- Increase of breakdown voltage
- Reduction of junction capacitance(acceptors removal)
- Sensitive volume increases with irradiaton

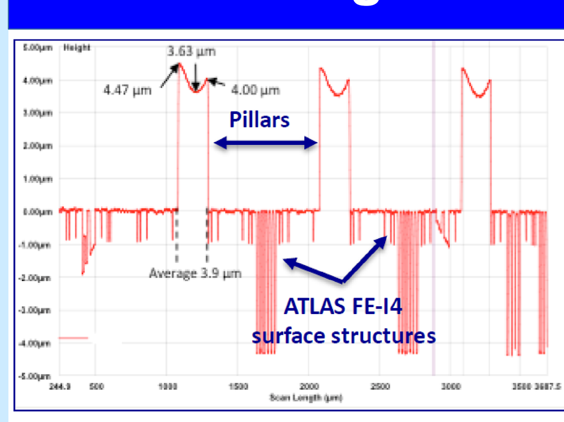
Procedure: Controlled Glue Thickness

Capacitively Coupled Pixel Detector

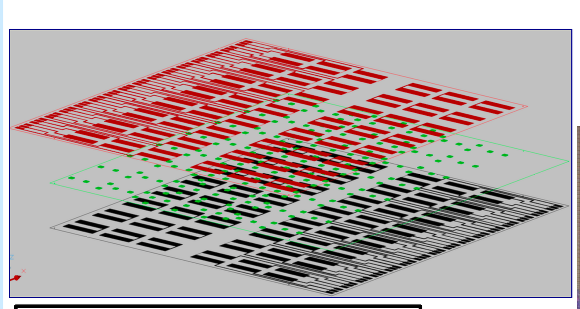
- **Pixel sensor** with integrated amplifier chain
- High-speed readout via a **r/o chip** capacitively coupled to the sensor (example: FE-I4 ATLAS chip)
- Capacitance con-trolled by SU8 spacers
- Planarity better than 1.5 µm peak-to-peak
- (5 mm size ATLAS CMOS pixel collaboration prototype)



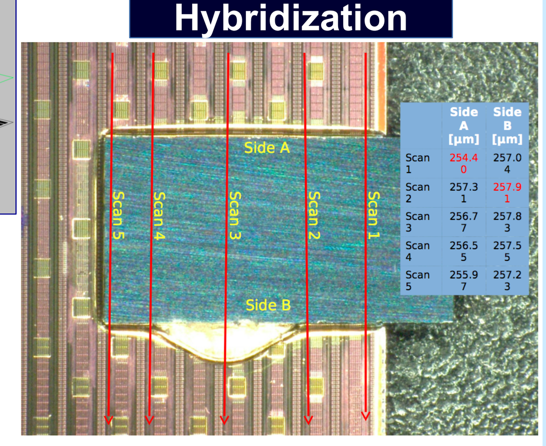
Engineering Process

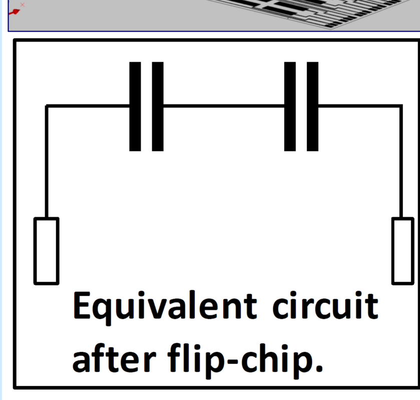


- Verified on single chips
- 6" wafer produced at FBK
- Capacitor arrays to measure uniformity
- On 2X2 cm² arrays



Hybridization

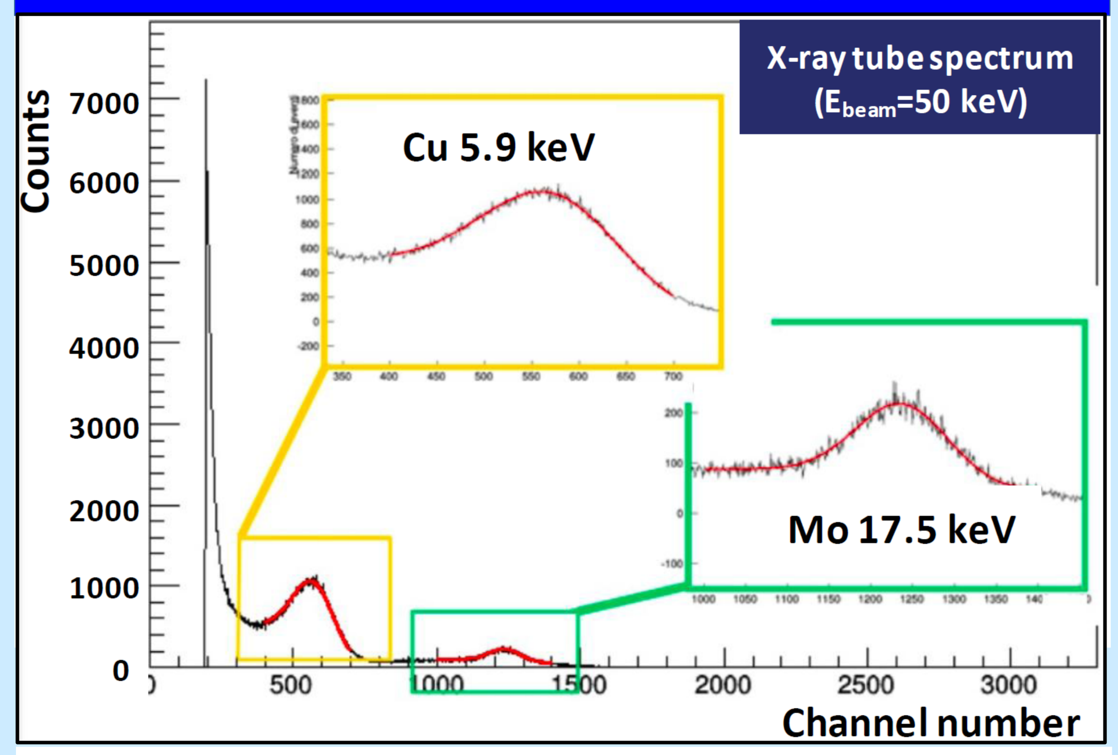




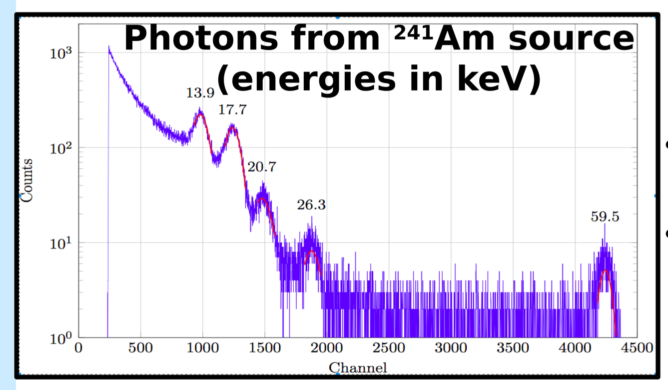
Equivalent Capacitive Model

Wafers:
- 6" CW silicon + 1 µm Oxide + 1.2 Al 1%Si (no passivation)
- Different layouts: 24-32 capacitors (3-7 pF)

Chip Characterization: Reponse to X and γ rays



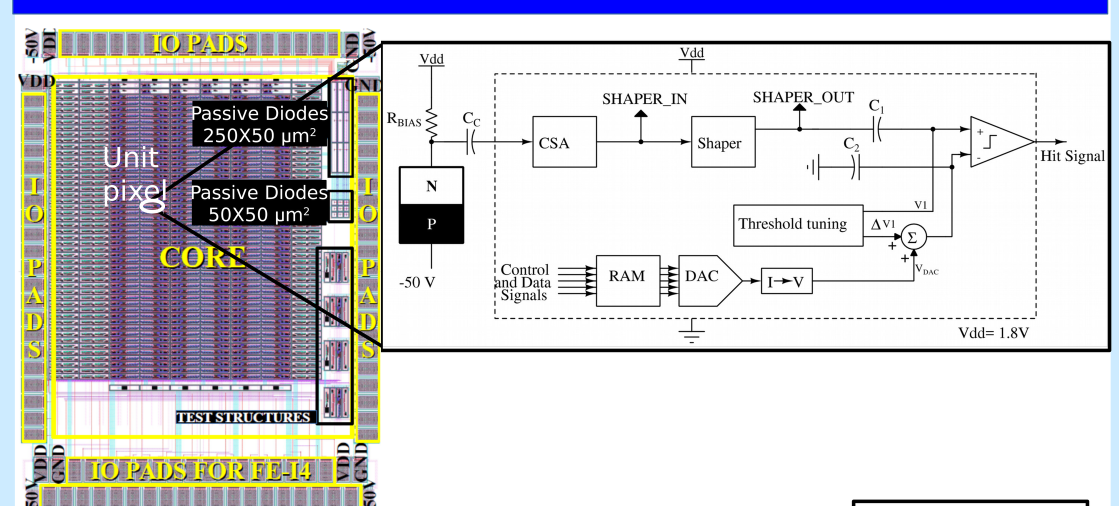
- External spectroscopic chain
- Resolution 1.0±0.2 keV
- ENC = 290±50 e

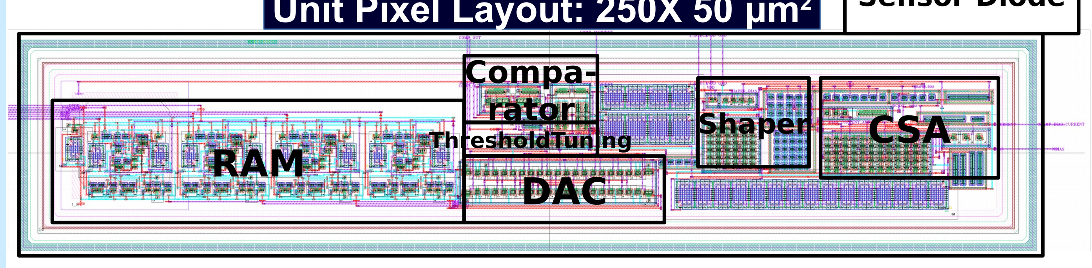


Performance of
- **250X50 µm²** pixel
- **125 Ω·cm** resistivity substrate
- Readout by external spectroscopy chain

Recently submitted 2nd test chip with integrated amplifier

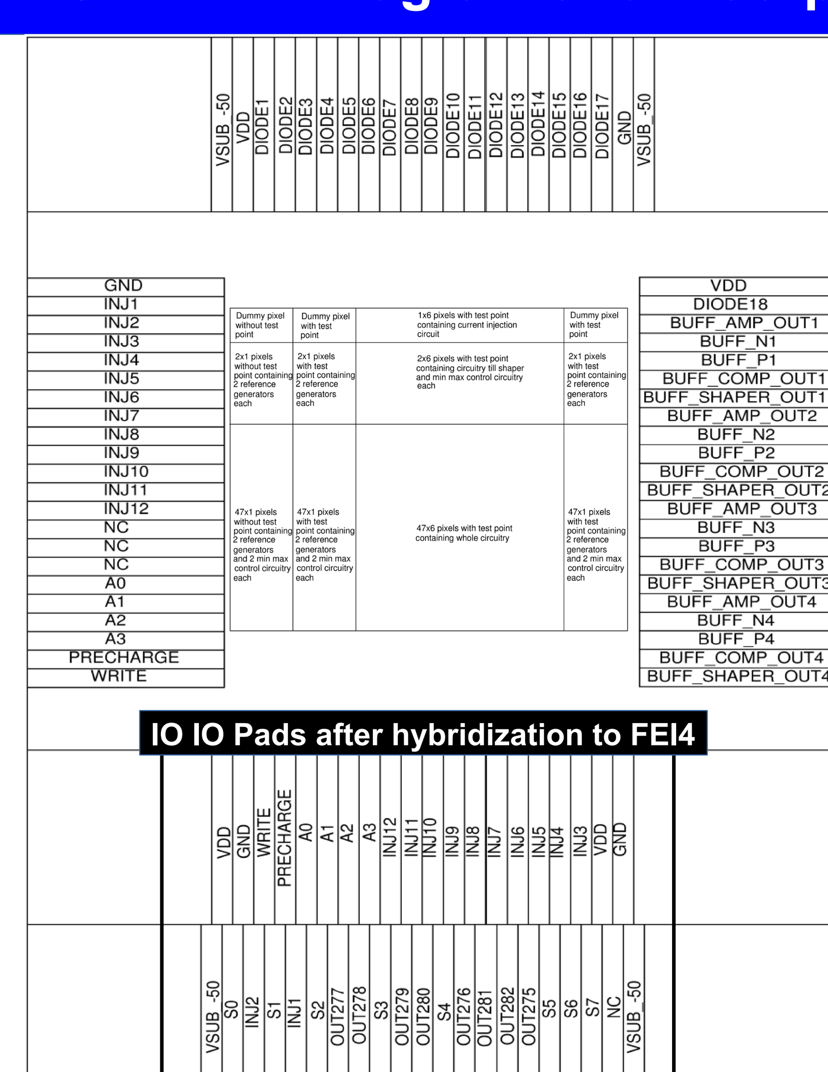
Second Prototype Submission: KE15AA





- **Features of the submitted chip**
  - Compatible to FEI4;
  - Area: 3X4 mm²
  - 282 pixels containing complete chain
  - Pixels containing self biased reference generators and PVT control circuitry
  - Current injection circuitry to mimic the radiation effect
  - Dummy pixels measurement possibilities: 50X50 µm² and 250X50 µm²

KE15AA: Pin Diagram and Floorplan



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