A Prototype of a New Generation Readout ASIC in 65nm CMOS for Pixel Detectors at HL-LHC

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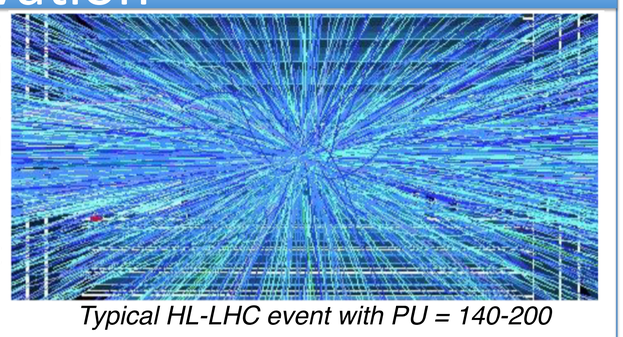
Motivation

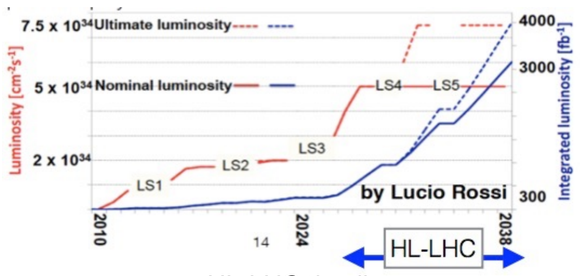
Pixel detectors for HL-LHC experiments require the development of a new generation front-end chip to stand unprecedented radiation levels, very high hit rates and increased pixel granularity.

The main requirements for the HL-LHC detectors:

- Small pixels: 50x50 µm²
- Large chips: 2x2 cm²
- Trigger up to 1 MHz with 12.8 µs latency (100x in both buffering and readout)
- For innermost layer:
  - Pixel hit rate up to 3 GHz/cm²
  - Radiation: 1 Grad in 10 years
  - Data readout up to 4-5 Gbs/s



Typical HL-LHC event with PU = 140-200



HL-LHC timeline

CHIPIX65 project

Approved by INFN in fall 2013, with the goals of:

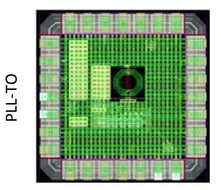
- Developing a CHIP for PIXel detectors using the 65nm CMOS technology for the first time in HEP experiments
- Propagate the use of the 65nm technology inside INFN
- 8 sections involved (Bari, Lecce, Milano, Padova, Pavia/Bergamo, Perugia, Pisa, Torino)
- Funding members of the CERN RD53 collaboration

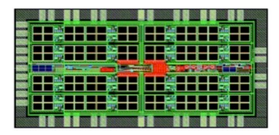
Radiation characterisation
- x-ray machine at LNL / Pd-INFN)
  - Total Ionising Dose (TID)
  - 1 GRad in ~ 2 weeks
- Low-p at CN accelerator LNL
  - TID and Total Displacement damage
- TANDEM / SIRAD
  - Single Event Effects - with Heavy Ion
- Studies on n-MOS, p-MOS
- Irradiation of IP-block, Noise measurements vs Irradiation

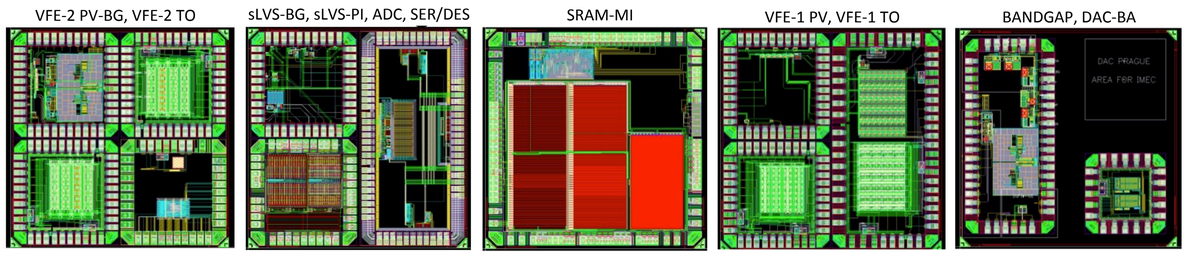
- Band Gap : **Pavia/Bergamo**
- DAC :**Bari**
- SLVDS driver : **Pavia/Bergamo, Pisa**
- SLVDS receiver : **Pavia/Bergamo,Pisa**
- PLL : Torino, (Padova)
- SER : **Pisa**
- DES : **Pisa**
- Monitoring ADC : **Bari**
- SRAM EOC : **Milano**
- Dual Digital Cell : Milano
- DC-DC : Lecce

- Analog-VFE synch : **Torino**
- Analog-VFE asynch : **Pavia/Bg**

Digital Electronics:
- Simulation Framework (**Perugia**)
  - System-Verilog-UVM (VEPIX53)
- Digital Architecture Studies (**To/Pg**)
- Digital Design (**Torino**)

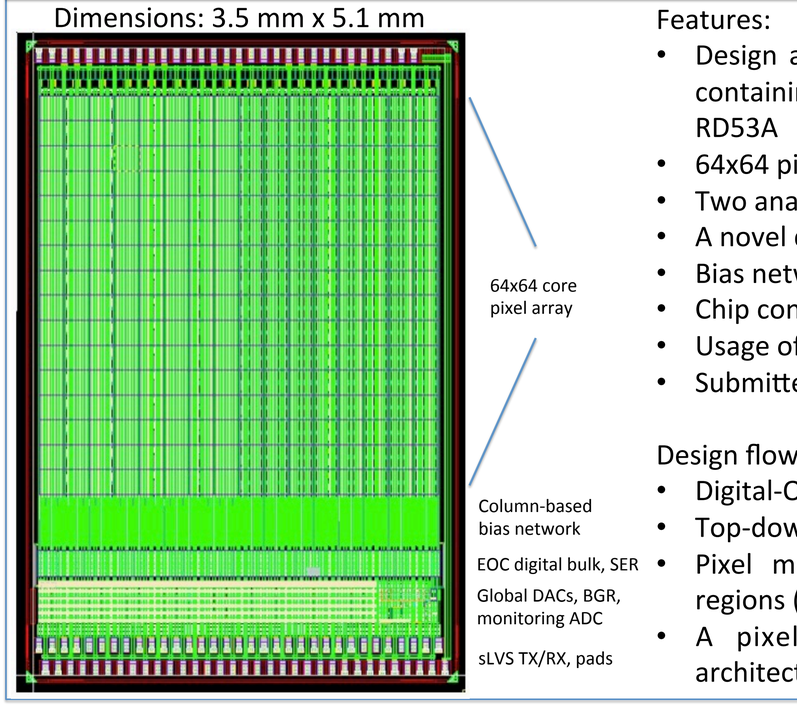






CHIPIX65 demonstrator

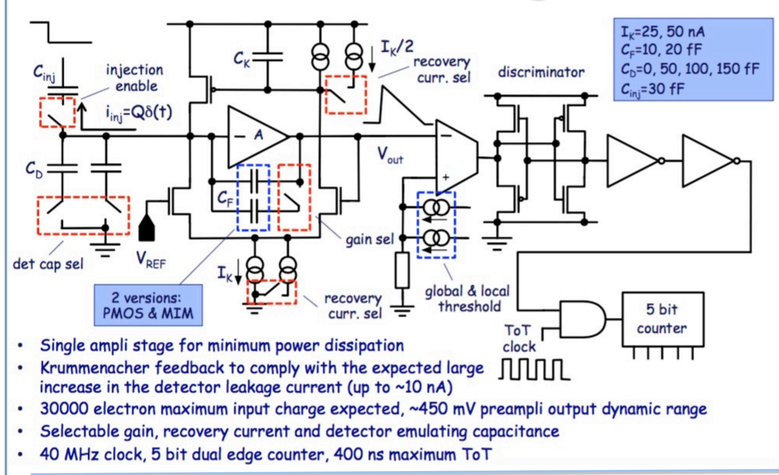
Dimensions: 3.5 mm x 5.1 mm



Features:
- Design a small and complex pixel matrix containing new solutions compatible with RD53A
- 64x64 pixels (50x50 µm² each)
- Two analog FEs (asynch and synch)
- A novel digital architecture
- Bias network and monitoring
- Chip configuration based on SPI protocol
- Usage of CERN I/O library
- Submitted in late June 2016

Design flow:
- Digital-On-Top chip assembly
- Top-down hierarchical flow
- Pixel matrix composed of 16x16 pixel regions (master and clone)
- A pixel region contains the digital architecture and the analog FEs

Analog front-ends



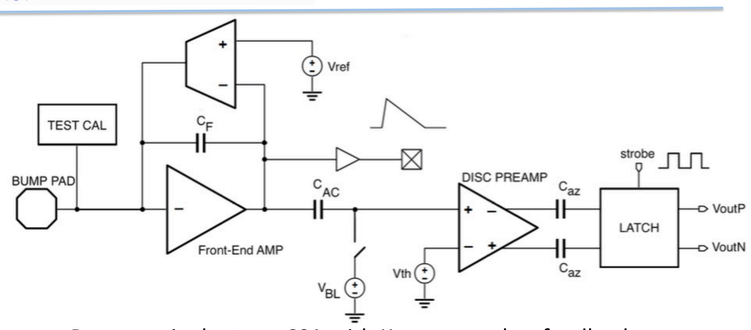
- Single ampli stage for minimum power dissipation
- Krummenacher feedback to comply with the expected large increase in the detector leakage current (up to ~10 nA)
- 30000 electron maximum input charge expected, ~450 mV preampli output dynamic range
- Selectable gain, recovery current and detector emulating capacitance
- 40 MHz clock, 5 bit dual edge counter, 400 ns maximum ToT

ASYNCHRONOUS ARCHITECTURE

- Two small prototypes submitted and tested
- Noise performance and response timing fully compliant with the specs
- No significant effects of leakage current (up to 15 nA) on signal shape and charge sensitivity
- TID irradiation performed up to 800 Mrad: minor changes in signal shape and charge sensitivity. About noise with C_{det}=50 fF: less than 10% increase in ENC after 500 Mrad, less than 20% after 800 Mrad

SYNCHRONOUS ARCHITECTURE

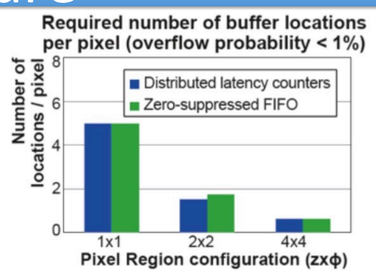
- Two small prototypes submitted and tested
- Noise performance:
  - ENC = 80 e- @ C_{det} = 50 fF for fast ToT (1 MIP in 150 ns)
- TID irradiation performed up to 600 Mrad
  - No significant variations in the signal amplitude
  - 10% noise increase @ C_{det} = 50 fF
  - Fully working



- Preamp: single stage CSA with Krummenacher feedback
- Synchronous discriminator AC coupled to the first stage
- Offset compensation done with capacitors (no trimming needed)
- Fast ToT using the latch as a local oscillator (up to 800 MHz)

Digital architecture

Pixel region choice:
- Focused on a centralised fully shared latency buffer
- 4x4 pixel region
  - Allows better sharing of resources like trigger matching
  - Number of memory locations/pixel should scale by a factor of about 2



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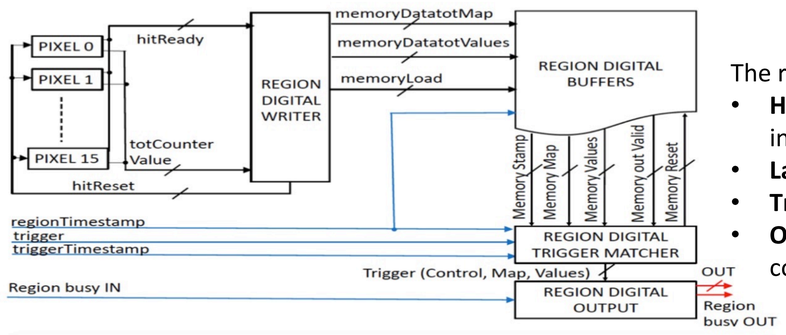
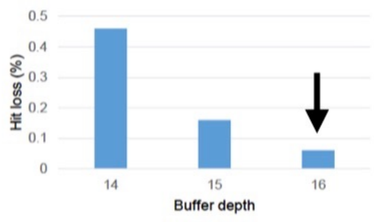


The region digital logic is composed of:
- **Hit mapper/writer** – manages the pixel interfaces and drives the latency buffer
- **Latency buffers**
- **Trigger matcher**
- **Output FSM/MUX –** implements the column drain protocol

LATENCY BUFFER

- The event inefficiency depends on the number of latency buffer locations: 16 locations have been used in the CHIPIX65 demonstrator determining inefficiency < 0.1 %



SUMMARY OF THE ARCHITECTURE PERFORMANCES

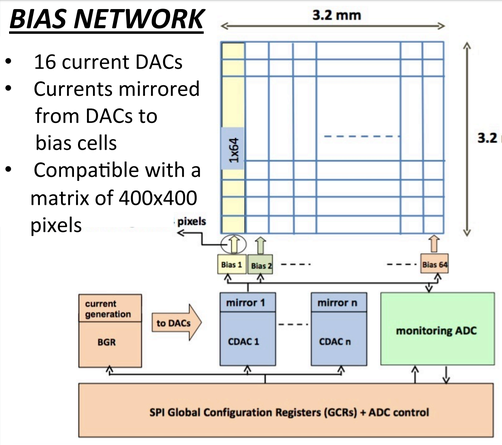
	Inefficiencies (digital) @ 3 GHz/cm²
Trigger latency	12.8 µs
Particle loss	<0.1%
Single pixel efficiency	99.9% (digitized 5-bit ToT info except for 0.4% with binary info only)
Ghosts probability	<0.03%

- Digital region operating modes
  - Triggerless/triggered/debug
  - Binary Only/5-bit-ToT
  - High/Low deadtime (to match Slow or Fast ToT from analog)
- Total power: around 6 µW/pixel

Bias and monitoring

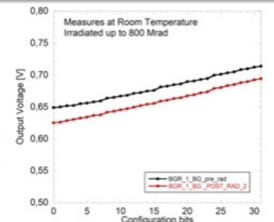
BIAS NETWORK

- 16 current DACs
- Currents mirrored from DACs to bias cells
- Compatible with a matrix of 400x400 pixels



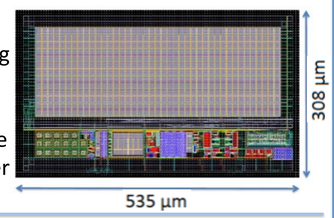
BANDGAP

- Temperature range: -40°C/80°C
- Irradiated up to 800 Mrad
- Trimming can correct process and radiation-induced variations with a mismatch < 2%



MONITORING ADC

- 12-bit ADC for monitoring slowly varying signals
- Conversion rate: 5kSample/s
- Voltage-to-current architecture
- Large capacitance for better precision



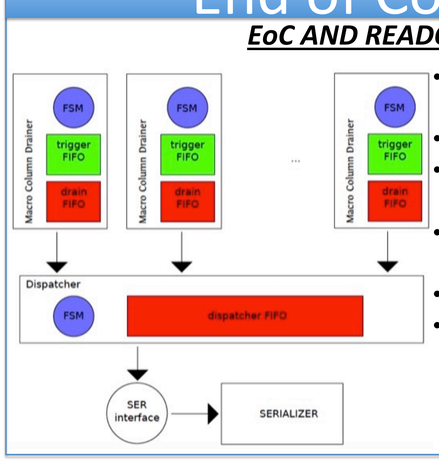
DAC

LSB = 100nA	DNL_{rms}(LSB)	DNL_{max}(LSB)	INL_{rms}(LSB)	INL_{max}(LSB)
Test results (20 DACs)	< 0.15	< 0.4	< 0.45	< 1
MC simulation (500 pts)	< 0.11	< 0.45	< 0.45	< 1.5

- 10-bit current steering DAC – LSB = 100 nA
- 8+2 segmented DAC (2 binary weighted + 8 unitary decoded cells)
- Characterised in lab
- Irradiation tests at Padova X-ray machine showed no significant degradation

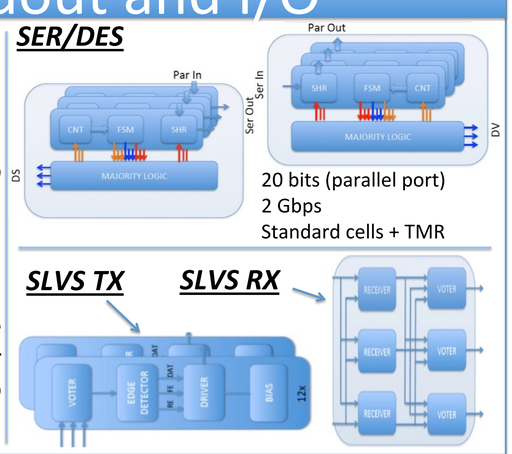
End of Column, Readout and I/O

EoC AND READOUT



- Trigger matched data drained out to EOC
- Timestamp generation
- Trigger timestamp generation
- Column drain protocol implementation
- Buffer the readout data
- Dispatcher prepares the data for serializer including 8b/10b encoding

SER/DES

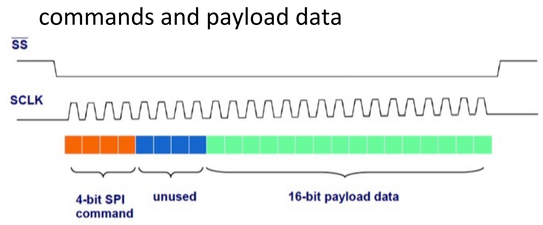


20 bits (parallel port)
2 Gbps
Standard cells + TMR

SLVS TX ***SLVS RX***

Chip configuration

- Configuration at 13.33 MHz using fully-duplex synchronous SPI master/slave transactions
- 24-bit SPI words contains configuration commands and payload data



Conclusions

- CHIPIX65 is a INFN project with around 40 people and 8 institutes and is a very active part of the CERN RD53 collaboration
- Two analog VFE have been designed, tested and irradiated
- Several IP-blocks have been developed, tested and irradiated
- The chip contains a novel Pixel Region architecture with digital inefficiency <0.1% at the HL-LHC rate (3 GHz/cm²) and providing 5-bit ToT information of 99.6% of hits
- The CHIPIX demonstrator, containing a matrix of 64x64 pixels, is an intermediate step towards the RD53A prototype
- The chip has been submitted at the end of June 2016

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