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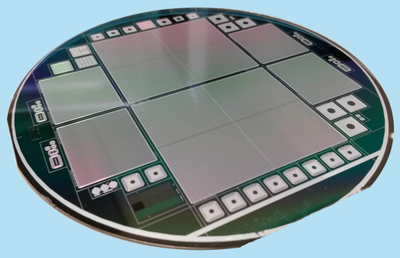

Large Area Thinned Planar Sensors for Future High-Luminosity-LHC Upgrades

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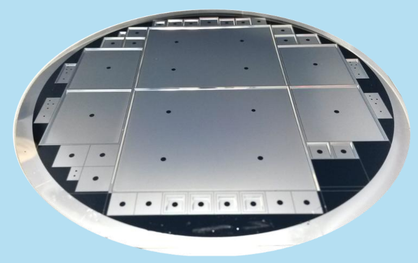

Motivation

Planar hybrid silicon sensors are a well proven technology for past and current particle tracking detectors in high energy physics experiments. However, the future high-luminosity upgrades of the inner trackers at the LHC experiments pose big challenges to the detectors. A first challenge is a radiation hardness up to a fluence of $2 \cdot 10^{16}$ n_{eq}/cm^2. For planar sensors, one way to counteract the charge loss and thus increase the radiation hardness is to decrease the thickness of their active area. A second challenge is the large detector area which has to be built as cost efficient as possible, i.e. it is aimed for low-cost and large-sized sensors.

Idea

The challenge of producing cost-efficient thin and large-sized sensors is approached by a wet-etching technology. Cavities are etched with KOH to the sensors' back side to reduce their thicknesses. At CiS, this is a well-proven technique from the MEMS field. The challenge within this project was to transfer the technology to the process flow of radiation detectors. A process scheme can be seen in fig.1.

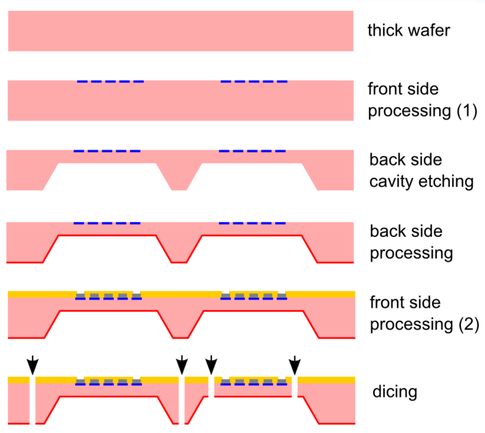

Fig.1: Process scheme

One advantage of this technology is that thick frames remain at the sensor edges and guarantee mechanical stability on wafer level while the sensor is left on the resulting thin membrane. During the dicing step, the frames can be removed in order to obtain completely thin sensors. For this cavity-etching technique, no handling wafers are required which represent a benefit in terms of process effort and cost savings.

Mechanical Results

The CiS has accomplished a proof-of-principle run with n-in-p ATLAS-Pixel sensors where cavities are etched to the sensors' back side to reduce their thicknesses. The wafer layout contains two FE-I4 quad sensors (QS) with a total area of 41x36mm², four FE-I4 single chip sensors (SCS, area of 21x19mm²) and several diodes and test structures. The wafers had a starting thickness of 525µm and were thinned to 150 or 100µm within the active sensor region.

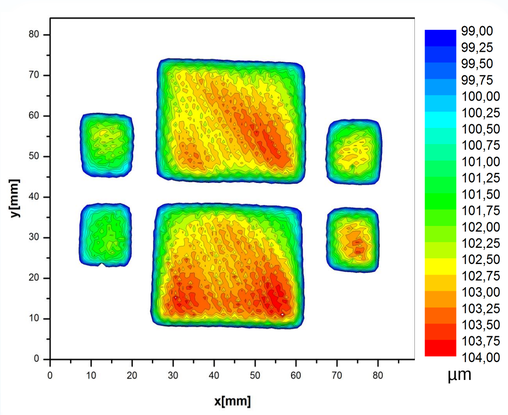

Fig.2: Measured membrane thickness of thinned pixel sensors

The first parameter which has to be surveyed in order to guarantee the compatibility of the cavity etching with the radiation detector technology is the thickness homogeneity of the membranes. Fig.2 shows that finally, thickness fluctuations in the order of only ± 2.5µm for the large, 100µm thick membranes could be reached. The fluctuations for the smaller membrane areas are even less. The roughness of the etched surface was determined via AFM measurements. In fig.3 it can be seen that the height fluctuations are in the order of only some 10nm.
Both measurements show excellent results as the fluctuations are well within the tolerances which are acceptable for radiation detectors.

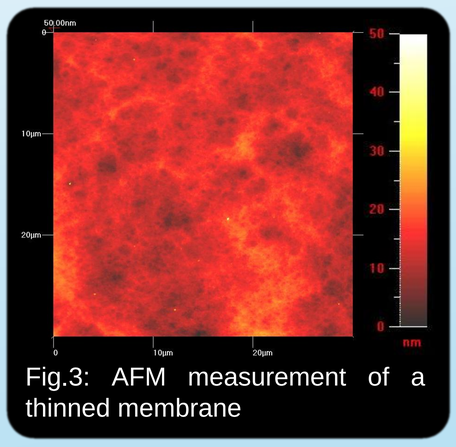

Fig.3: AFM measurement of a thinned membrane

Electrical Results

The prototype sensor wafers have been electrically characterised on the basis of comparable sensor productions like ATLAS pixel or ATLAS IBL. From the CV measurements of diodes (see fig.4), the depletion voltages (V_{depl}) can be read which fit very well to the theoretical calculations: ~15V for 150µm, ~7V for 100µm thick membranes and >200V for not-thinned diodes. The IV characteristic looks very well (see fig.5): The breakdown voltages are mostly more than 50V above V_{depl} which guarantees a stable operation.

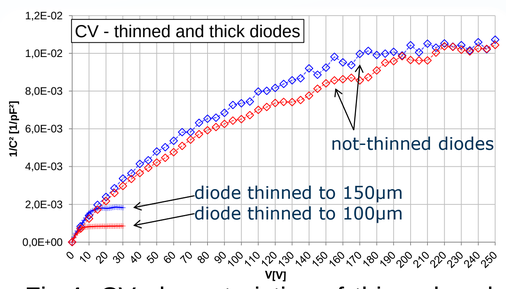

Fig.4: CV characteristics of thinned and not-thinned diodes

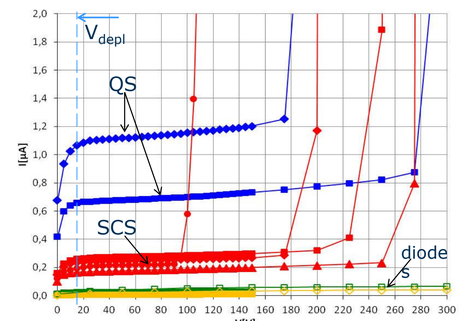

Fig.5: IV characteristics of pixel sensors and diodes, thinned to 150µm

The electrical yields of the different sensor types and thicknesses are plotted in fig. 6. As expected, the yield of the SCS are higher than of the QS, likewise do the thicker sensors behave better than the thinner ones. With a total yield of 76% for the QS and 94% for the SCS, it can be stated that this first prototype run leads to excellent results. It demonstrates that the membrane etching technology could be successfully transferred to the radiation detector process.

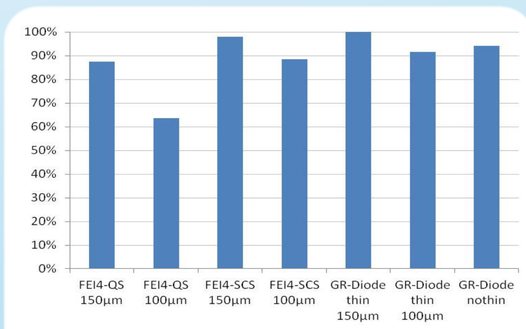

Fig.6: Electrical yields of different sensor types and thicknesses

Post Processing

The first wafers have been followed up by deposition of electroless under bump metallisation (UBM). One part got Ti/Ni/Au, another one got Ti/Pt/Au for comparison. The backside cavities did not present any problem to the deposition process as the wafers are exclusively handled at the edge. The electrical yield of the pixel sensors is 98% for the UBM step.
The saw dicing step was conducted within the thinned regions, close to the guard rings. The mechanical yield for the dicing step is 88%, which is slightly worse than for comparable, conventional productions. This is comprehensible as the dicing step was conducted for the first time for suchlike, thinned radiation detectors.
The first SCS have been successfully assembled with read-out chips at *Fraunhofer IZM*. Source scans (s. fig.7) show that the flip chipping process worked well as for most of the assemblies, only a few missing bumps in the corners are observed.

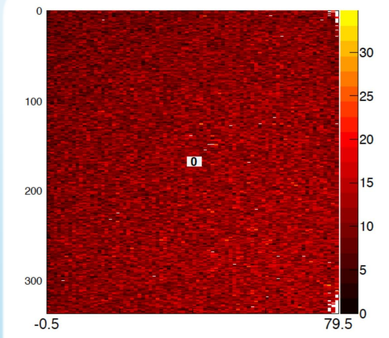

Fig.7: Source scan of FE-I4 single chip assembly *(by courtesy of A.Macchiolo, MPP)*

Conclusion & Outlook

The first prototype run to produce cost efficient thin and large-sized planar sensors shows excellent results. The mechanical properties as well as the mechanical and electrical yields of the sensors are convincing and promising in order to move forward the development of this topic: The technology is currently transferred to 6" wafer size. First results of etching trials with dummy wafers with even larger thinned areas are expected soon.

Acknowledgements

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