# Instrument Control Unit Overview

**CDPU** is the processing module of the Instrument Control Unit (ICU)

CDPU perform the **software based control of the unit**, as well as the processing, digital interfaces and management functions.

CDPU Main Processing : Leon2FT based System-on-chip processor

executes:

**DSW** : sw drivers for functions -> **responsibility of University of Cartagena**

(e.g. read value of ADC channel 1 )

**ASW** : application sw -> **responsibility of OATO - INAF**

(e.g. monitor temperature sensors and check for overflow,

load motor profile and check for overcurrent)

Development of the **ASW on going**:

Design Review expected before end of the Year

DAS not yet available but needed to develop ASW

-> SECOIASIM

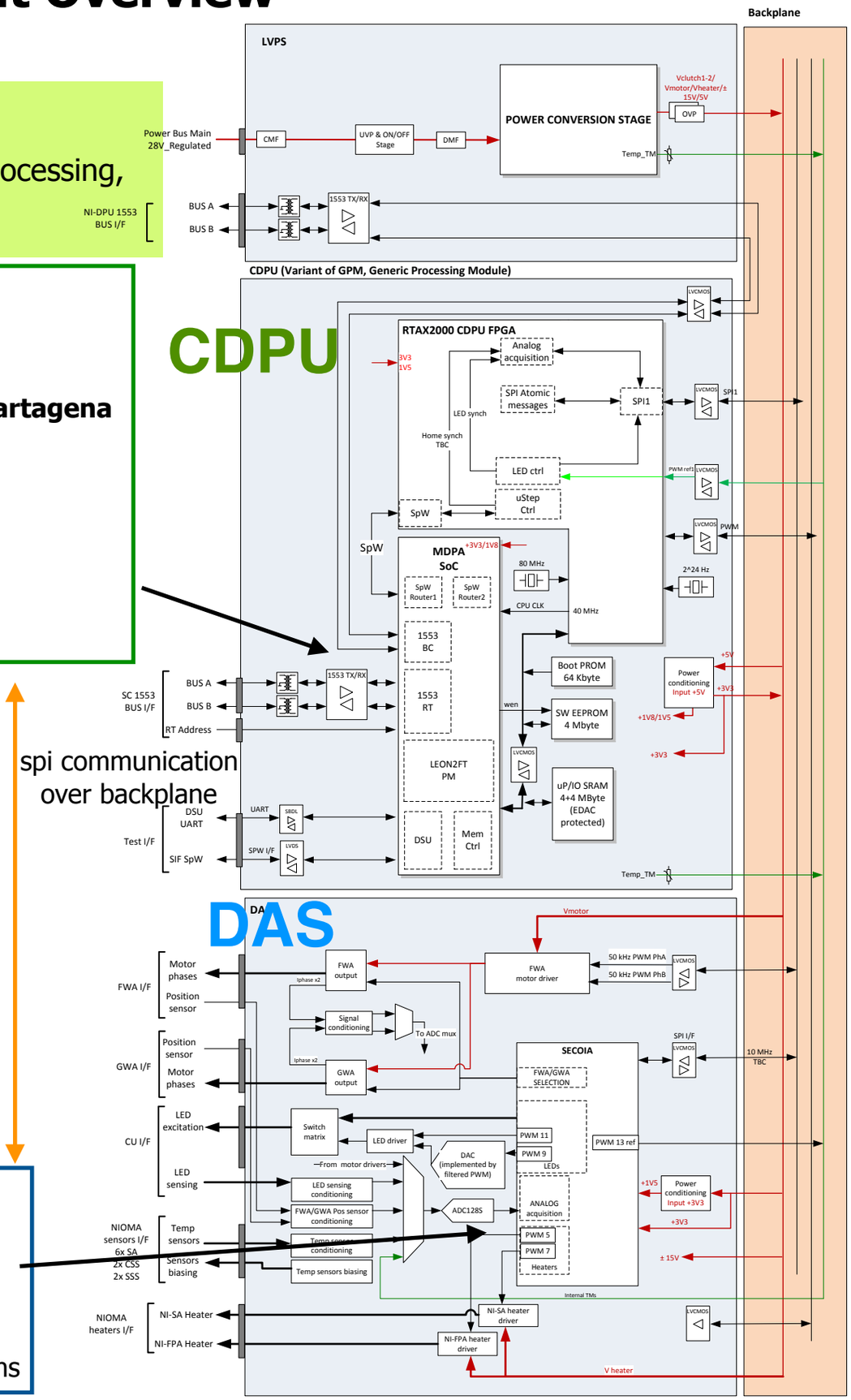
**DAS board:** instrumentation interface

DAS Main Device:

**Secoia ASIC**

(analog inputs - digital I/O - PWM output)

Motor interface - LED interface - Heaters control - Analog acquisitions



# SecoiaSim  Project : a FPGA-based Secoia Simulator

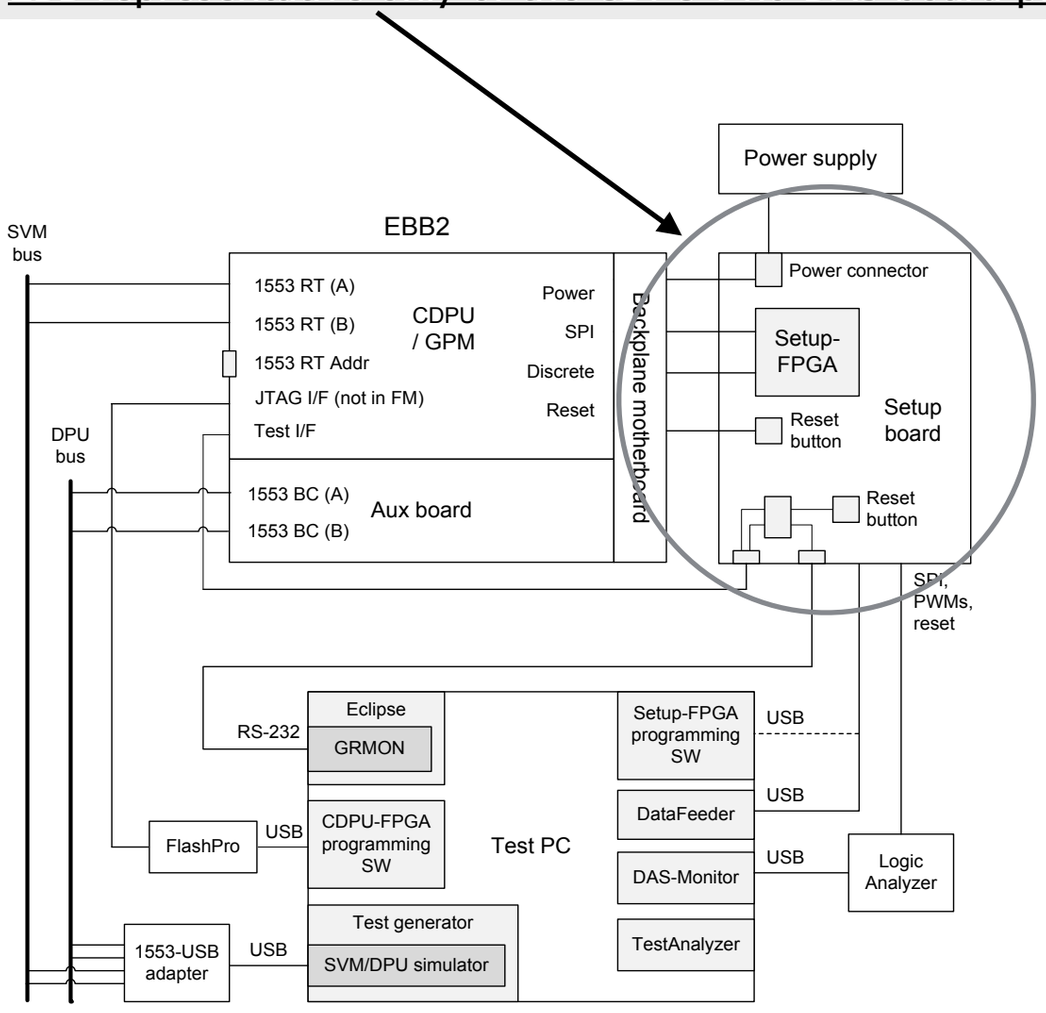
**SecoiaSim : hardware simulator for SECOIA (only a subset of functionalities) implemented with FPGA**
Developed for DSW test , it will be used also to **support the ASW development** and test

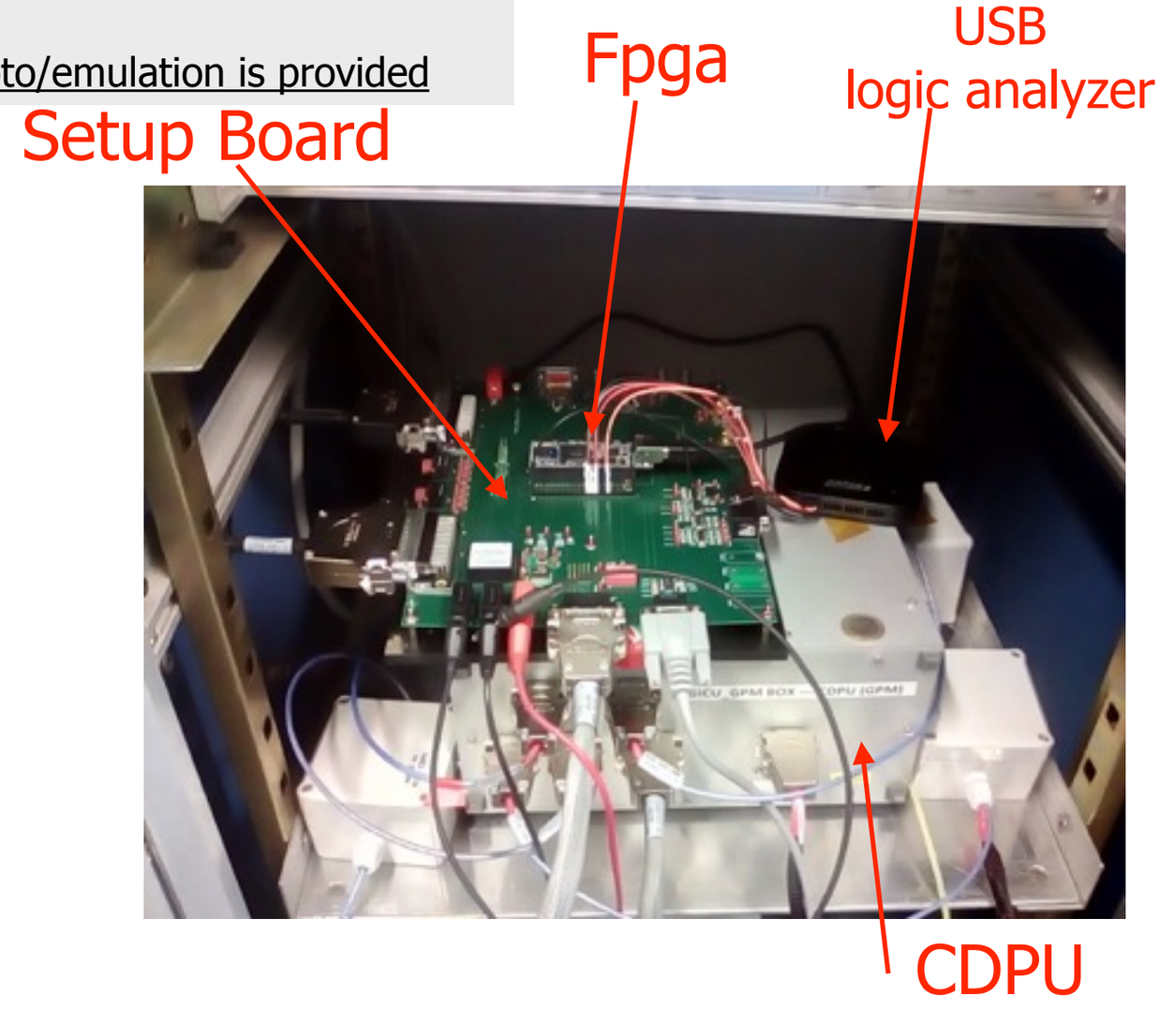
**Coordination** of the project is a **UPCT** (University of Cartagena) responsibility;
**joined** by UAH (Alcala') and **INFN - Bologna**

**Firmware design** shared between UPCT - **INFN-Bologna** - UAH
Software test & developed by UPCT

It is implemented on the FPGA (**Xilinx Spartan 3A**) - based module
hosted into the **ICU-EBB Setup Board** (part of the ICU test bench delivered by CRISA)

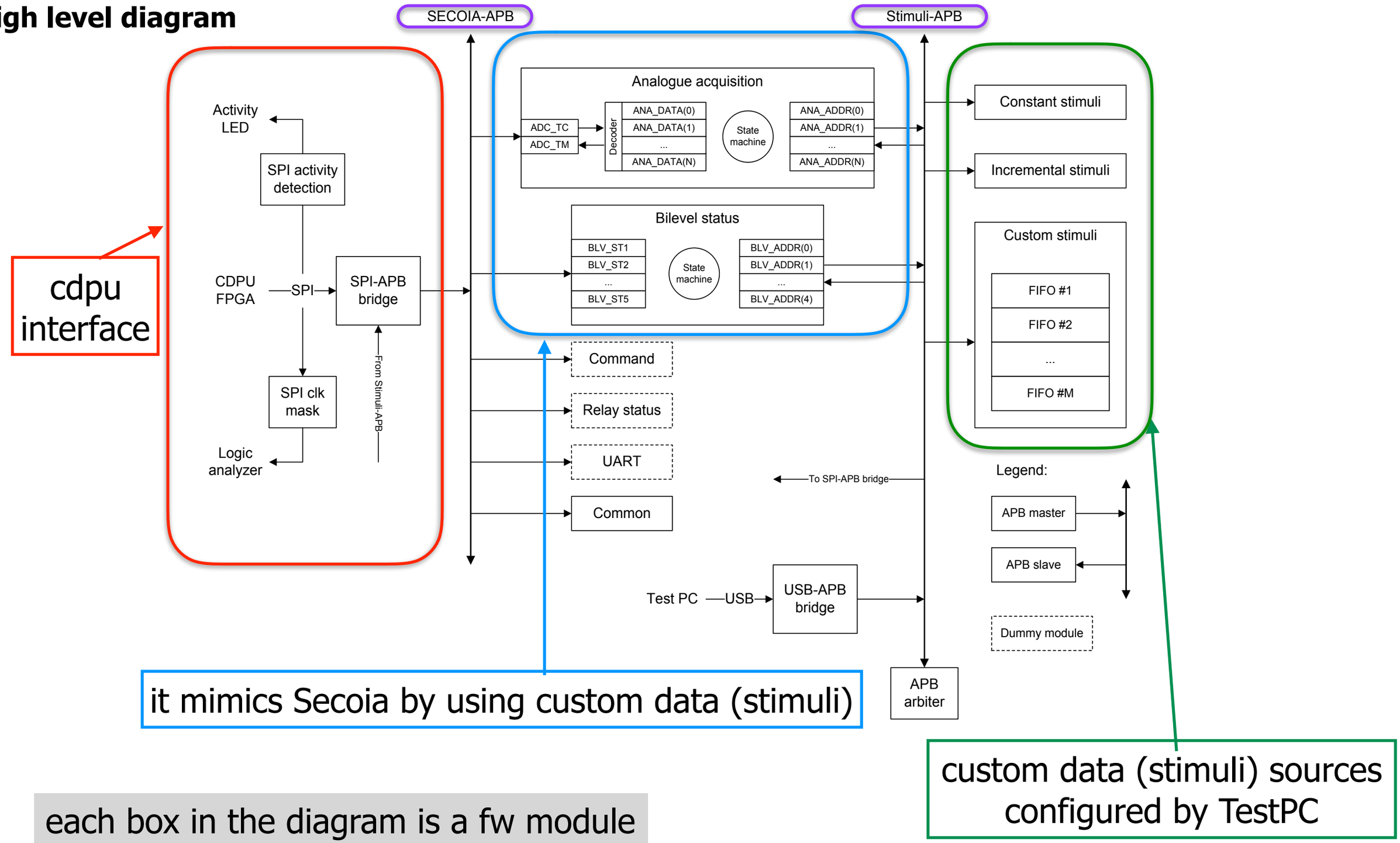
EBB representative only of the CDPU : no DAS board proto/emulation is provided



# SecoiaSim - FW design

## high level diagram




each box in the diagram is a fw module developed independently

Modules are connected using APB bus

# SecoiaSim - Status and Plan

Started in April `16, planned to be ready beginning of July
**Version 1.0 delivered on July16th**

One **test bench** available in Spain devoted to DSW test
**2 in Italy** for ASW test: 1 in OATO, **1 in Bologna**
1 additional FPGA-based mezzanine available in Bologna for dedicated development fw upgrade

**INFN involvement:**

- implementation of about 1/3 of the **VHDL modules (done!)**
- participation in the overall **code review (done!)**
- constant collaboration and consultation with UPCT on **design refinement, bug fixing, design update (on going)**
- supply of the **GIT repository (Baltig)** both for fw and sw

**Status: Italian test stands are operational and ready**

**Future Activities:**
(support) **collaboration with OATO** on both **developing ASW test cases** and properly configuring of the SecoiaSim

i**mplementation of additional features** peculiar to ASW test
(for instance: generation of correct/wrong data answering to a given motor profile)

i**mprove fw performance** (if needed after test cases definition):
(for instance: using the available DDR3 memory to inject a long data sequence)