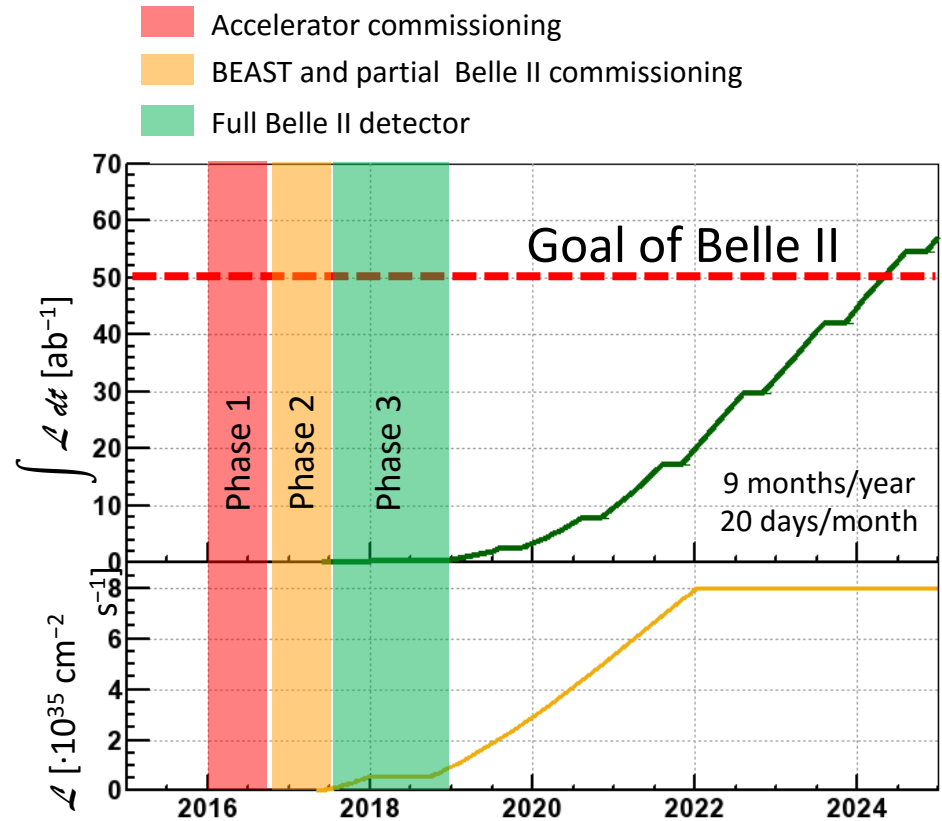
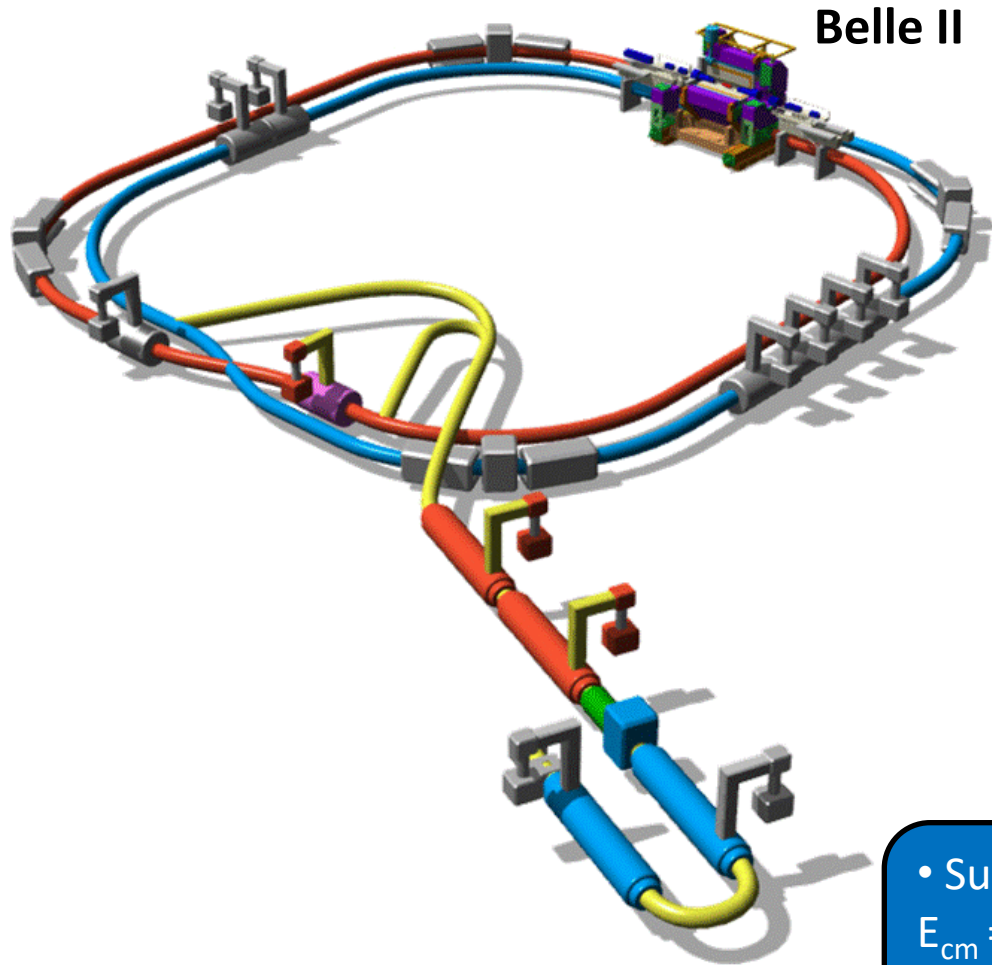


# The Belle II Pixel Detector

DEPFET Collaboration

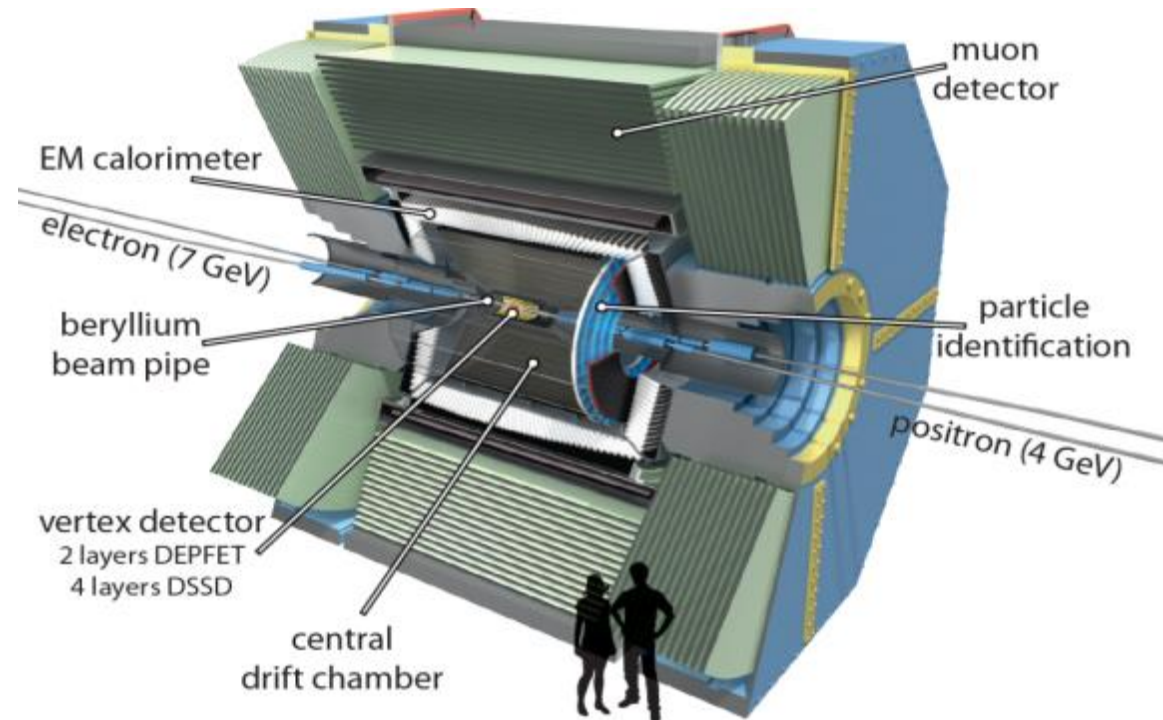
# The SuperKEKB Accelerator



- SuperKEKB: Asymmetric energy  $e^+e^-$  collider  
 $E_{\text{cm}} = m(\Upsilon(4S)) = 10.58 \text{ GeV}$
- Peak luminosity:  $\mathcal{L} = 8 \cdot 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$  (x40 than KEKB)  
Beam size reduction. Higher current.

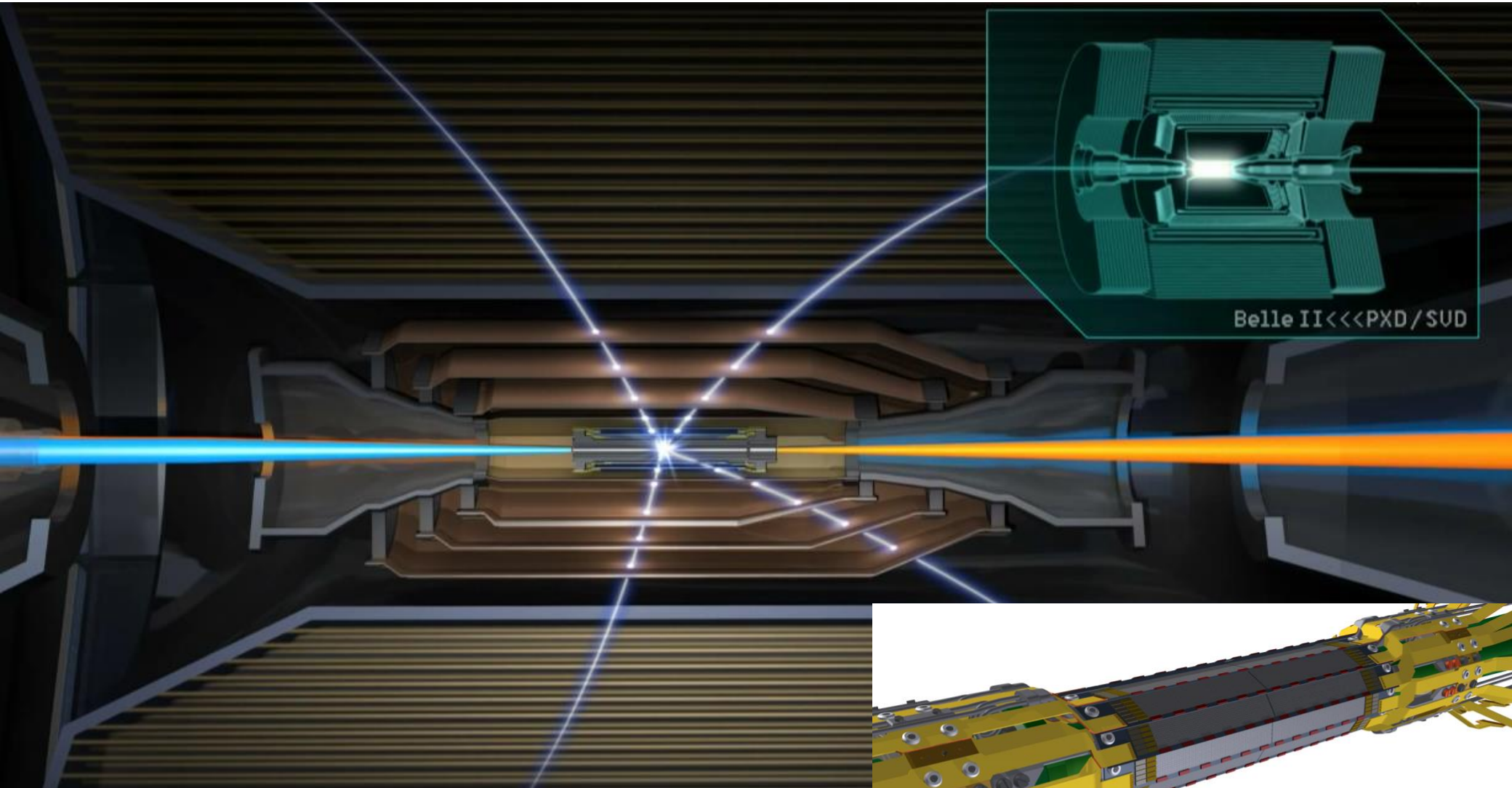
# The Belle II Detector

- Detector requirements
  - Light material
  - **Vertexing capability**
  - Particle identification
  - E.M. calorimetry
  - $K_L^0$  and muon ID
  - Data handling capabilities

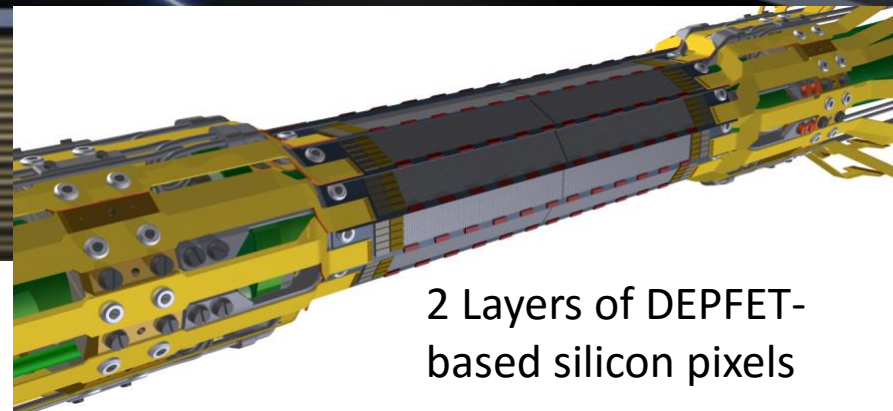


→ New detector: **Belle II**

# The Belle II Pixel Detector



Belle II<<<PXD/SUD

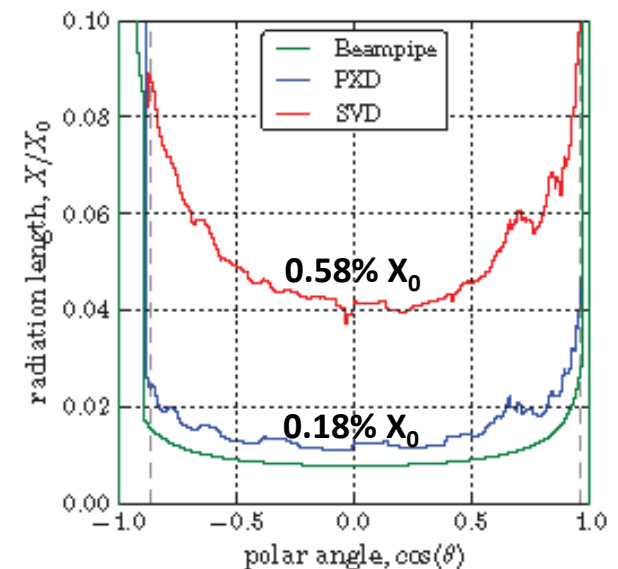
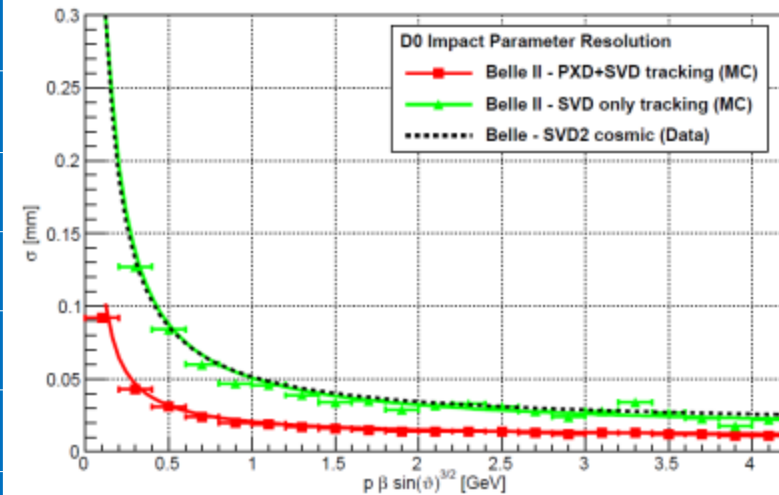


2 Layers of DEPFET-based silicon pixels

# Belle II Vertex Detector Requirements

	Belle II PXD
Occupancy	0.4 hits/ $\mu\text{m}^2/\text{s}$
Radiation	2 Mrad/year
Duty cycle	1
Frame time	20 $\mu\text{s}$
Momentum range	Low momentum ( $< 1 \text{ GeV}$ )
Acceptance	$17^\circ\text{-}155^\circ$
Material budget	0.21% $X_0$ per layer
Resolution	15 $\mu\text{m}$ ( $50 \times 75 \mu\text{m}^2$ )

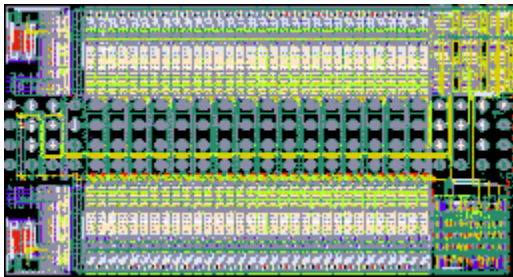
- Modest resolution (15  $\mu\text{m}$ ), dominated by multiple scattering  $\rightarrow$  Pixel size ( $50 \times 75 \mu\text{m}^2$ )
- Lowest possible material budget (0.2%  $X_0$ /layer)
  - Ultra-transparent detectors
  - Lightweight mechanics and minimal services



# The DEPFET Ladder

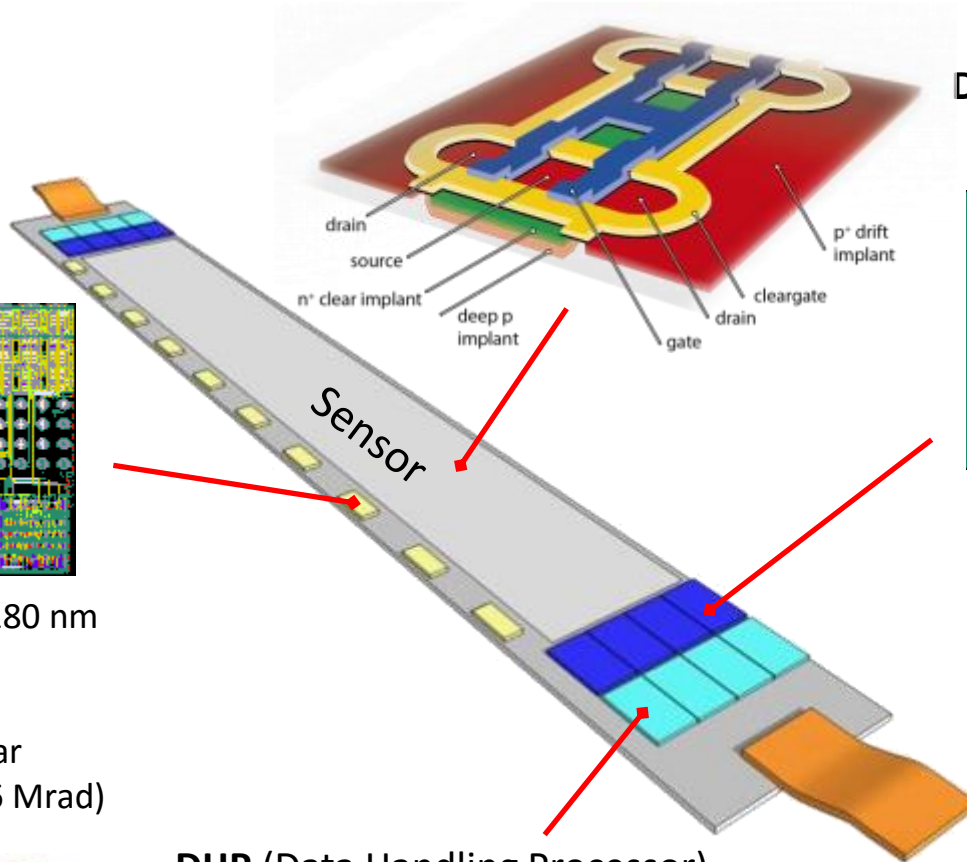
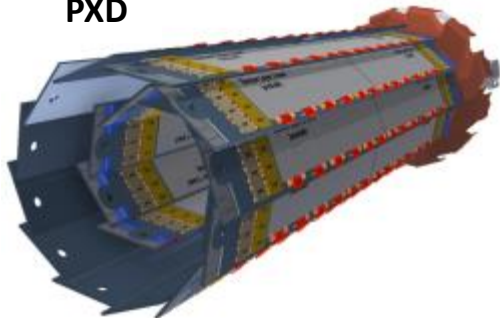
## SwitcherB

Row control

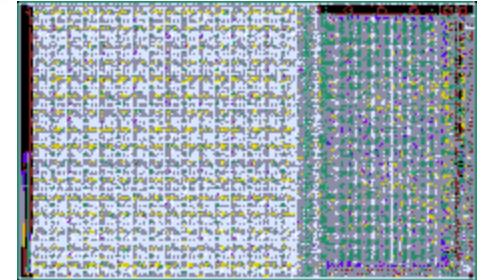


AMS/IBM HVCMOS 180 nm  
 Size  $3.6 \times 1.5 \text{ mm}^2$   
 Gate and Clear signal  
 Fast HV ramp for Clear  
 Rad. Hard proved (36 Mrad)

## PXD

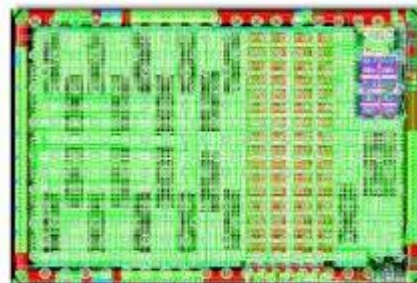


**DCDB** (Drain Current Digitizer)  
 Analog frontend

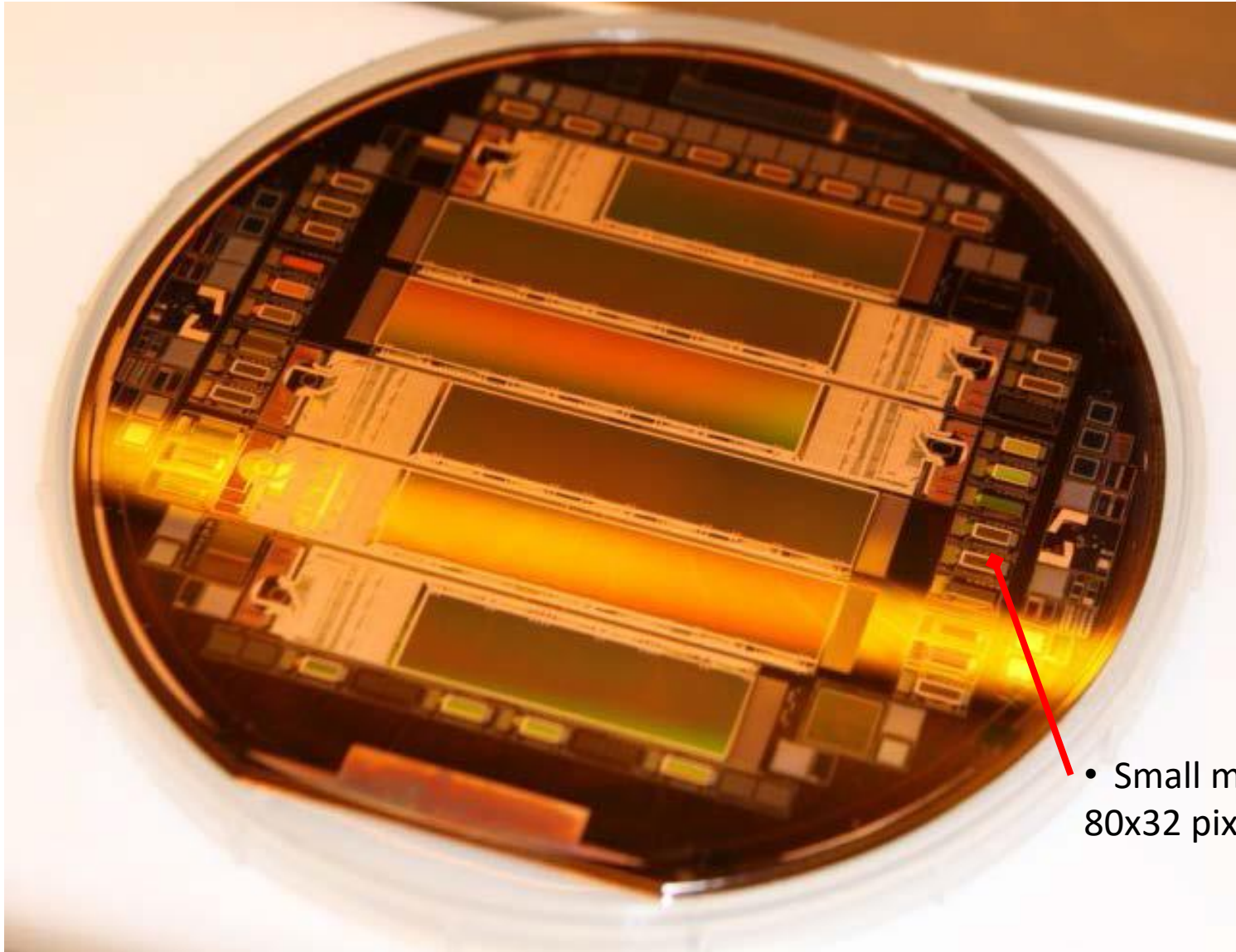


UMC 180 nm  
 Size  $5.0 \times 3.2 \text{ mm}^2$   
 TIA and ADC  
 Pedestal compensation  
 Rad. Hard proved (20 Mrad)

**DHP** (Data Handling Processor)  
 First data compression



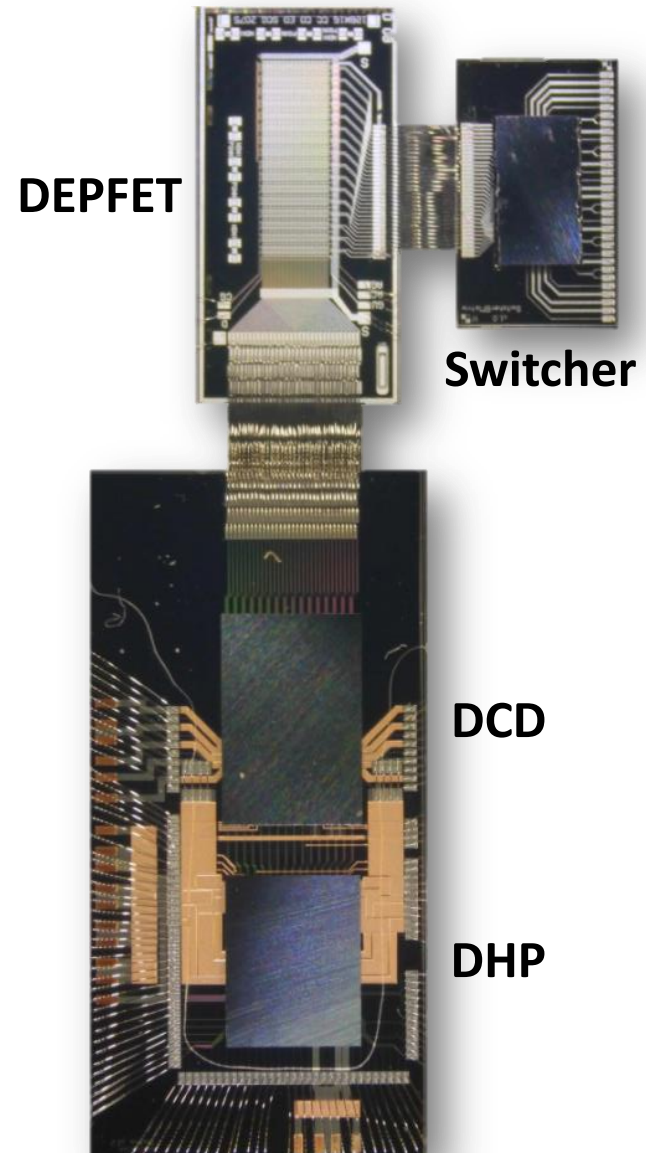
# PXD9: Belle II DEPFET Sensors



- Small matrices  
80x32 pixels

# Hybrid 5 – Full System Demonstrator

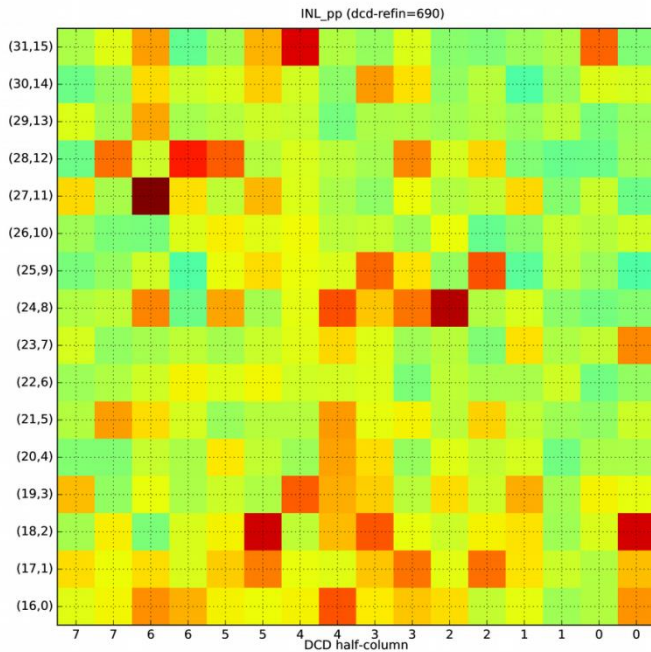
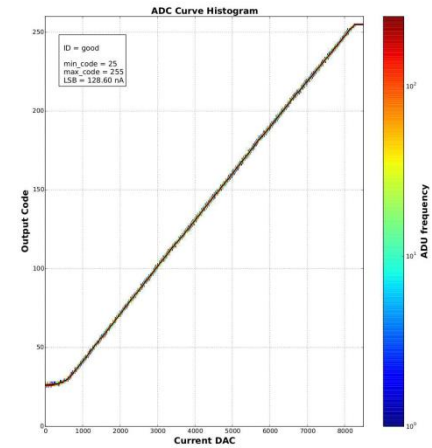
- PXD9 small Belle II type matrix
  - Pixel pitch:  $50 \times 55 \mu\text{m}^2$
  - Thinned to  $75 \mu\text{m}$
  - Gate length:  $5 \mu\text{m}$
  - Thin gate oxide
  - $32 \times 64$  pixels readout
- Final readout chain
  - SwitcherB
  - DCDB
  - DHPT
  - DHH



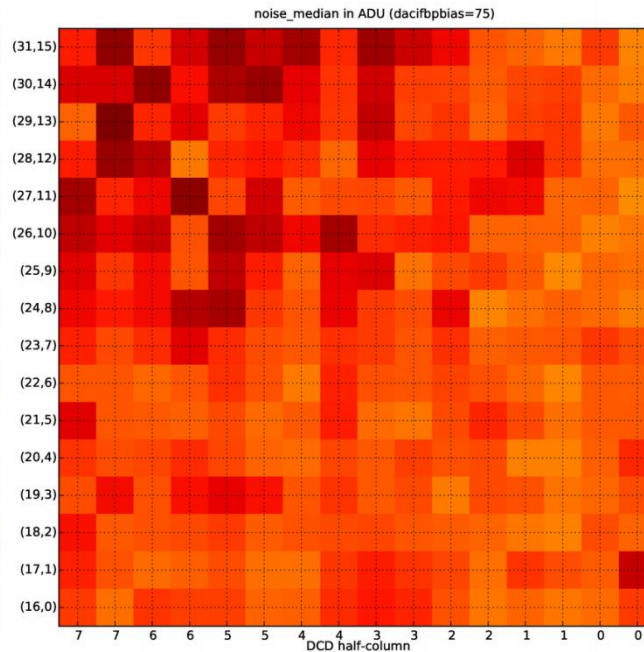


# ASICs Performance

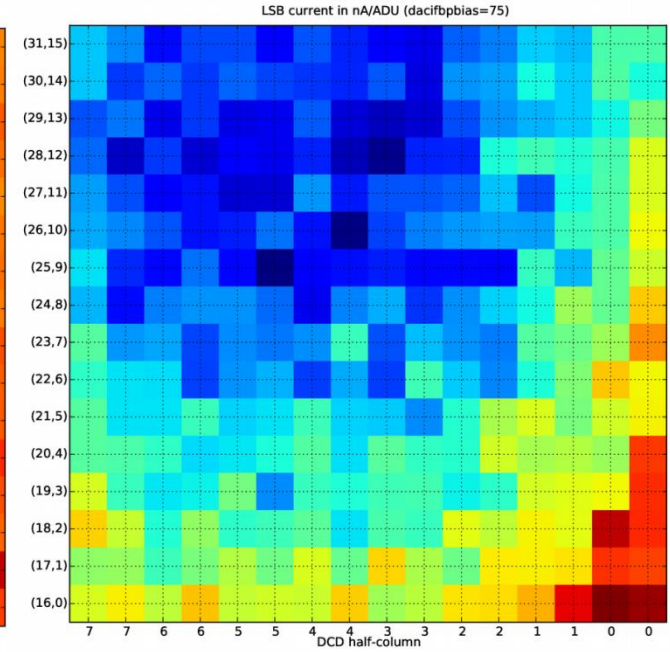
- DCDB4.2  
All channels show good linearity (INLpp < 8 ADU)  
All channels show low noise < 0.55 ADU  
Homogeneous gain map



INLpp < 8 ADU  
Median = 4.5



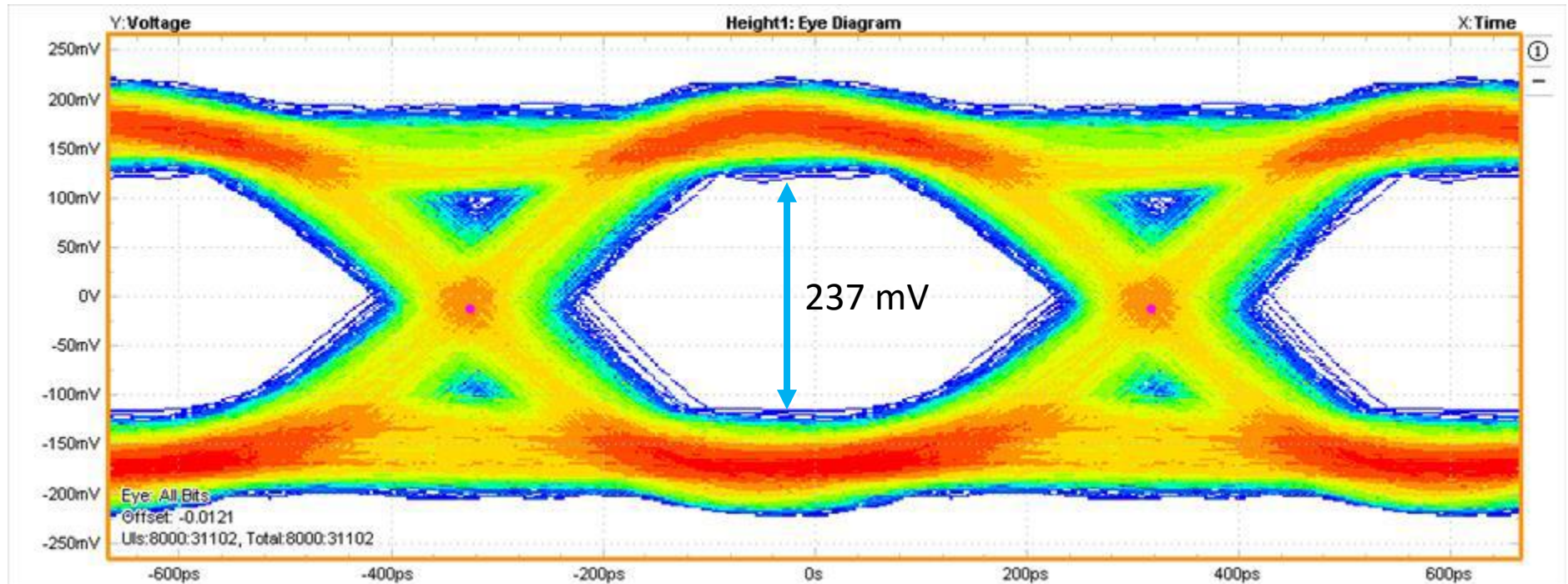
Noise < 0.55 ADU  
Spread < 0.08 ADU



Homogeneous gain  
Min to max variation ~10%

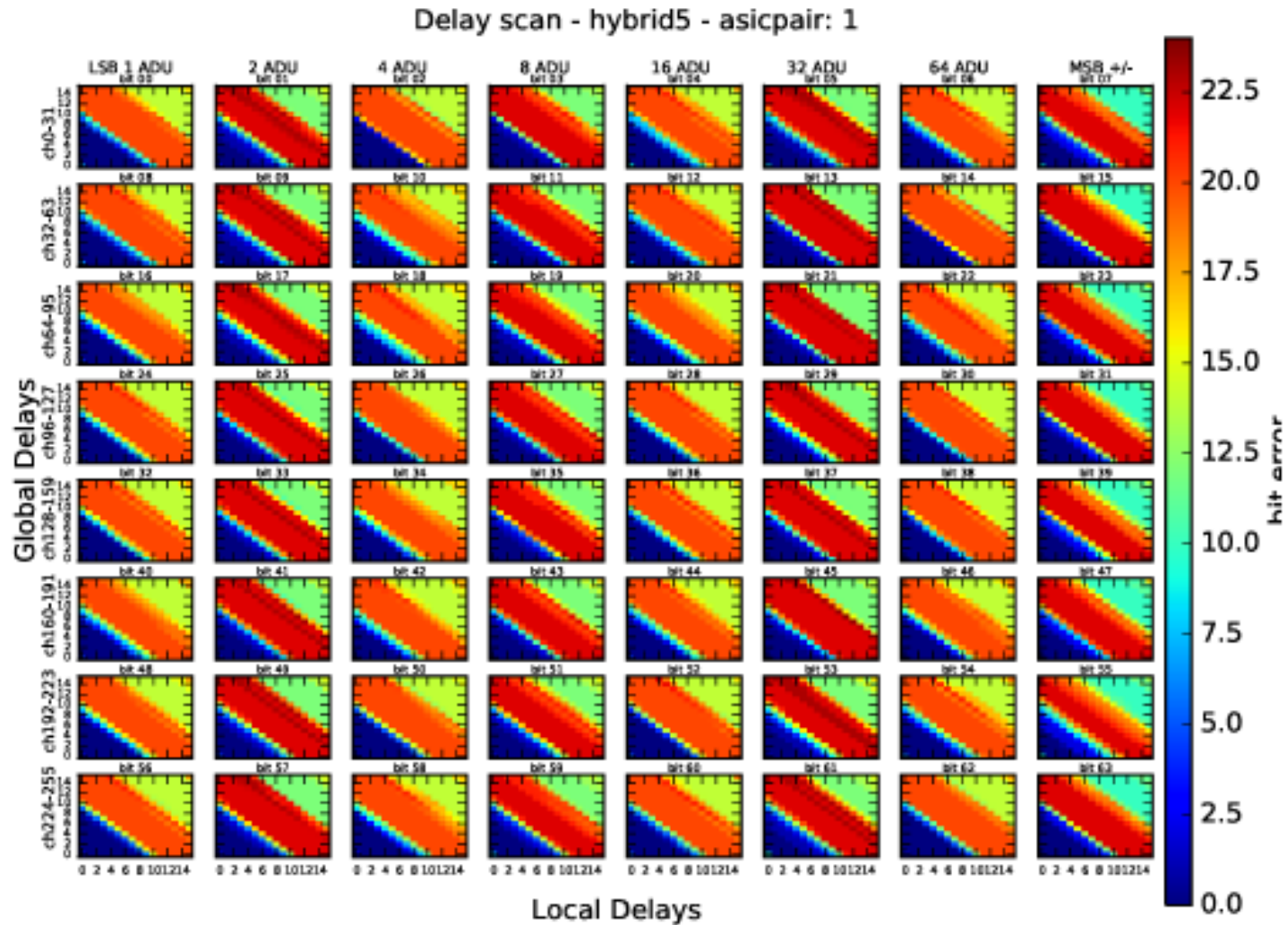
# ASICs Performance

- DHPT1.2: Proper data transmission after 10 m Infiniband cable



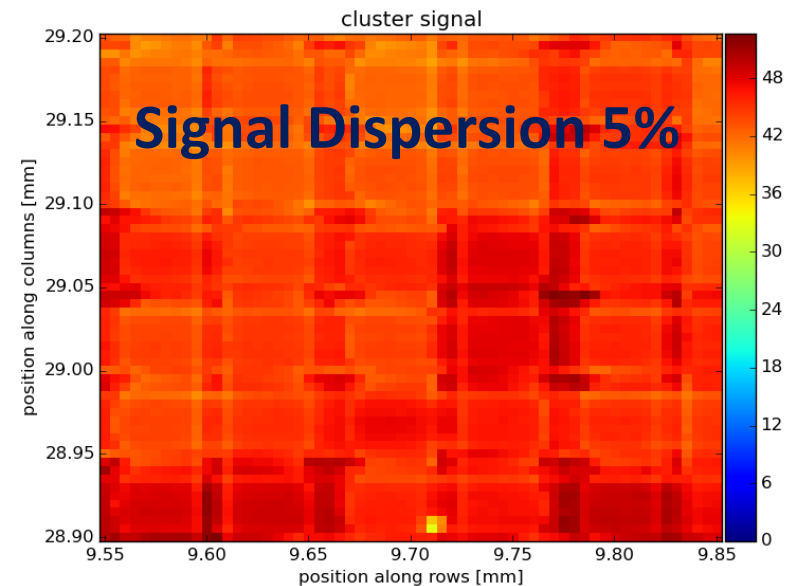
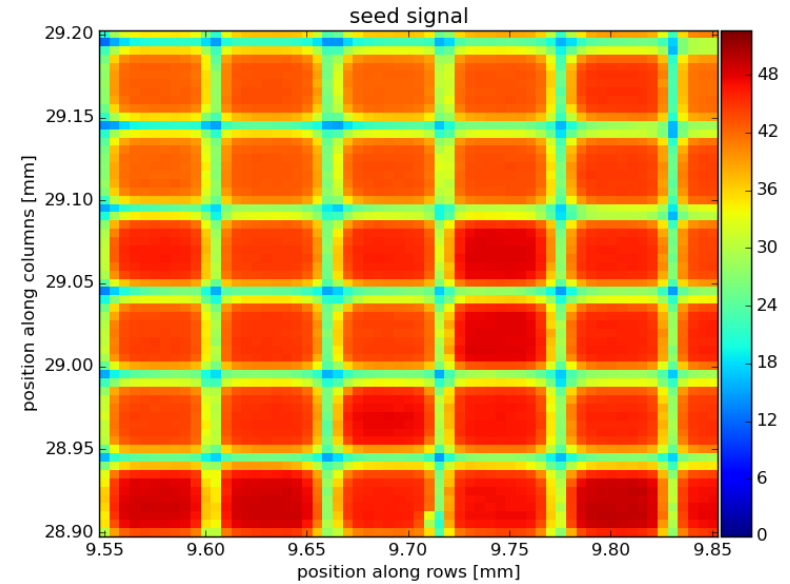
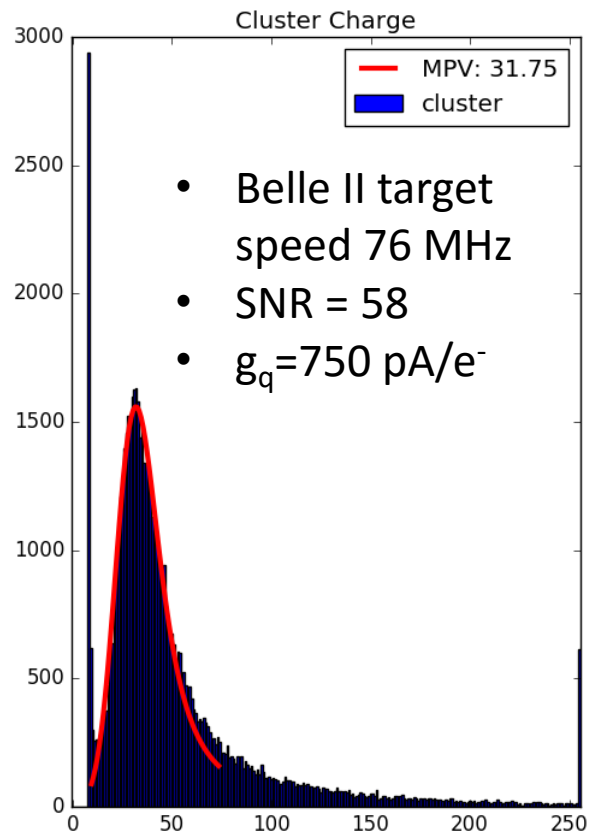
# ASICs Performance

- Error free DCDB4.2-DHPT1.1 communication



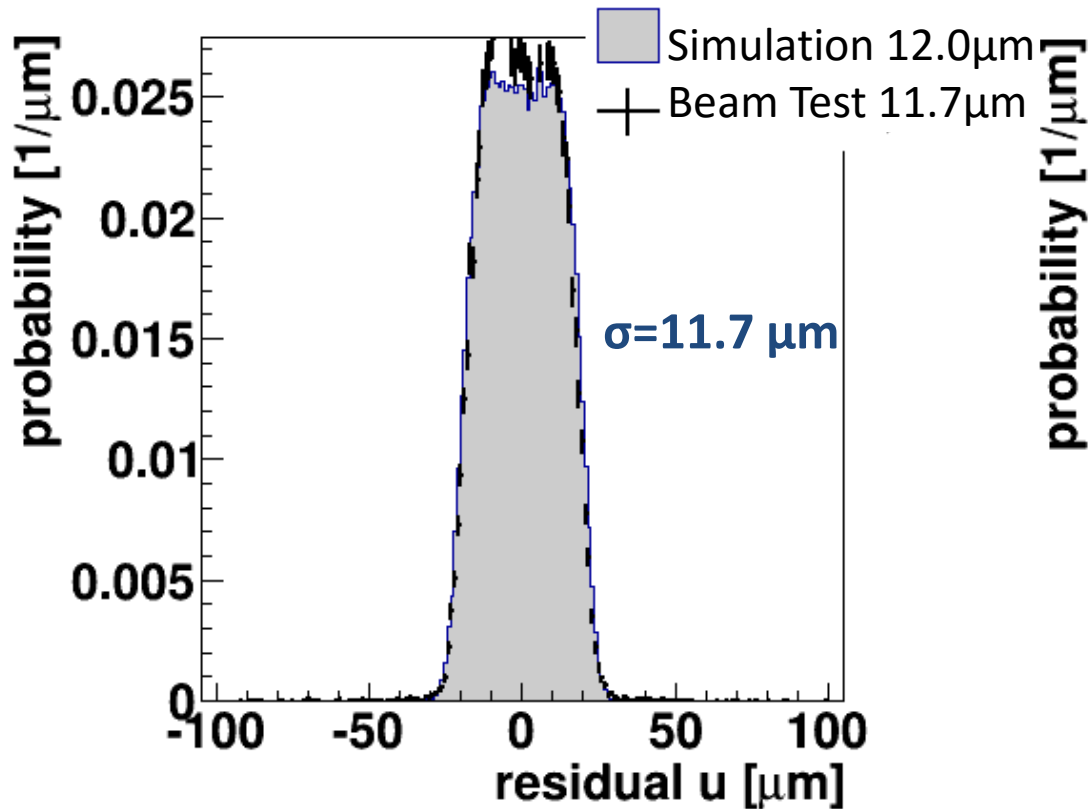
# Belle II DEPFET Sensors

- Optimization of DEPFET voltages
  - Source measurements
  - Laser measurements

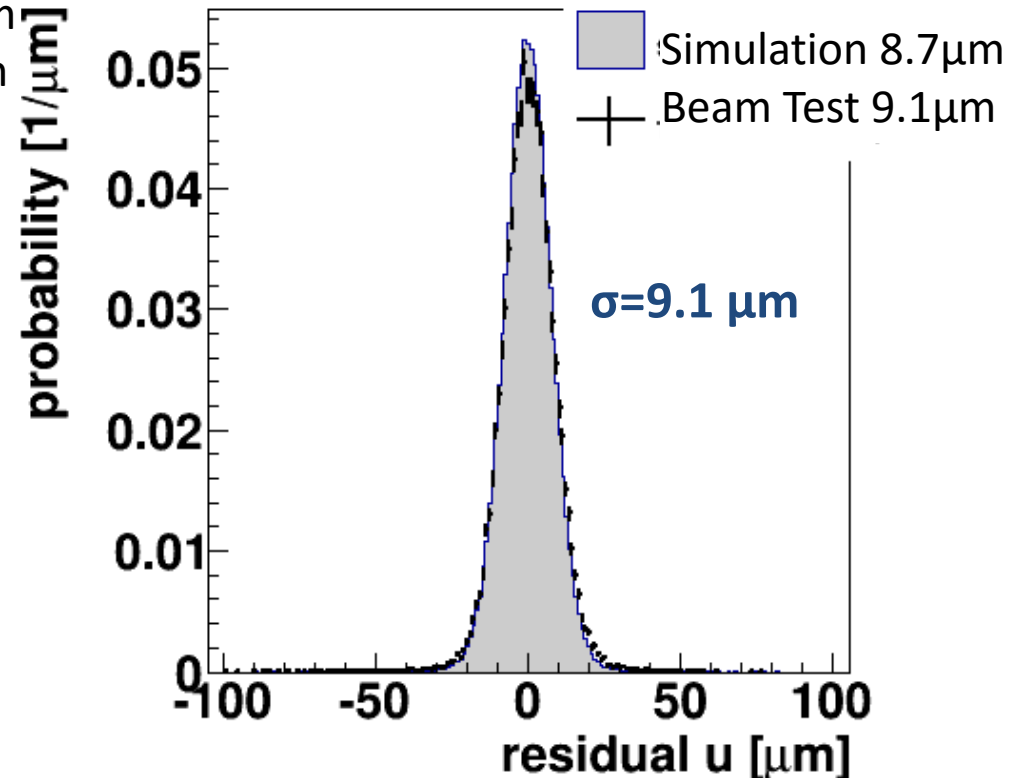


# Belle II PXD Residuals

0° tilt: perp. incidence



30° tilt: many 2 pixel clusters



- Matrix tilted along column: multi-column clusters
- Expectation for single pixel readout:  $\text{RMS} = 50 \mu\text{m} / \sqrt{12} \approx 14.5 \mu\text{m}$

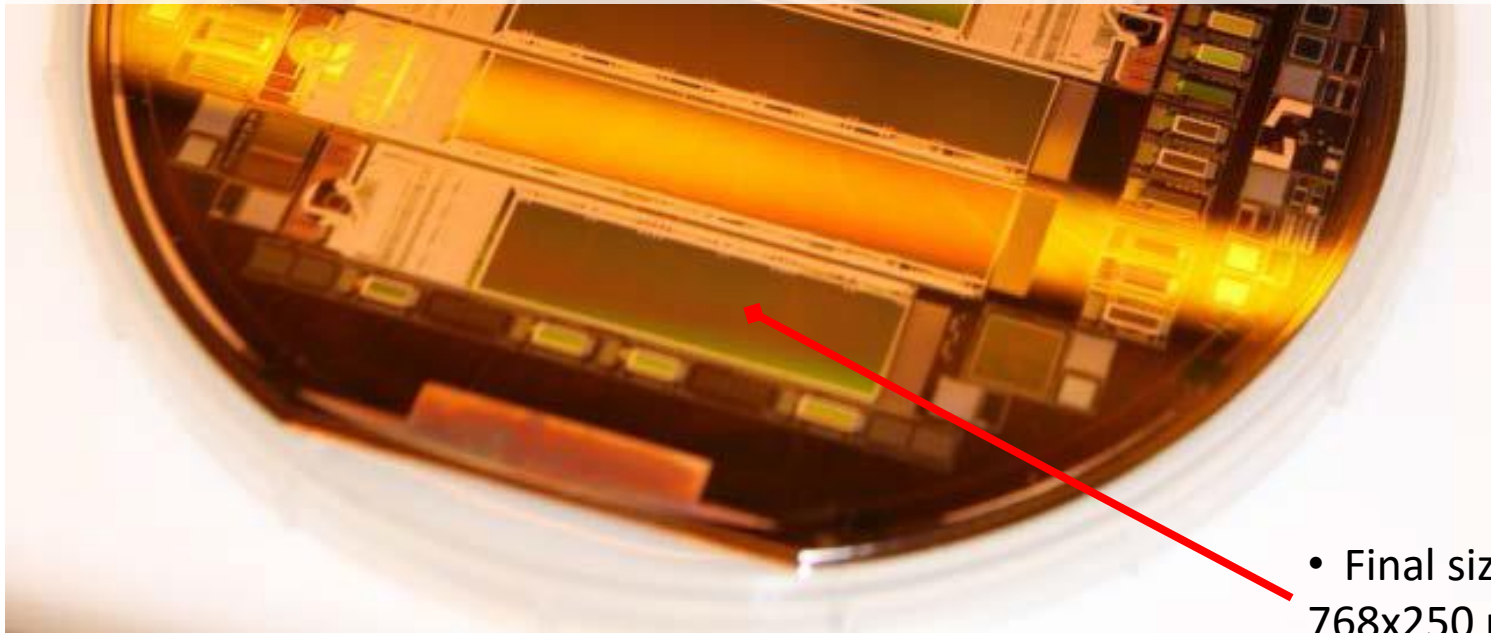
# PXD9: Belle II DEPFET Sensors

- ALL results are satisfactory, as expected by design and also according to simulations:

ASICs performance: Noise, speed, ...

Sensor: Charge collection, signal-to-noise, gain, residuals, ...

→ Not mentioned here: Irradiation campaigns, stability tests, other test vehicles...

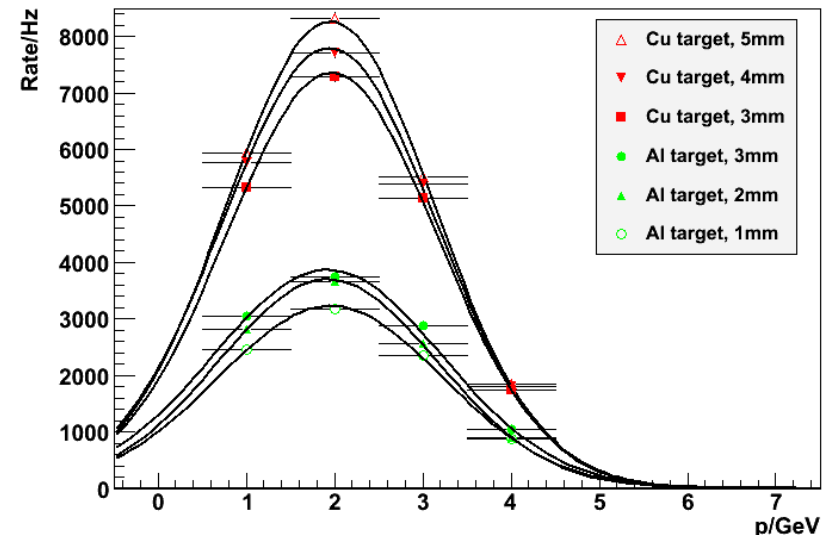


- Final size modules  
768x250 pixels

# DESY TB

- VXD common test beam in April 2016
- Small sector of the final sensors and ASICs\*  
2 PXD + 4 SVD layers
- Complete VXD readout chain: HLT, monitoring, event building, PocketDAQ
- CO<sub>2</sub> cooling, slow control, environmental sensors
- Illumination with (up to) 6 GeV e<sup>-</sup> under solenoid magnetic field (PCMAG)
- Alignment, tracking algorithms, ROI

## ■ Goal: System integration and Phase 2 Commissioning



# Belle II Vertex Detector

- **Silicon Vertex Detector (SVD)**

4 layers of DSSD

$r = 3.8 \text{ cm}, 8.0 \text{ cm}, 11.5 \text{ cm}, 14 \text{ cm}$

$L = 60 \text{ cm}$

$\sim 1 \text{ m}^2$

- **Pixel Detector (PXD)**

2 layers of DEPFET pixels

$r = 1.4 \text{ cm}, 2.2 \text{ cm}$

$L = 12 \text{ cm}$

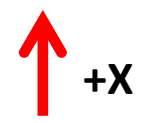
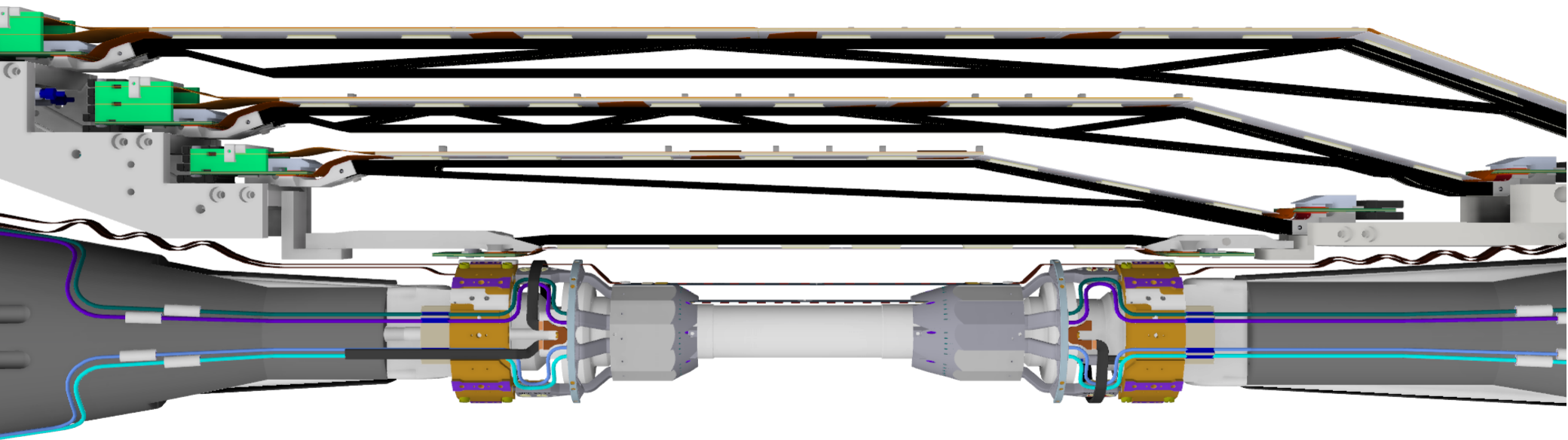
$\sim 0.027 \text{ m}^2$



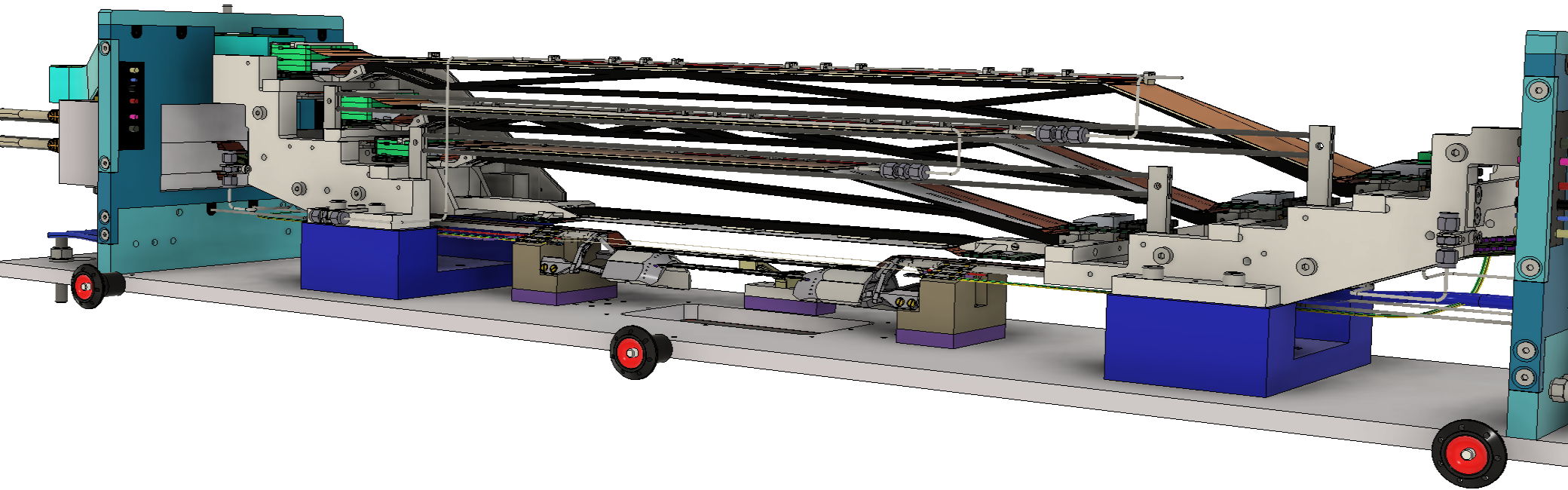
# VXD Phase 2 Hardware

- Two PXD and four SVD layers
- +X direction, horizontal plane (highest background sensitivity)

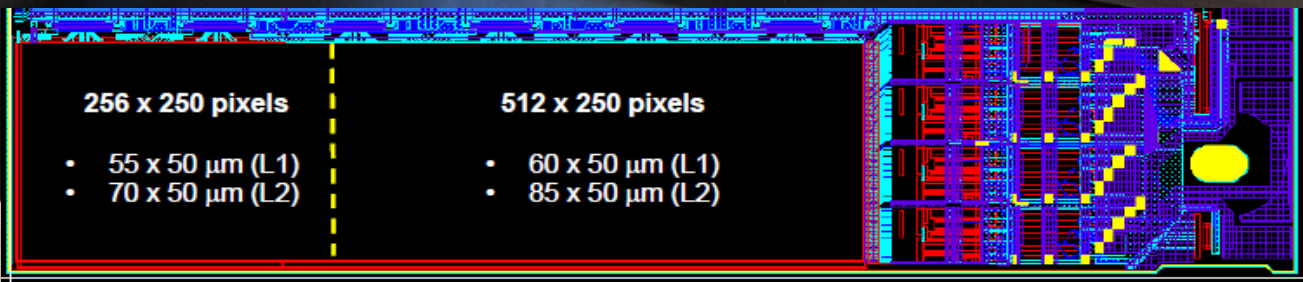
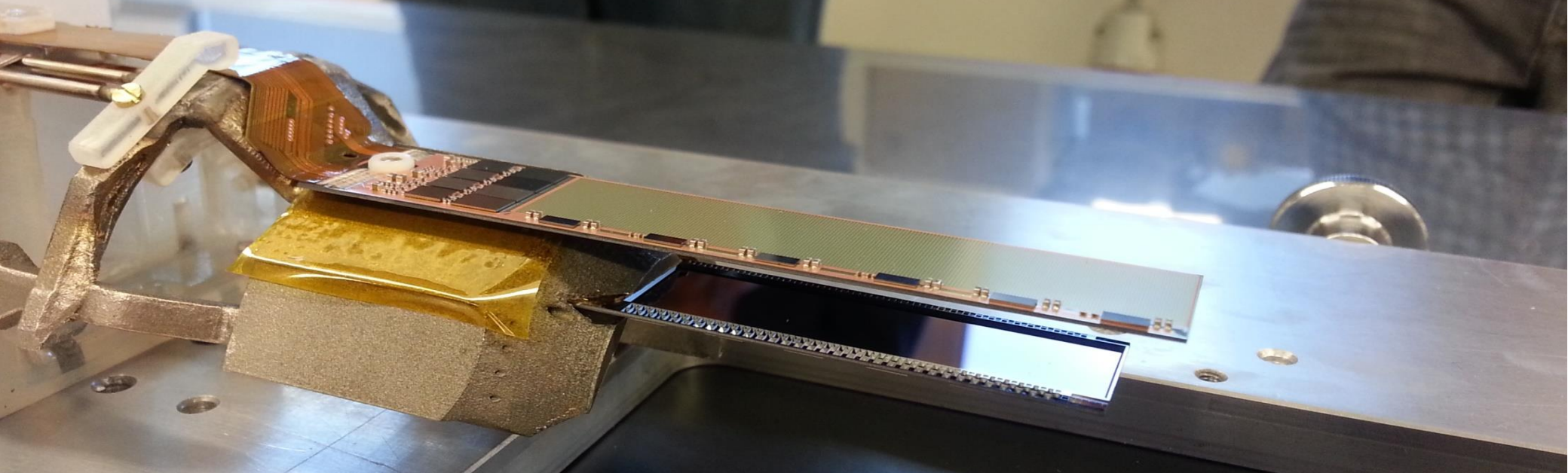
Test Beam set up to mimic Phase 2 arrangement



# Test Beam Set Up



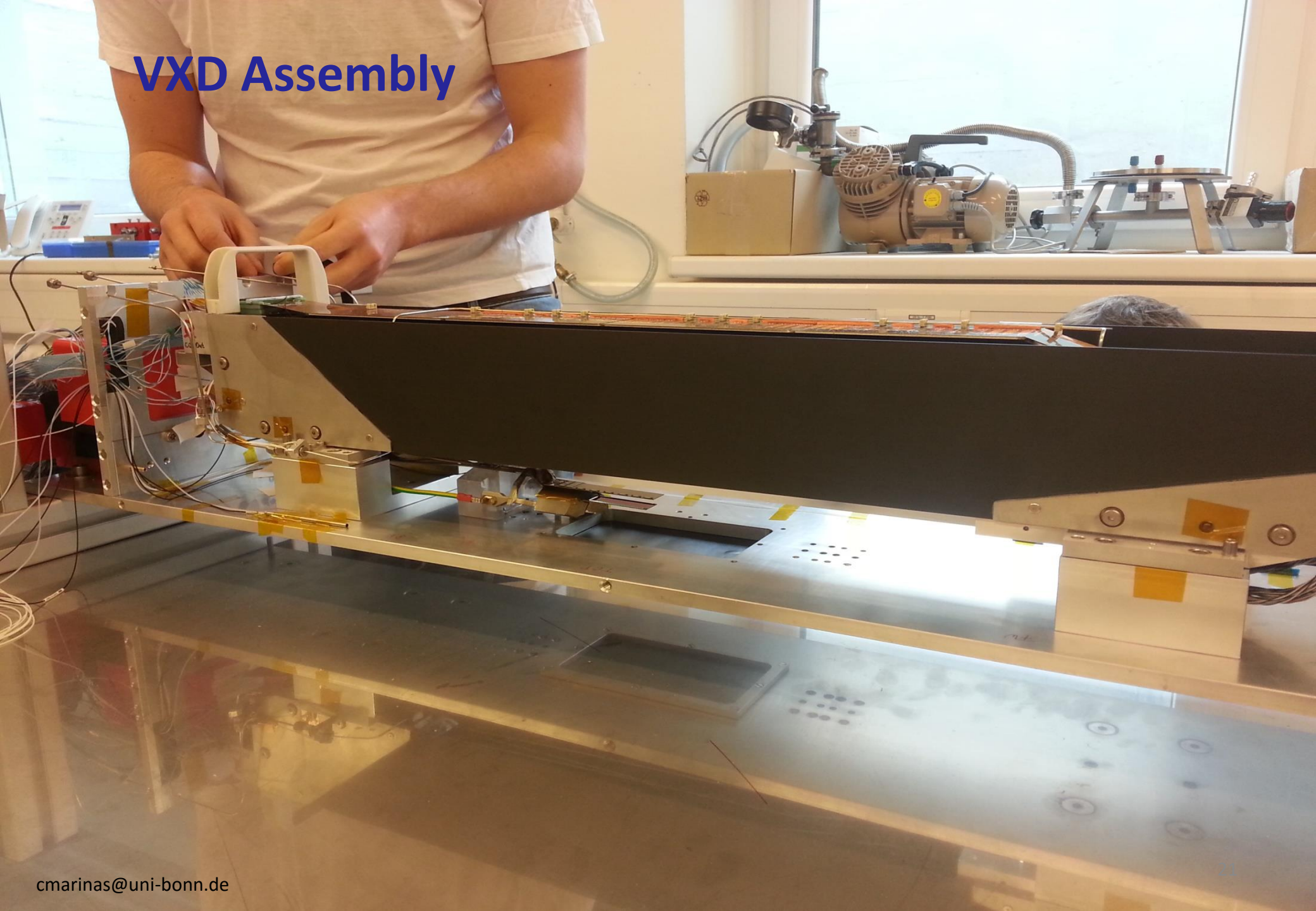
# PXD on the SCB



# SVD Cartridge



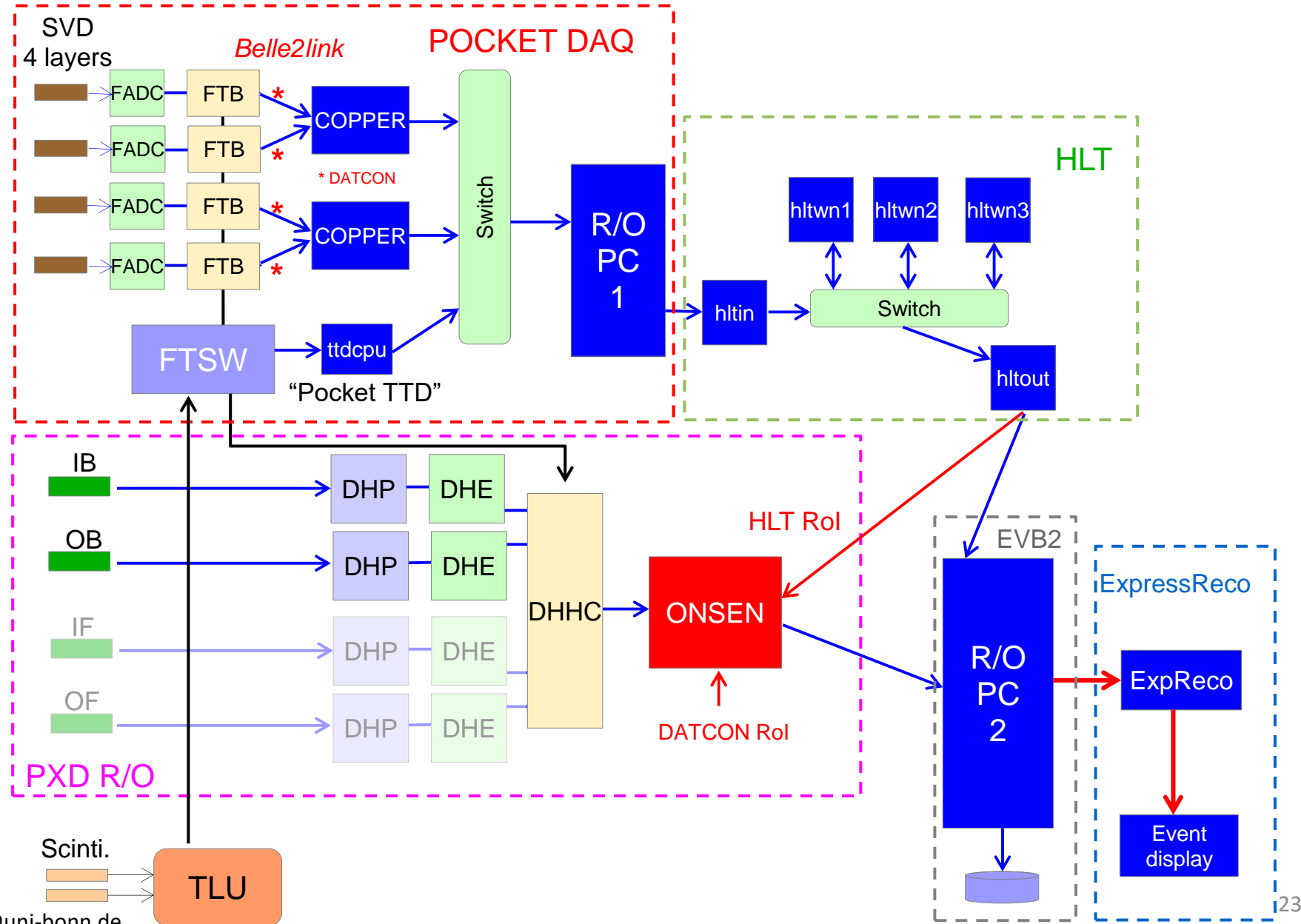
# VXD Assembly



# Integration into PCMAG

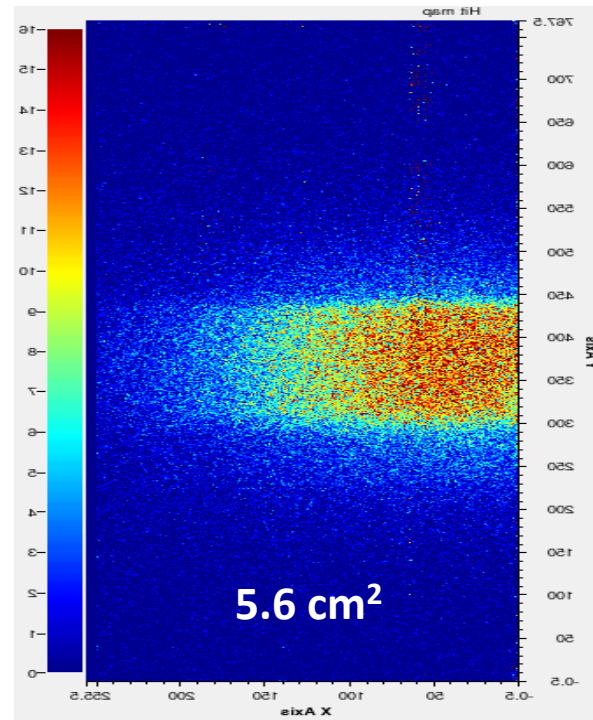
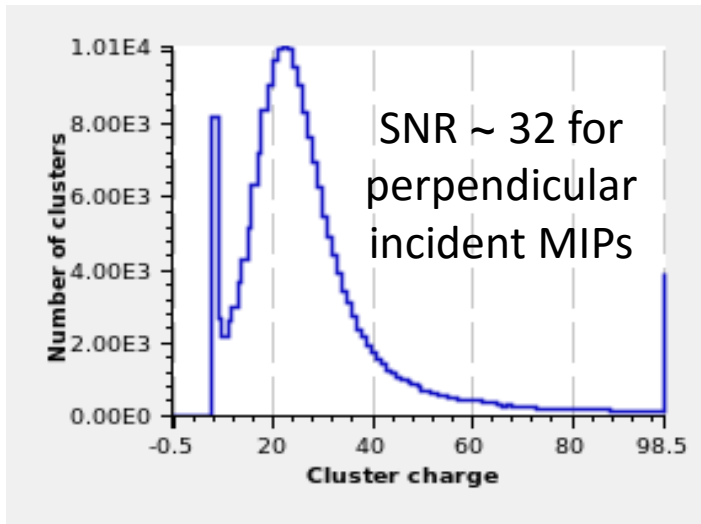


# VXD-Test Beam DAQ Structure

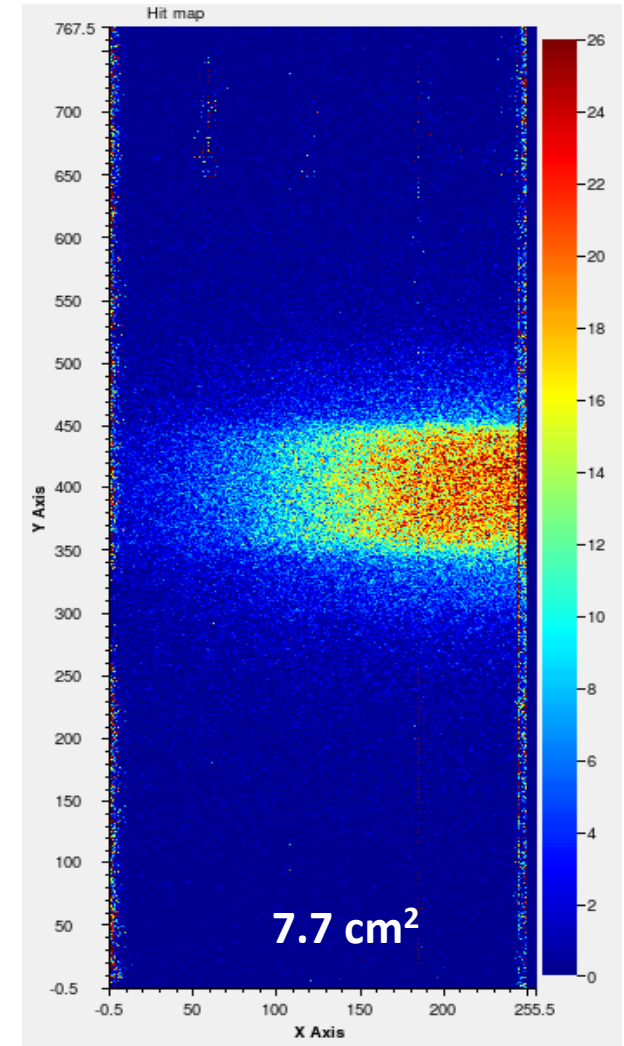


# PXD Hit Maps

- Threshold = 5 (~ 1200 electrons)
- MIP ~ 6000 electrons



Inner Backward

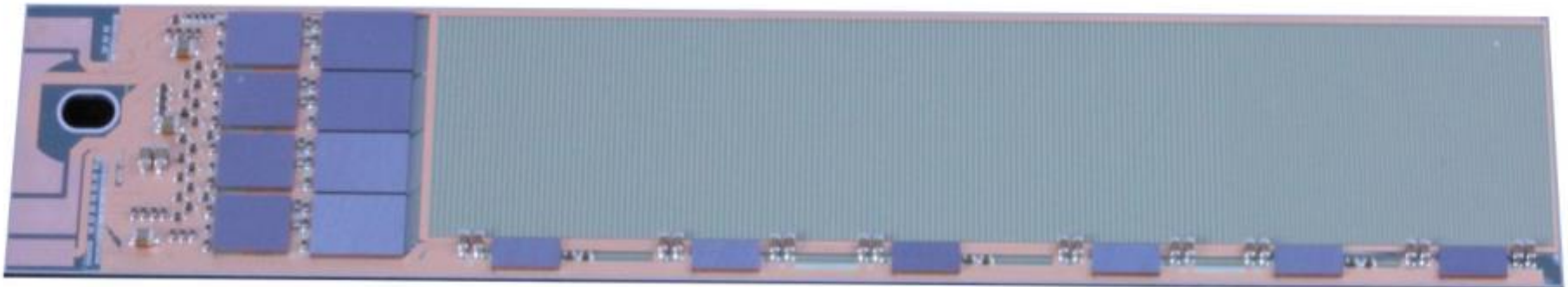
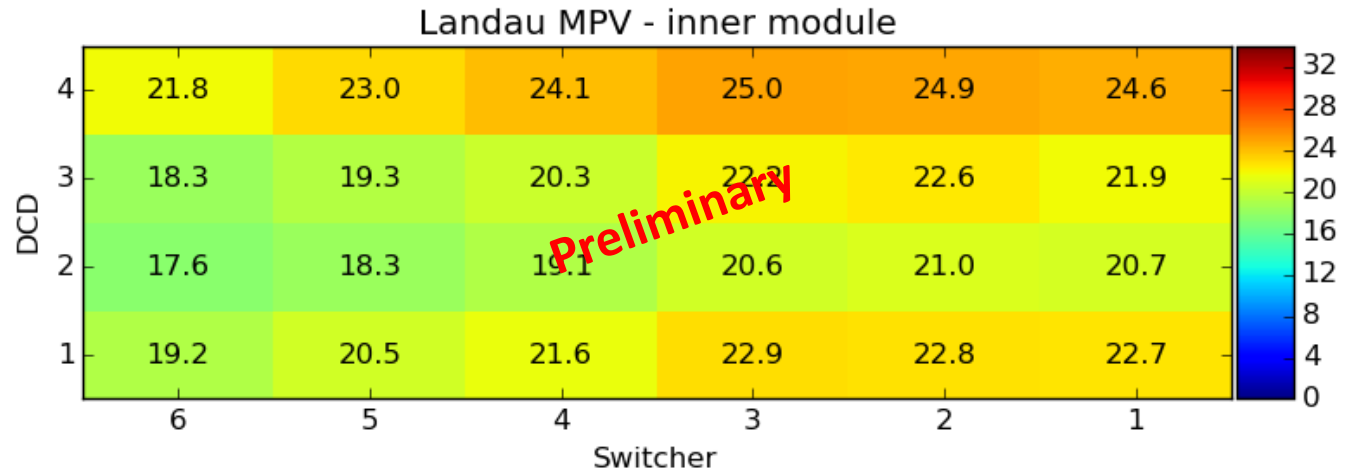
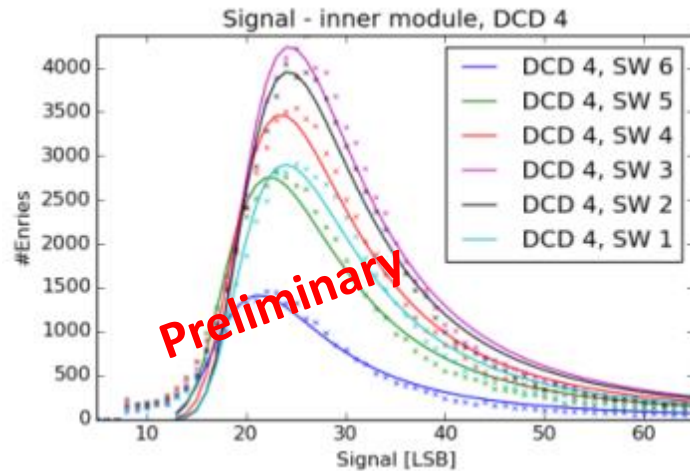


Outer Backward

Trigger on 4 scintillators  
Collimated beam  
No magnetic field

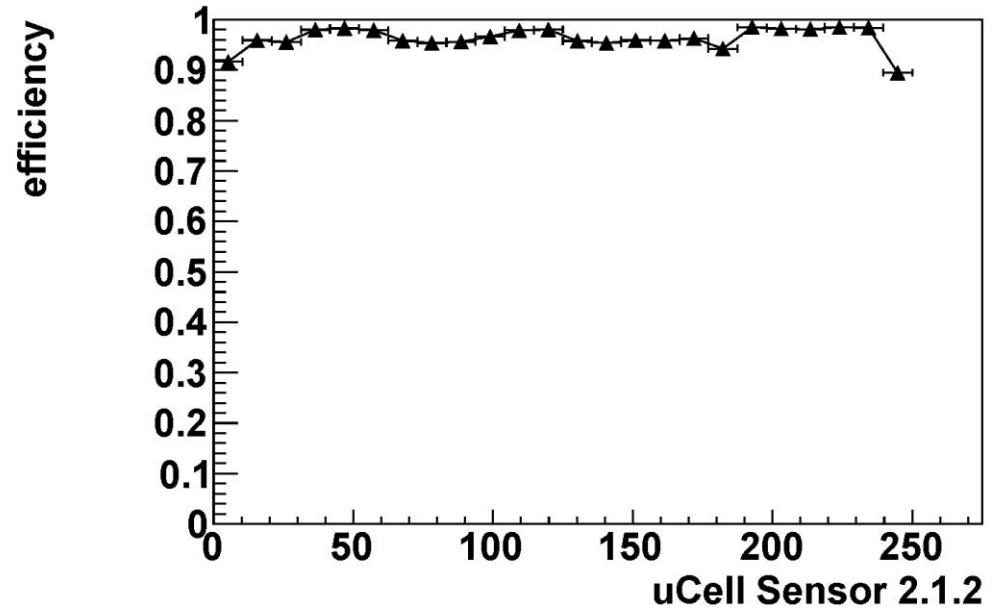
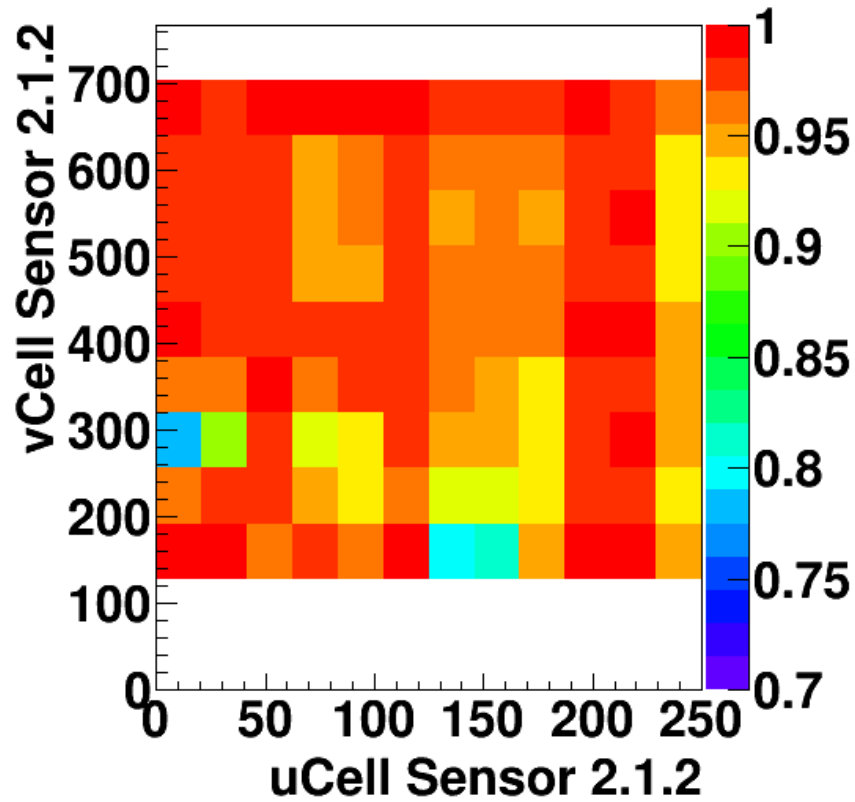


# PXD Signals



- The response from the matrix is rather uniform even without tuning. Modules just worked using operating parameters from Hybrid 5
- There is lot of room for improvements with better optimization of voltages and ASICs

# PXD Efficiency

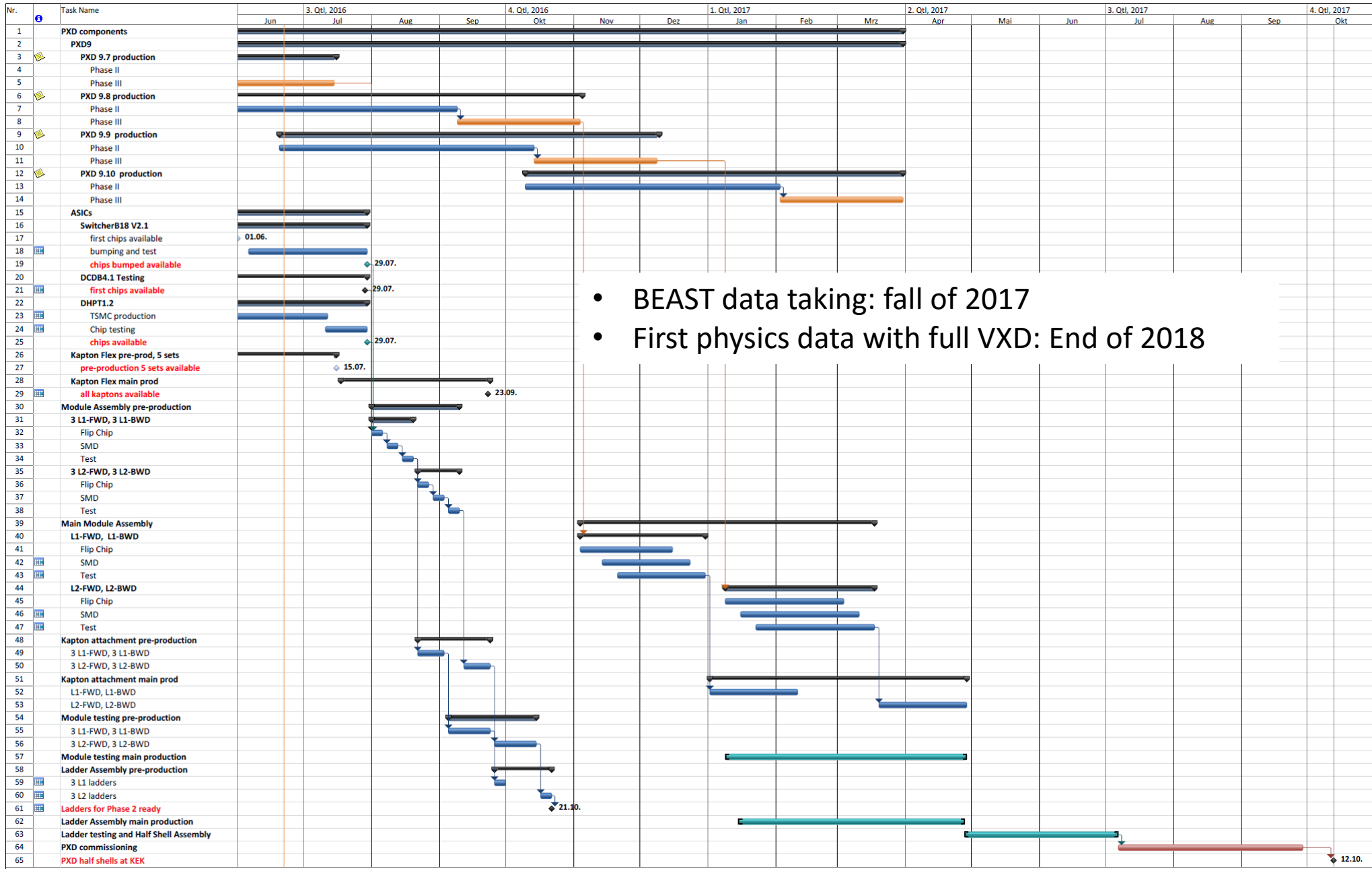


Efficiency >95%

# Conclusion

- Full scale detector demonstrator: Sensor and ASICs OK
- 2 PXD layers fully operational with SVD: 'Final' Phase 2 hardware
  - High SNR and efficiency, residuals according to specs
  - Only possible with an operational DAQ system
  - Slow control and monitoring system ready
- Preparations for the BEAST commissioning phase started
- Mass detector production will follow

# Schedule



- BEAST data taking: fall of 2017
- First physics data with full VXD: End of 2018



**Thanks**