Resoconto Elettronica Digitale NUCL-EX

per Consiglio di Sezione INFN-Firenze

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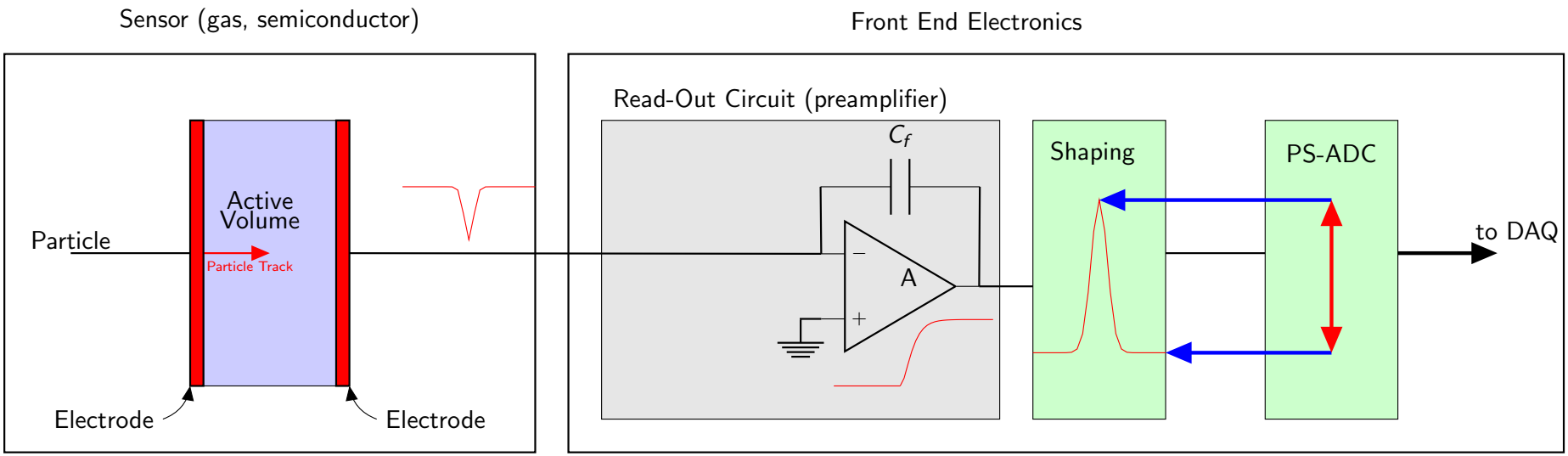
Peak Sensing-ADC vs Sampling-ADC

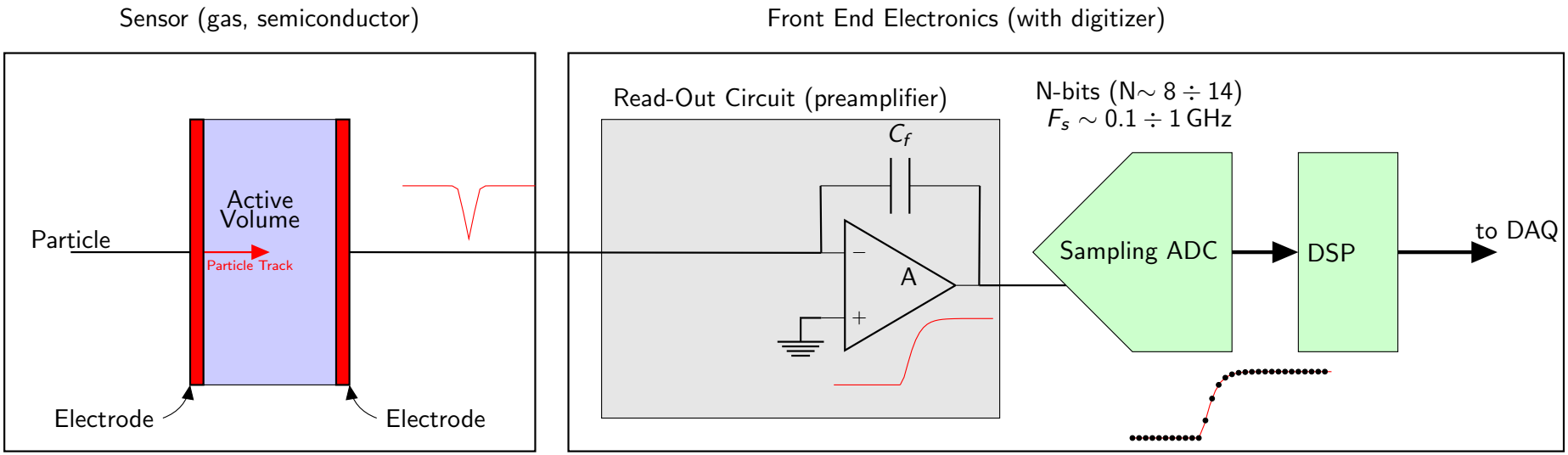


Standard analog Front End for energy measurement:

- current integrated by CSA (amplitude $\approx -Q/C_f$ if $A \gg 1$);
- linear shaping (e.g. semi-gaussian);
- shaped output amplitude converted into binary by ADC (single A/D conversion);

Signals are processed by analog electronics until info can be extracted in a single A/D conversion.

Peak Sensing-ADC vs Sampling-ADC



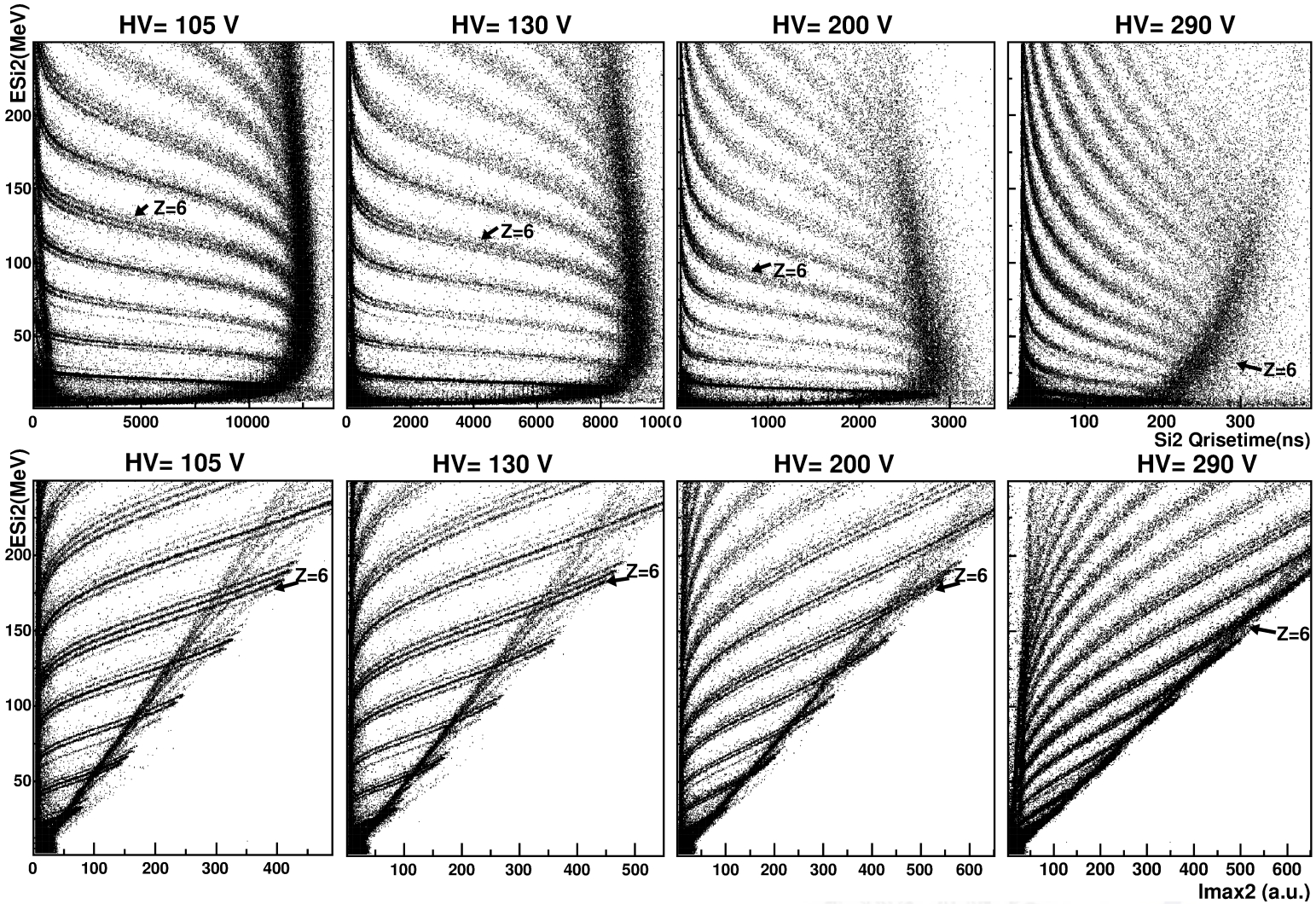
Sampling based Front End:

- Preamp signal is "sampled" (converted to *digital signal*);
- digital: discrete both in time and amplitude;
- DSP (Digital Signal ProcessING) techniques on dedicate μprocessors (Digital Signal ProcessORs), programmable logic units (FPGAs) or standard CPUs.

Advantages of digitizers

- better stability with respect to analog circuits
- flexibility (processing just a matter of calculation)
- easy pulse shape analysis implementation
- predictable and reduced dead time
- easy implementation of pile-up rejection
- processing not possible with analog can be implemented

Example: PSA in Si detectors

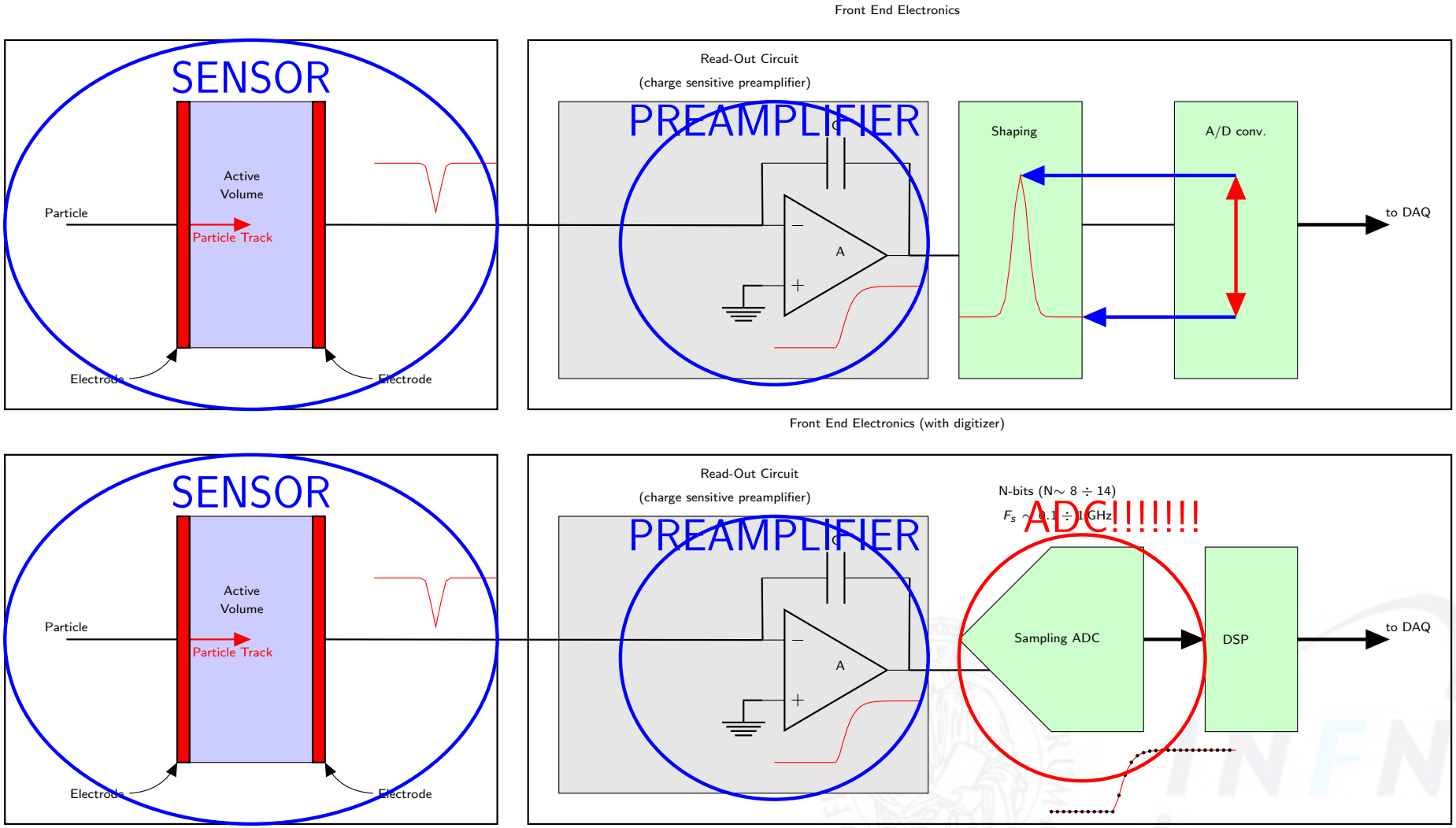


Dis-advantages of digitizers

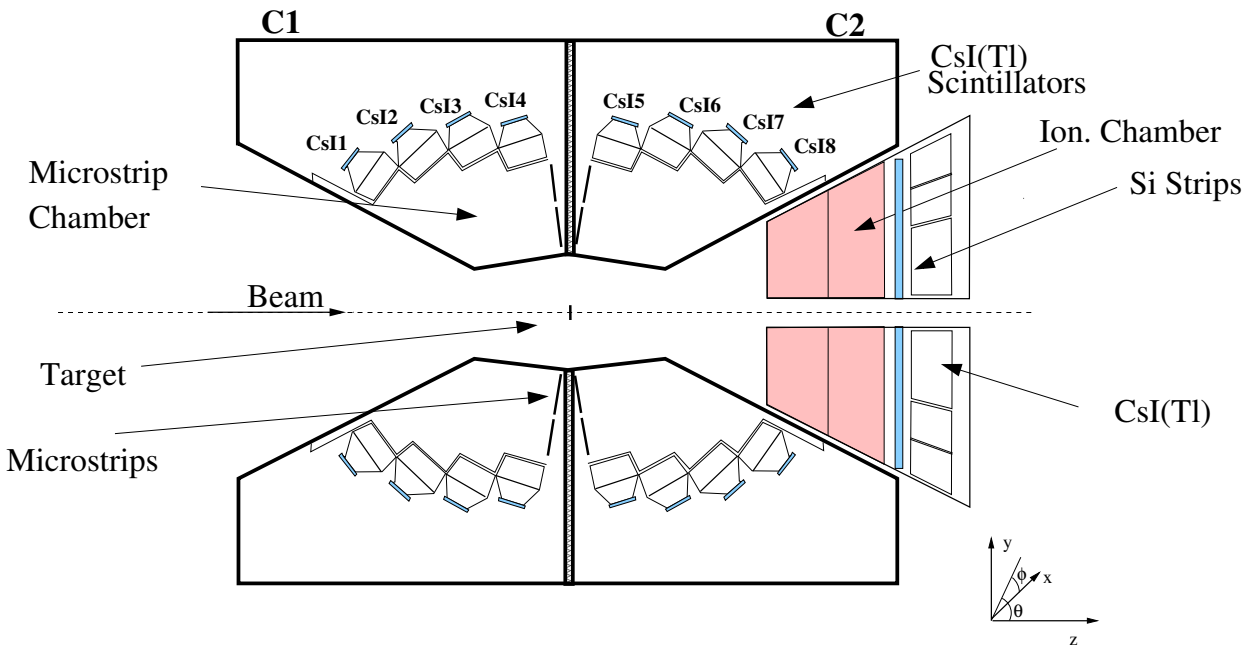
- bandwidth limit+aliasing, loss of info for “fast” signals
- interpolation needed for “original” signal reconstruction
- additional noise from sampling ADC
- huge amount of data to handle

ADC contributes to noise

NOISE SOURCES EVIDENCED BY ELLIPSES!

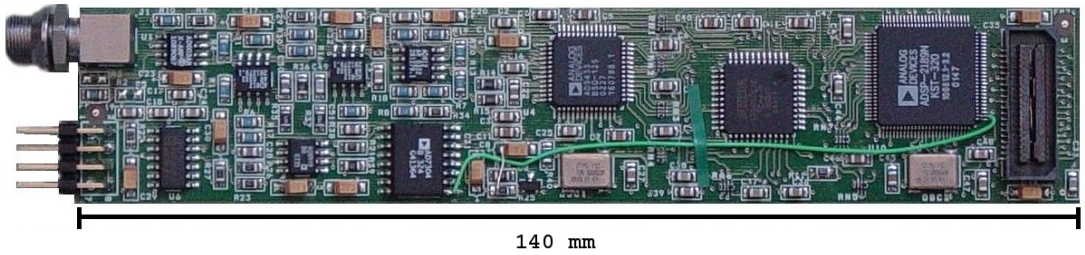


GARFIELD+RCo at LNL

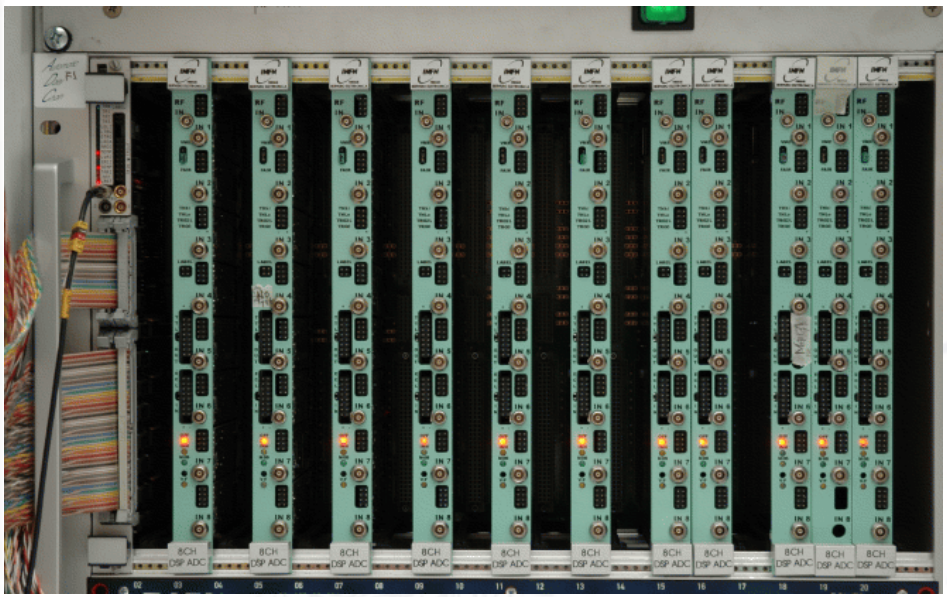


- GARFIELD: Drift chambers + CsI(Tl)
- RCo (Ring Counter): Ion Chamb. + Si + CsI(Tl)
- all detectors (except part of Drift Ch.) digitized

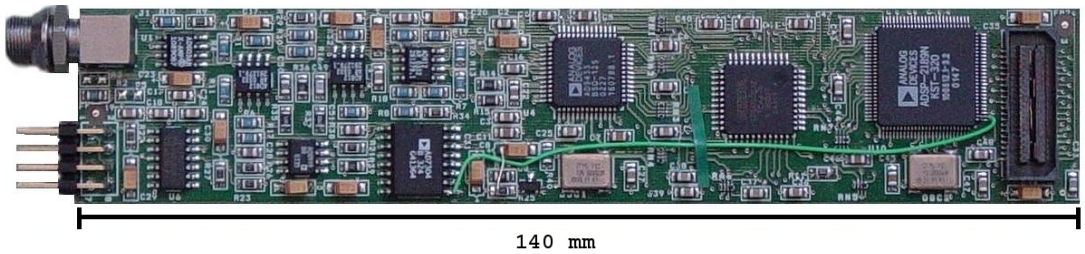
GARFIELD+RCo at LNL: digitizers (start 2003)



- 1 channel/board
- 12 bit; 125 MSPS
- 9.5 ENOB
- sel. polarity



GARFIELD+RCo at LNL: digitizers (start 2003)



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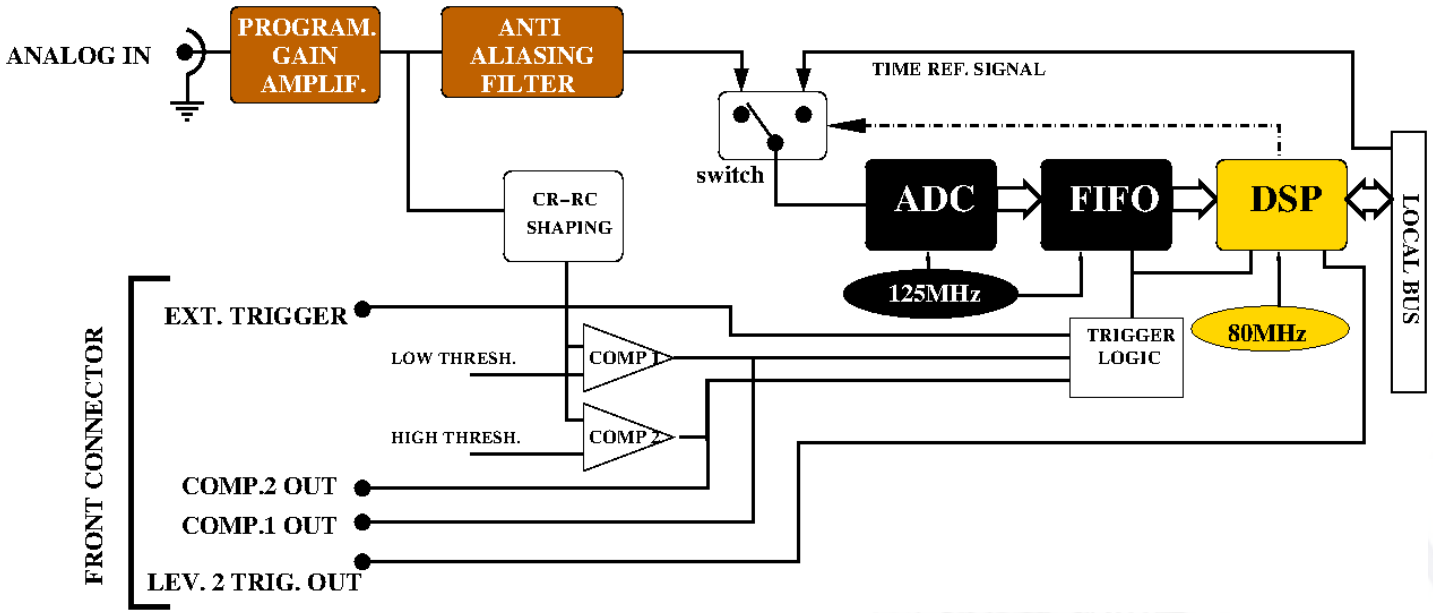
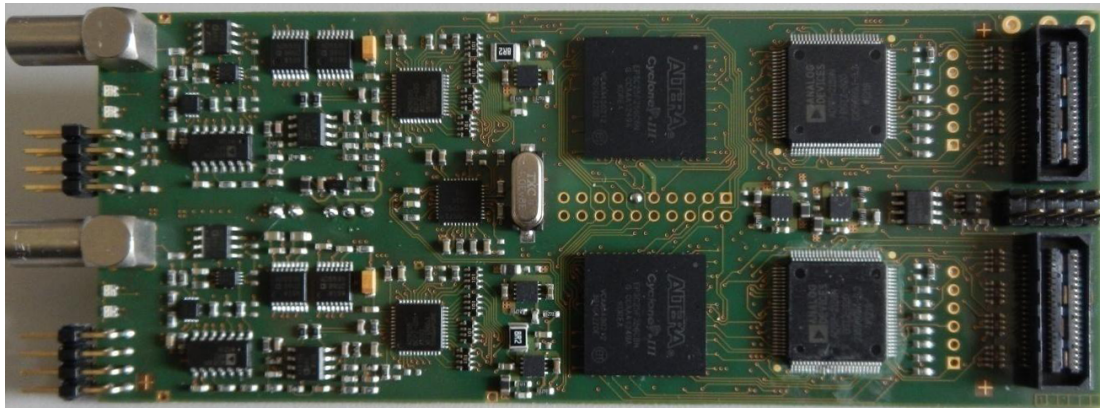
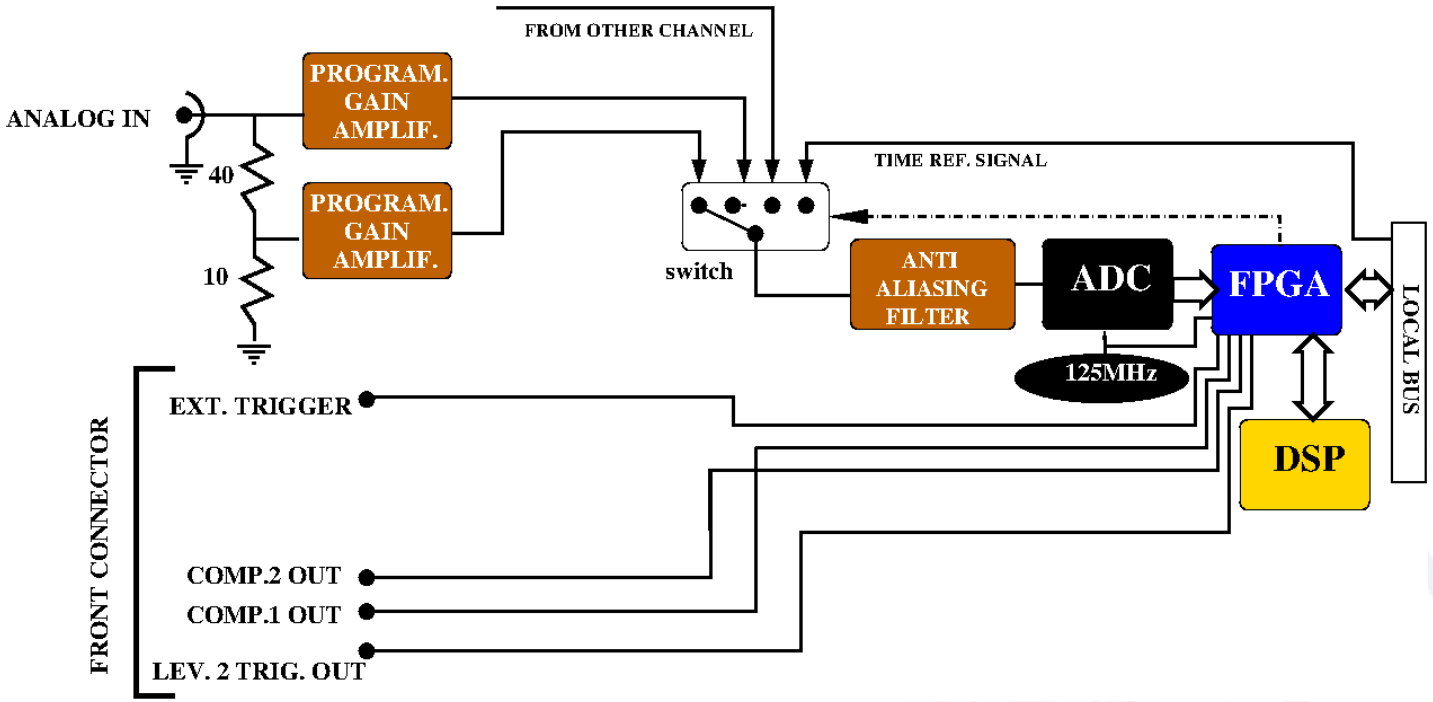


GARFIELD+RCo at LNL: new digitizers (start 2011)



- 2 channel/board
- 14 bit; 125 MSPS
- 11.5 ENOB
- adj. DC offset



New digitizer

- design: Stefano Meneghini (INFN-Bo), Luigi Bardelli, Maurizio Bini, G.P.
- 14 bit; 125 MSPS;
- two dynamic ranges (better SNR); adjustable range from 100 mV to 10 V
- DC coupled
- adjustable DC offset (polarity selection)
- two channels per board (sampling clocks have opposite phase)
- FPGA centric
- cost: about 300 euros/channel
- DSP: ADSP2189N; FPGA: Altera Cyclone III; Clock gen: AD9572
- VCA: AD8337; ADC: AD9255

New digitizer: timeline

- June 2010: first contacts
- Fall 2010: components defined, simulations
- April 2011: 1st scheme
- Feb 2012: 1st 2 prototypes
- Spring 2012: 1st tests
- Summer-Fall 2012: work on masses, components, etc. to reduce noise
- Winter 2012: new corrected design v3.0
- May 2013: new prototypes
- Jan 2014: last noise tests OK
- May 2014: tender for production (44 pcs)
- Oct 2014: 1st 2 prototypes
- Spring 2015: 44 boards produced, start work on advanced firmware (Pietro Ottanelli)
- Dec 2015 1st 2 prototypes new production; test of firmware+board in realistic conditions at LNS
- May 2016: 21 boards produced

Firmware for the on-board FPGA (Cyclone III)

- written in VHDL
- acquisition logic
- trapezoidal shaper with pole-zero canc. for energy measurements;
- internal trigger system (bipolar shaper+zero crossing);
- state machine to directly access the EPCS (E2Prom memory device) to write the FPGA firmware without using the JTAG cable;
- trigger management logic which allows for using complex trigger schemes (more than 1 trigg source possible)
- use of a PLL on the FPGA to change relative phase shift between ADC clock and FPGA clock (avoid errors when reading samples from the ADC);
- Finite Impulse Response filter for real-time interpolation with cubic-splines (with optional derivation)
- real-time extraction of Imax

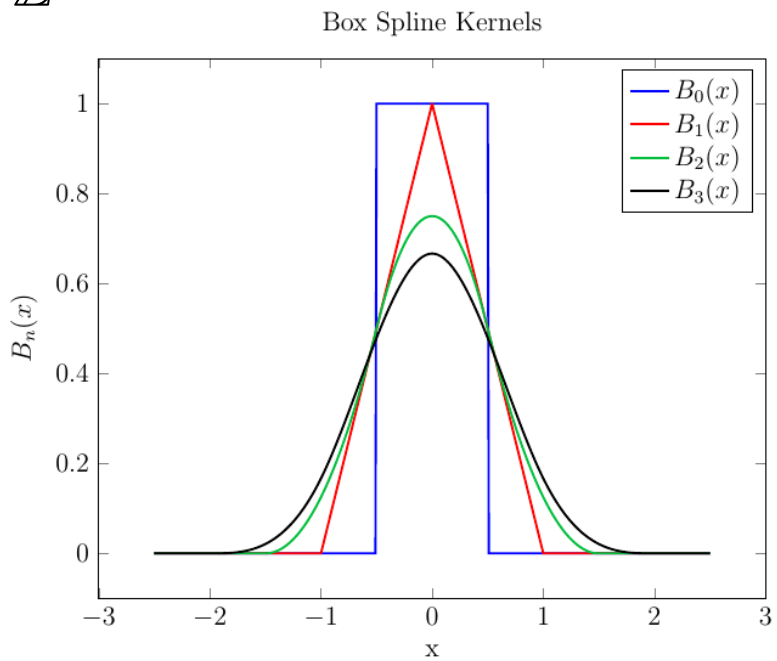
Interpolation basic principles

Starting from samples $x[n] = x(n\,t_s)$, look for $g(t)$ in

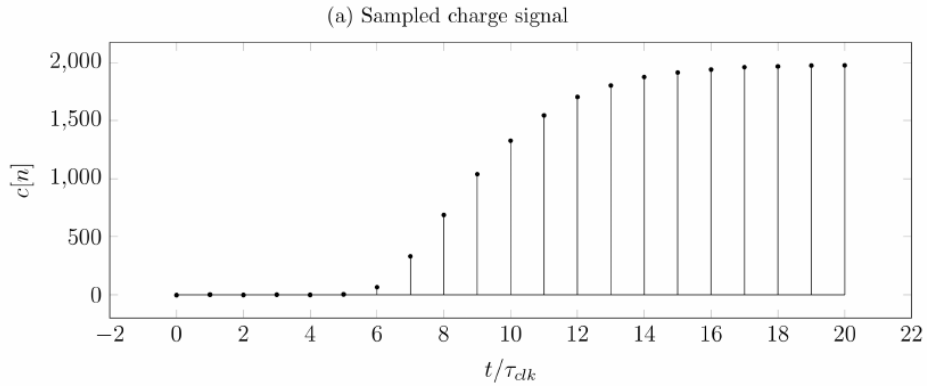
$$K(f,\, t_s) = \left\{ g(t) \mid g(t) = \sum_{m=-\infty}^{+\infty} b[m]\, f(t/t_s - m) \right\}$$

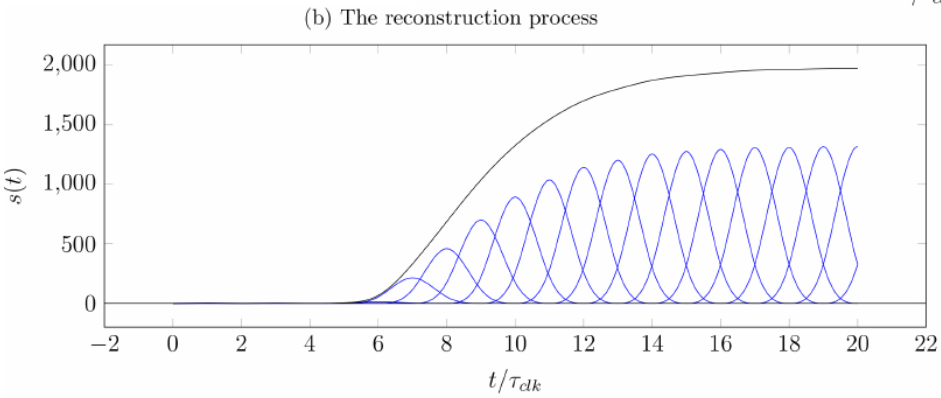
Find member of K passing through the samples:
$\sum_{m=-\infty}^{+\infty} b[m]\, f(n-m) = x[n] \quad \forall n \in \mathbb{Z}$

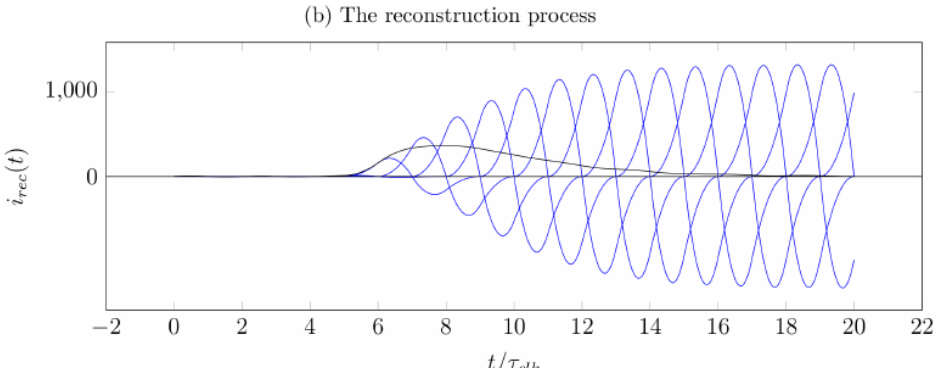
E.g.: $f(t)$ is a box-spline:

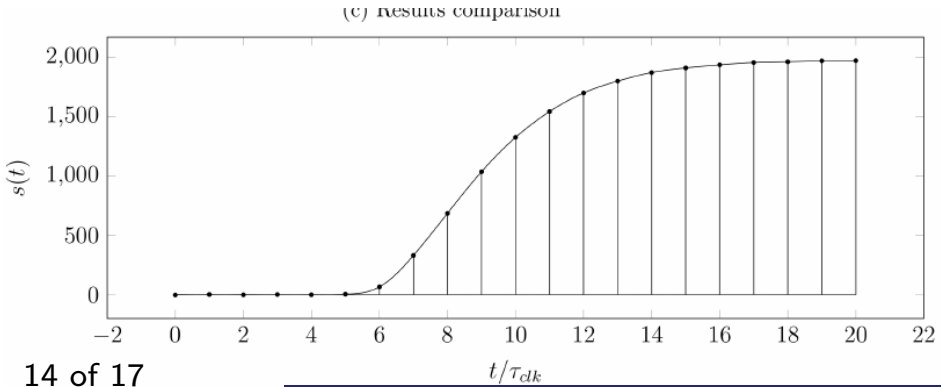


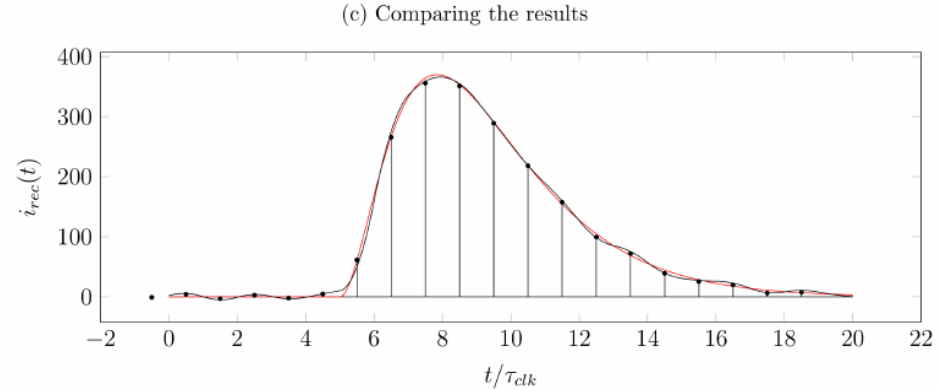
Interpolation examples (w/ and w/o derivation)



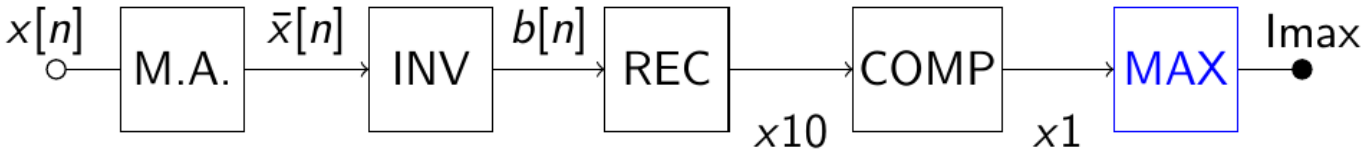








Interpolation firmware



- first a Moving Average is applied (MA);
- linear filter (INV) produces the coefficients;
- reconstructing filter (REC) produces 10 samples for each clock;
- pipelined algorithm (COMP) compares 10 samples per clock;
- maximum value is stored (1 per clock);
- blue block (MAX) searches for the maximum of its input.

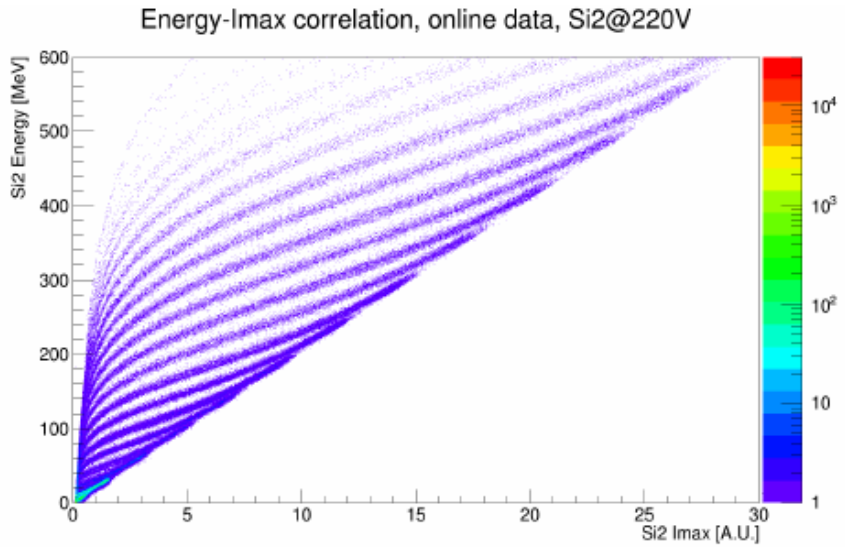
PSA on-line on-board

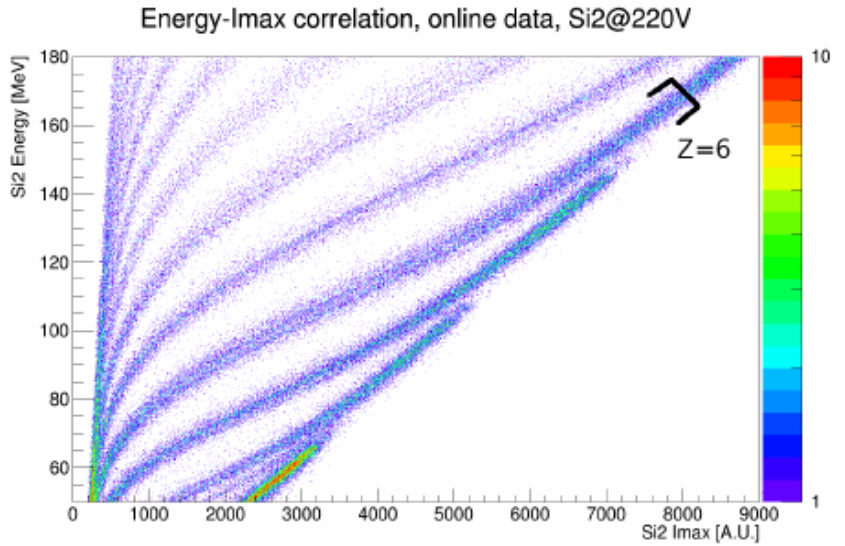
Test results:

- derived charged signal produced
- hi dynamic range (2 GeV)
- PSA res. limited by ADC noise

Future developments:

- new digitizers integration in GARFIELD acq
- interpolation with “smoothing” splines
- new measurement with higher gain (better SNR)
- test with coupled channels
- on-line interp also in FAZIA?





Thank you!